

MOST

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST150 oPhy Compliance
Measurement Guideline**

**Rev 1.1
06/2010**

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Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

	Document	Revision
[1]	MOST Specification	3.0
[2]	MOST Basic Physical Specification	1.0
[3]	MOST150 oPhy Automotive Physical Layer Sub-Specification	1.1
[4]	MOST Compliance Requirements	2.0

MOST Document references

	Document	Revision
[5]	IEC 60958-3 Digital audio interface - Part 3: Consumer applications	June 2006
[6]	IEC 61280-2-2 Fibre optic communication subsystem test procedures - Part 2-2: Digital systems - Optical eye pattern, waveform and extinction ratio measurement	March 2008
[7]	IEC 60825-1/ Safety of laser products - Part 1: Equipment classification and requirements	-
[8]	IEC 60825-2 Safety of laser products - Part 2: Safety of Optical Fibre Communication Systems (OFCS)	-
[9]	JIS 6863 Test Methods for Attenuation of All Plastic Multimode Optical Fibers	January 1990
[10]	ANSI/TIA-455-126 Spectral Characterization of LEDs	November 2007
[11]	TIA/EIA-644-A-2001 Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	2001
[12]	JEDEC No. JESD8C.01 Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits	
[13]	IEC 61300-3-4 Fibre optic interconnecting devices and passive components - Basic test and measurement procedures - Part 3-4: Examinations and measurements - Attenuation	

Other documents

Document History

Changes Rev. 1.0 to Rev. 1.1

Change Ref.	Section	Changes
1V1_001	3.7	Adaptation of undershoot mask
1V1_002	5	Absolute figures for t_{off4} etc. eliminated

Revision 1.0

Change Ref.	Chapter	Changes
1V0_001	All	Initial version.

Terminology and Abbreviations

Abbreviation	Explanation
AJ	Alignment Jitter
AWG	Arbitrary Waveform Generator
EOC	Electrical Optical Converter
FOT	Fiber Optic Transceiver
NIC	Network Interface Controller
OEC	Optical Electrical Converter
PG	Pattern Generator
PLL	Phase Lock Loop
POF	Plastic Optical Fiber
SDA	Serial Digital Analyzer
SMD	Surface Mount Device
SP	Specification Point
THM	Through Hole Mount
TJ	Transfer Jitter
UI	Unit Interval

1 General Remarks

1.1 Introduction

This document *MOST150 oPhy Compliance Measurement Specification* specifies basic measurement methods, relevant for verifying compatibility of networks, nodes, modules, and components with the requirements specified in the documents *MOST Basic Physical Specification [2]* and *MOST150 oPhy Automotive Physical Layer Sub-Specification [3]*.

This document shows basic measurement principles and setups for all specified parameters in [3]. There might be other options for determining parameters, which are more suitable for characterization and end-of-line testing in the supply chain. Selection and definition of an appropriate test strategy is in the responsibility of the supplier. However, all used measurement procedures shall provide measurement traceability to the basic principles shown in this document.

For the majority of parameters, the specification [3] is defined as an interface specification. Parameters and the requested performance ranges are stated for components sending into the interface. The same performance ranges need to be considered as input tolerances for components being connected to the interface as receiver. For verification of output performance of a component that sends into an interface, the input variations have to be considered – if they exist.

The process of compliance verification is defined in the MOST document *MOST Compliance Requirements [4]*. It describes how to achieve compliance certification for MOST subsystems (devices) and components.

For documentation clarity some values of MOST150 oPhy Automotive Physical Layer Sub-Specification [3] are used within this document. In case of discrepancies with the MOST150 oPhy Automotive Physical Layer Sub-Specification, the MOST150 oPhy Automotive Physical Layer Sub-Specification shall be deemed the controlling document.

1.2 Operating Conditions

Temperature range for modules or components $T_A = -40^{\circ}\text{C}$ to $+95^{\circ}\text{C}$ according to [3].

Voltage range for modules or components $3.3\text{ V} \pm 5\%$ according to [3].

Note that there are functional requirements for the EOC within an extended voltage supply range according to [3].

1.3 Measurement Tools, Requested Accuracy

State-of-the-Art Tools:

- **Digital Oscilloscope**
 - DSO Type
 - $\geq 10\text{ GS/s}$
 - $\text{BW} \geq 1.5\text{ GHz}$
 - Sampling Memory $\geq 10\text{ MSample}$
 - Active Probe (single-ended, differential)
- **High-speed OEC:**
 - $\text{BW} \geq 250\text{ MHz}$ (DC-coupled) for b0/b1 measurement to calculate extinction ratio r_{e2}
 - $\text{BW} \geq 750\text{ MHz}$ (DC- or AC-coupled) for all other measurements
 - Performance recommendation

- Response flatness: 1 dB
(Constant Gain over BW; linear transfer function over the opt. input range)
- Low DC Offset error
- **High-speed EOCs**
 - Light source with a pulse shape representing a “high bandwidth emitter”
 - Transition time $t_r, t_f < 1.00$ ns
 - Overshoot > 1.25 of Normalized Amplitude
 - Extinction Ratio: 10 to 12 dB
 - Light source with a pulse shape representing a “low bandwidth emitter”
 - Transition time t_r, t_f between 1.00 ns and 0.5 UI
 - Overshoot: No overshoot
 - Extinction Ratio: 10 to 12 dB
- **Optical power meter:**
 - Accuracy: better than ± 0.25 dB
 - Accuracy optical power meter and SP2 adapter better than ± 0.5 dB
 - Wavelength: 650 nm
 - Range: > 0 dBm ... < -60 dBm
 - Trigger input (for timing measurements)
- **Ampere meter:**
 - Accuracy: better than 2 μ A
 - Trigger input (for timing measurements)
- **Pattern generator for generating MOST150 stress pattern:**
 - BW 300 Mbit/s
 - Trigger output (for timing measurements)
- **Optical attenuator:**
 - Attenuation up to 40 dB
 - Preferably attenuation via gray filter, not via air gap
- **Optical Y – coupler**
- **Optical spectrometer**
 - Resolution ≤ 1 nm
 - Spectral range at least 500 nm – 800 nm

2 Electrical characteristics

2.1 Test according to LVDS

Testing of devices, modules, or components has to be performed according to the measurement methods and setups specified in [11]. Parameters and their respective limits are also derived from [11], with on exception: according to [3], V_{CM} is specified in a tighter range.

2.2 Test according to LVTTTL

Testing of devices, modules, or components has to be performed according to [12].

3 Optical Characteristics

3.1 Measurement of Optical Output Power @ SP2

The optical power measurement setup is given in Figure 3-1. This measurement adapter allows the test of parameter P_{opt2} considering the specified note “Power within a far field angle of 30° ($NA = 0.5$) and a diameter of 1.0 mm”.

The optical power at SP2 is transferred by a glass fiber with a numerical aperture of greater than 0.5, a core diameter of 1000 μm , and a typical length of 30 mm. An aperture between glass fiber and photo detector confines the transferred beam to the required numerical aperture of 0.5. The size of the aperture is dependent of the distance between glass fiber and the aperture (see Figure 3-2). The end face of the glass fiber must be polished to avoid scattering and a conversion of the beam waist from SP2 to the end of the glass fiber. The glass fiber is mounted into a MOST compatible ferrule, which can be inserted into an SP2-contact of a MOST device for measuring the optical power at SP2.

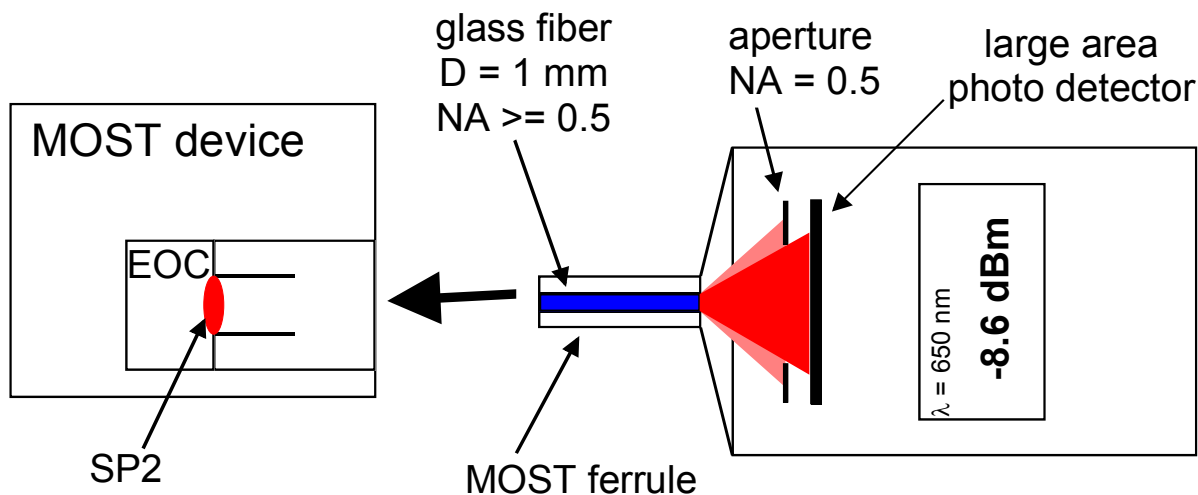


Figure 3-1: Schematic of optical power meter

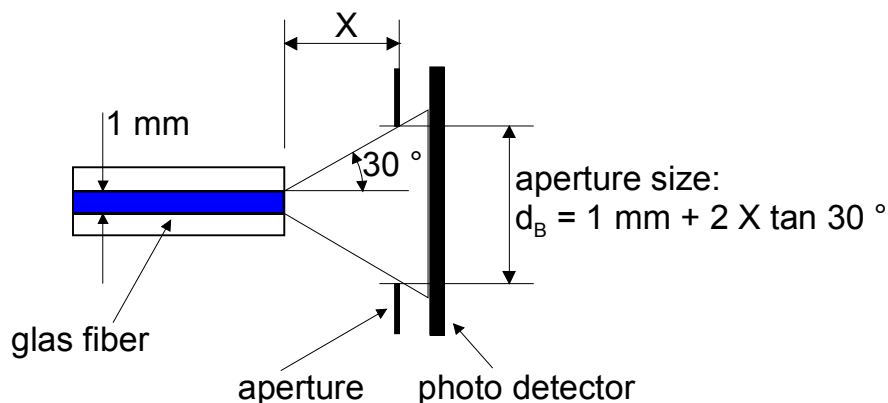


Figure 3-2: Calculation of aperture size d_B

Note: It should be ensured that the size of the photo detector is large enough to receive all the light after the aperture.

3.2 Measurement of Optical Input Power @ SP3

The optical power measurement setup is given in Figure 3-3. This measurement allows the testing of the parameter P_{opt3} considering the specified note “Power within a far field angle of 30° ($\text{NA} = 0.5$) and a diameter of 1.0 mm ”.

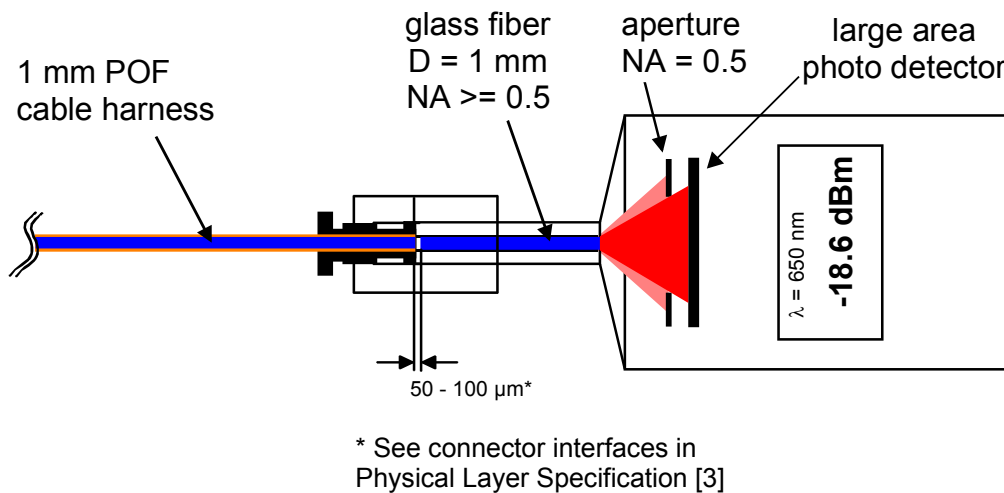


Figure 3-3: Optical power measurement setup for SP3

A glass fiber and an aperture transfer the measured optical power on a large area photo detector. For description and the calculation base for the aperture see section 3.1.

In [3], P_{opt3} is described as value, when the incoming signal has passed the receiving contact end face. Compared to the glass fiber used in the measurement setup, the surface quality of a real SP3-contact may be worse. This could result in a slightly lower input power than shown by the measurement. However, this small mismatch is fully covered by the specified connection loss. The axial offset shown in the diagram considers a requirement defined in the connector interface drawings [3].

3.3 Measurement of PigTail Fiber Attenuation

Attenuation of a PigTail fiber can be measured using the Insertion method (according to IEC 61300-3-4 [13]). The measurement setup consists of a Light Source, a Mode Mixer (acc. [9]), a Launching Fiber for generating the stimulus signal. For detection of optical power, a power meter is used. The connection between DUT and power meter is realized with a secondary Launching Fiber or an equivalent arrangement.

The measurement is performed in two steps. The first step consists of the measurement of the initial power level P_{Initial} (see Figure 3-4) while the second step provides the measurement of the power level with the connected PigTail Fiber P_{DUT} (see Figure 3-5).

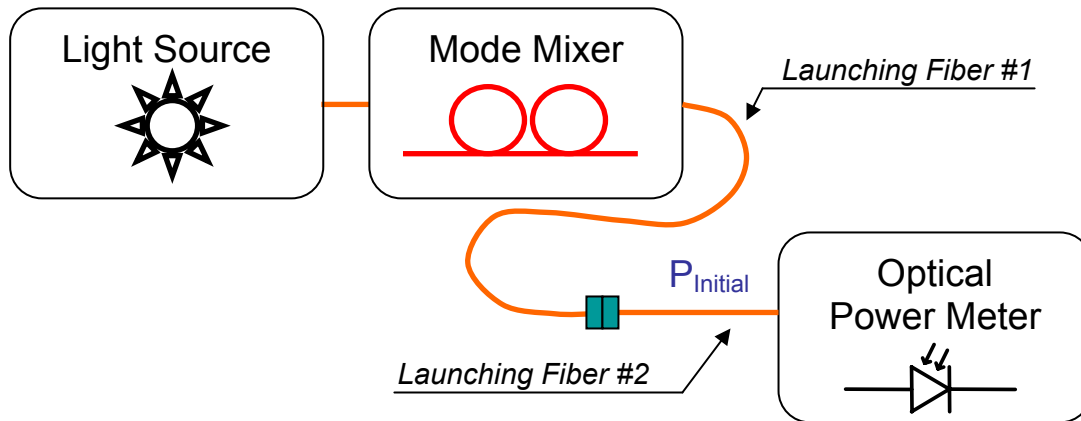


Figure 3-4: Measurement of $P_{Initial}$

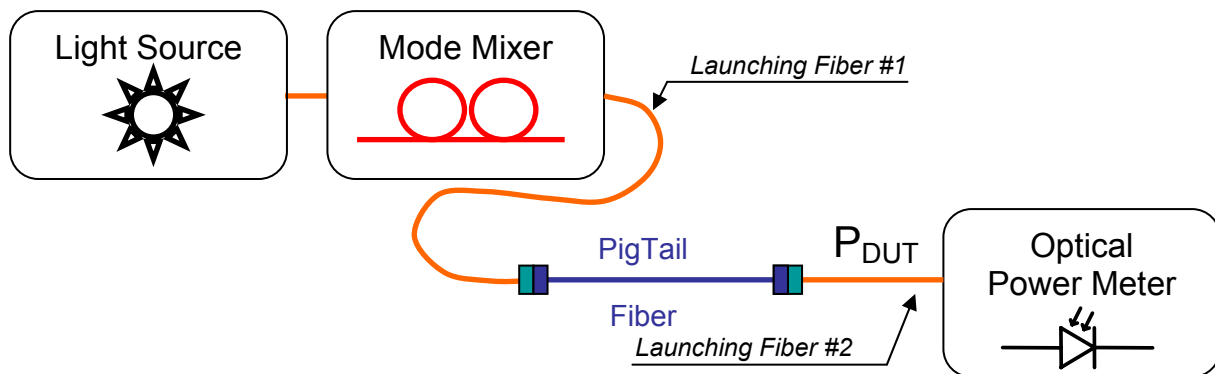


Figure 3-5: Measurement of P_{DUT}

The optical power is measured in logarithmic scale (dBm). The attenuation of the PigTail fiber is the difference between $P_{Initial}$ and P_{DUT} expressed in (dB).

$$A_{PigTail} = P_{DUT} - P_{Initial}$$

Practical Considerations:

In the MOST150 oPhy Automotive Physical Layer Sub-Specification [3], all optical power levels are measured within a spot of diameter 1 mm and an acceptance angle of 30°. This represents the coupling characteristic of a POF with NA = 0.5, which is typically used in the wire harness. The Light Source in combination with the Mode Mixer and the Launching Fiber #1 creates the equilibrium mode power distribution (EMD). The PigTail fiber is tested using EMD launch condition. The secondary Launching Fiber is used for interfacing with the PigTail fiber. It would also eliminate power above NA = 0.5, if exists. As long as the PigTail fiber does not modify the power distribution, the filter function of the secondary Launching Fiber is not required. For simplification, the Launching Fiber #2 can be replaced by a SP2-Adapter or equivalent setups.

For building up the test setup, optical terminals need to be created for interfacing with the SP2/SP3-contact geometry on one side and with the ferrules for the SMD-Transceiver on the other side. The contact shape of the FOT-side ferrules provides different diameters (mechanical coding); apart from that, the SP2/SP3 contacts have different contact dimensions. According to IEC 61300-3-4 [13], an adaptor may be used (known as “temporary joint” in [13]) for coupling of these differently shaped ferrules.

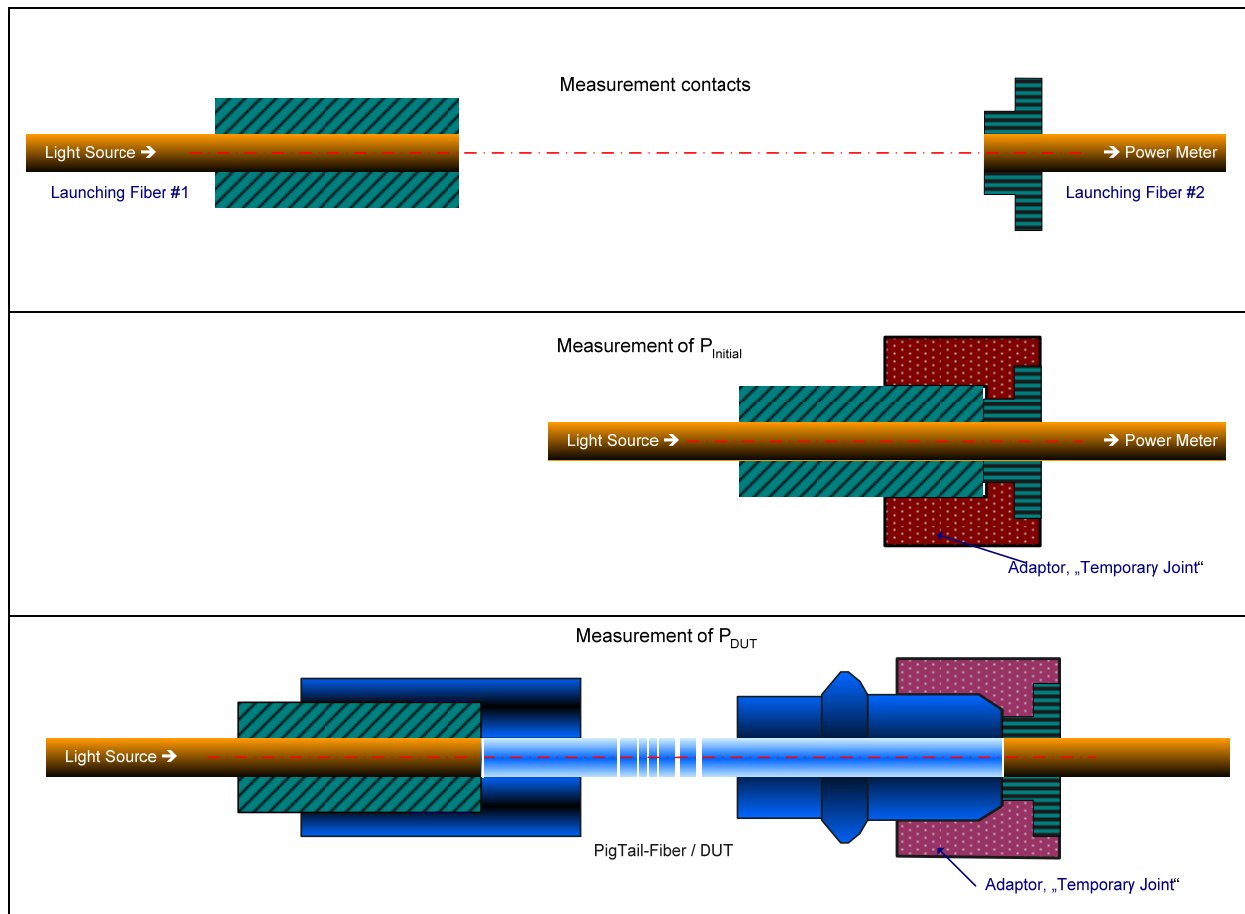


Figure 3-6: Usage of adaptors for matching different contact shapes

3.4 Spectral Parameters @SP2

Center Wavelength and Spectral Width (RMS)

The MOST150 oPhy Automotive Physical Layer Sub-Specification [3] defines the wavelength spectrum of a transmitter with the parameter center wavelength and spectral width. This is necessary to consider possible spectral asymmetries of state-of-the-art light sources. This measurement method is also a more precise definition for optical wavelength spectrums.

The measurement procedure is described in TIA-455-126 [10].

Note:

- measurement resolution shall be $\leq 1 \text{ nm}$
- S/N ratio for the measurement equipment at least 20 dB
- S/N ratio determines the part which is allowed to be cut from the spectrum
- Dark calibration necessary

Figure 3-7 shows an example of how to determine center wavelength and spectral width (RMS).

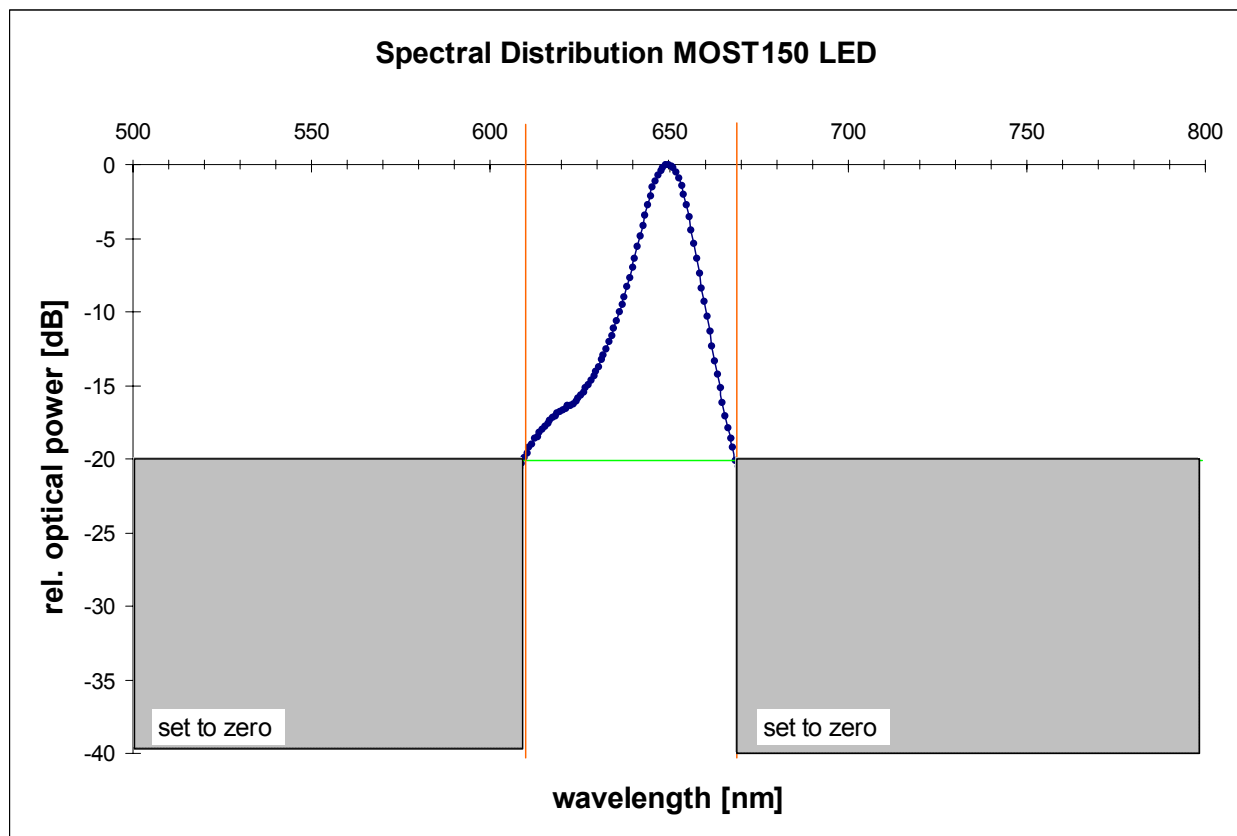


Figure 3-7: Example determination of spectral parameters.

3.5 b0/b1 Detection @SP2

To determine b0/b1 levels, the MOST150 stress pattern shall be used. At least 500 5UI- or 6UI-pulses need to be extracted out of the measured data. Extraction can be done by triggering on pulse-width ranges or by software based selection on a prior acquired waveform. b1 is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired high-pulses. B0 is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired low-pulses. t_{OSLS} and t_{OSLE} are defined in [3] and shown in Table 3-1.

Measurement Region	Value	Unit
t_{OSLS}	2.500	UI
t_{OSLE}	4.000	UI

Table 3-1: Optical Signal Level Measurement Interval

The measured optical amplitudes b1 and b0 are an integral part of further measurements at SP2. The accuracy of b1/b0 detection determines the accuracy of such a linked measurement. Any variation in a measurement setup or in the environmental conditions may change b1 and b0. Therefore, b1/b0-detection should be performed shortly before the linked measurement.

Basically, for detection of b1 and b0, DC-coupled or AC-coupled measurement-OECs may be used; however, there are severe restrictions given due to the corresponding measurement. Table 3-2 shows the parameters which are based on b1/b0 and the restriction for the measurement-OEC.

The DC offset of a DC-coupled OEC should be kept as low as possible. It is recommended to compensate a remaining offset using dark calibration. For accurate measurement results, it is important to achieve a sufficient signal-to-noise ratio.

Parameter	Symbol	Restriction	Usage of b1/b0
Extinction Ratio	r_{e2}	DC-coupled, BW>250 MHz	Calculation, ratio of b1 to b0
Transition Times	t_{r2}, t_{f2}	DC-coupled, BW>750 MHz AC-coupled, BW>750 MHz	Determination of the 20% / 80% amplitudes
Transferred Jitter	J_{tr2}	DC-coupled, BW>750 MHz AC-coupled, BW>750 MHz	Determination of the trip-point, 50% amplitude
Alignment Jitter	-	DC-coupled, BW>750 MHz AC-coupled, BW>750 MHz	Normalization of the amplitude for adjusting the eye mask
Overshoot/ Undershoot	-	DC-coupled, BW>750 MHz AC-coupled, BW>750 MHz	Normalization of the amplitude for adjusting the masks
<p>Note: In case of using an AC-coupled measurement-OEC for all measurements excluding Extinction Ratio, a DC-coupled OEC with lower bandwidth-setting such as used for MOST25 may be re-used for determination of Extinction Ratio.</p> <p>See section 1.3 for more detailed OEC requirements.</p>			

Table 3-2: Restrictions for Measurement-OECs

Figure 3-8 provides an example of how to measure b0 and b1 by a histogram method.

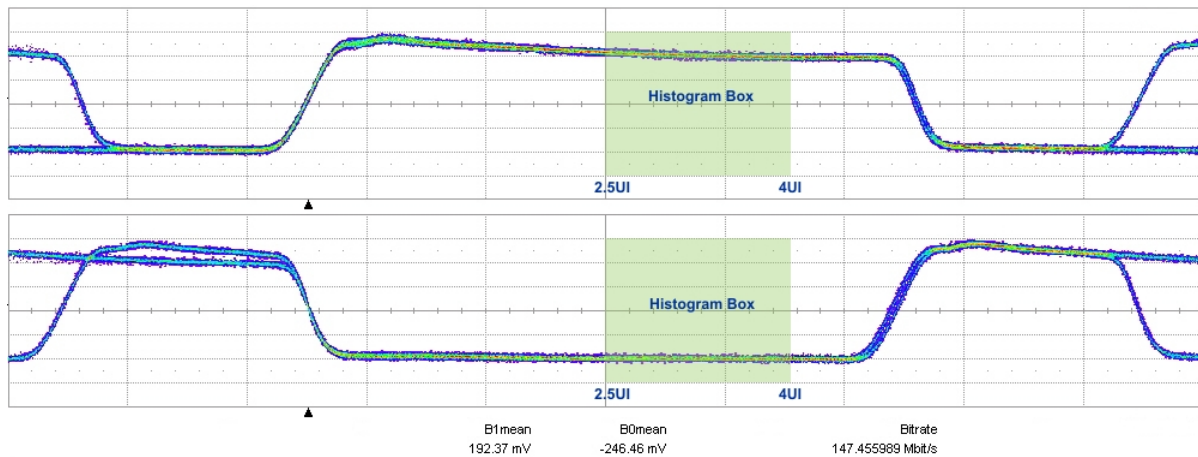


Figure 3-8: Detection of b0 and b1

3.6 Extinction Ratio @SP2

Extinction Ratio r_{e2} is calculated based on the measured optical levels for b1 and b0 as described in section 3.5 by using a *high precision DC coupled O/E-converter*.

Extinction Ratio r_{e2} is given with:
$$r_{e2} = 10 \cdot \log\left(\frac{b1}{b0}\right);$$

$$b1 = \text{OpticalHighLevel}$$

$$b0 = \text{OpticalLowLevel}$$

Note: For measuring b1 and b0, a *high precision DC coupled O/E-converter* shall be used.

3.7 Optical Overshoot and Undershoot @SP2

The optical pulse shape of an SP2 signal is tested with a parameterized mask. The mask parameters are given in normalized amplitude, which is based on the measured optical logic levels b0 and b1. Time parameters are specified in units of UI and the origin for the timescale is defined from the mid point of the rising or falling edge of the signal. Overshoot and undershoot measurements contain only one edge of a pulse class, which forms the trigger edge. Timing variations that might be included in the data stream and would be visible on subsequent edges are excluded from this measurement. The timing corridor given around the trigger point (overshoot H_O , C_O , undershoot G_U , R_U given in [3]) serves for tolerating noise coming from the measurement-OEC. The measured signal must not touch the “Keep Out” areas of the masks.

There are two basic strategies to perform the measurement.

1. Draw a mask that is adjusted in vertical and horizontal scale to the conditions (b1, b0, timing resolution) given by a particular measured waveform.
2. Predefine a fixed scheme for horizontal and vertical settings of the mask and normalize the measured waveform.

The following example shows an overshoot and undershoot measurement using the second option. The oscilloscope's display grid is used (10 divisions horizontally and 8 division vertically) to fix the tolerance scheme.

Example Overshoot:

Horizontally, a timeframe of 2 UI is displayed. According to the requested timing extremes of -0.63 UI (A_0 , F_0) and 1.37 UI (K_0 , E_0) given in the mask parameters [3], the zero-point is set to 3.15 divisions. Vertically, the 50% level of the amplitude swing is centered in the oscilloscope's grid; b0 is set to -2 divisions, b1 is set to +2 divisions, which gives sufficient headroom for displaying the maximum tolerable overshoot of 40%. The trigger is set to rising edge for all types of data pulses (2...6UI).

Normalization of the waveform's amplitude is done using the following formulas:

$$\text{normalized_amplitude}(i) = (\text{amplitude}(i) - \text{vertical_offset}) / \text{vertical_scale}$$

where

$$i = 1 : \text{waveform_length}$$

$$\text{vertical_offset} = (b1 + b0) / 2$$

→ 50%-level

$$\text{vertical_scale} = (b1 - b0) / 4$$

→ full swing ($b1 - b0$) is normalized to 4 divisions

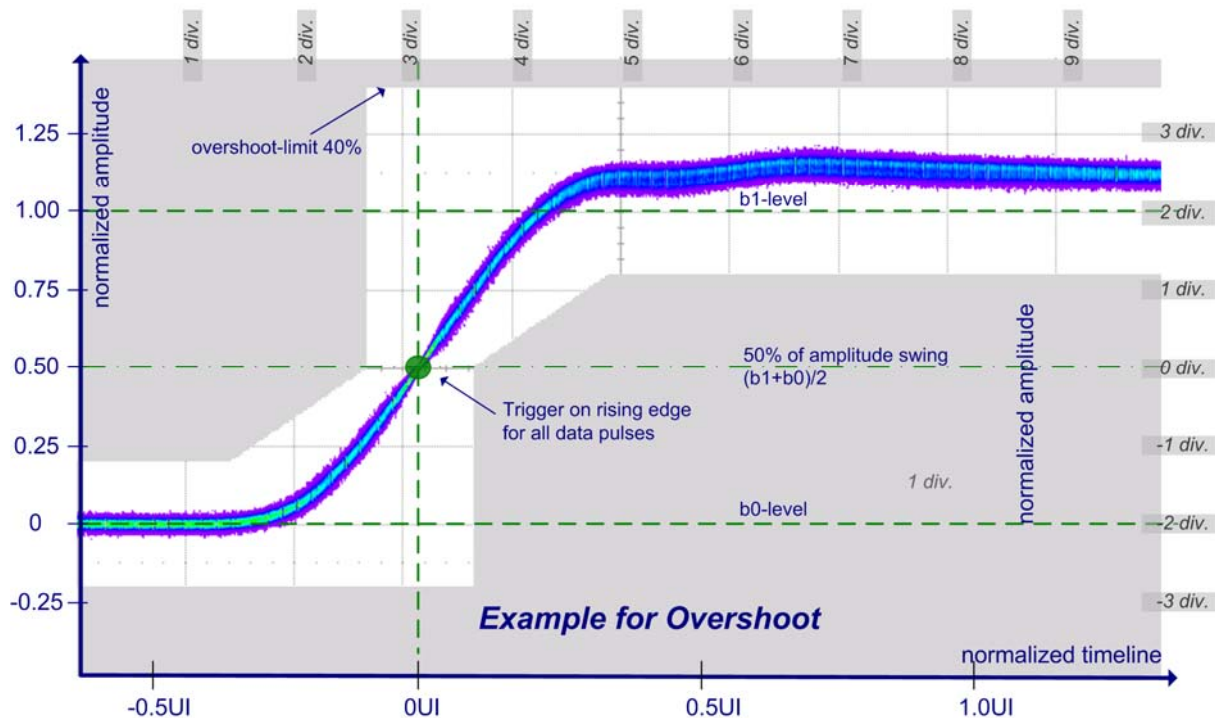


Figure 3-9: Example Overshoot

For Undershoot measurement, masks for each pulse width need to be generated (2, 3, 4, 5, 6 UI). Between the overshoot region and the falling edge there is a gate ($\pm 15\%$), which limits the starting point of the transition in amplitude.

Example Undershoot 2UI:

Horizontally, a timeframe of 2 UI is displayed. According to the requested timing extremes of -0.63 UI (A_U , K_U) and 1.37 UI (J_U , T_U) given in the mask-parameters, the zero-point is set to 3.15 divisions. Vertically, again the 50% level of the amplitude-swing is centered in the oscilloscope's grid; b_0 is set to -2 divisions, b_1 is set to +2 divisions.

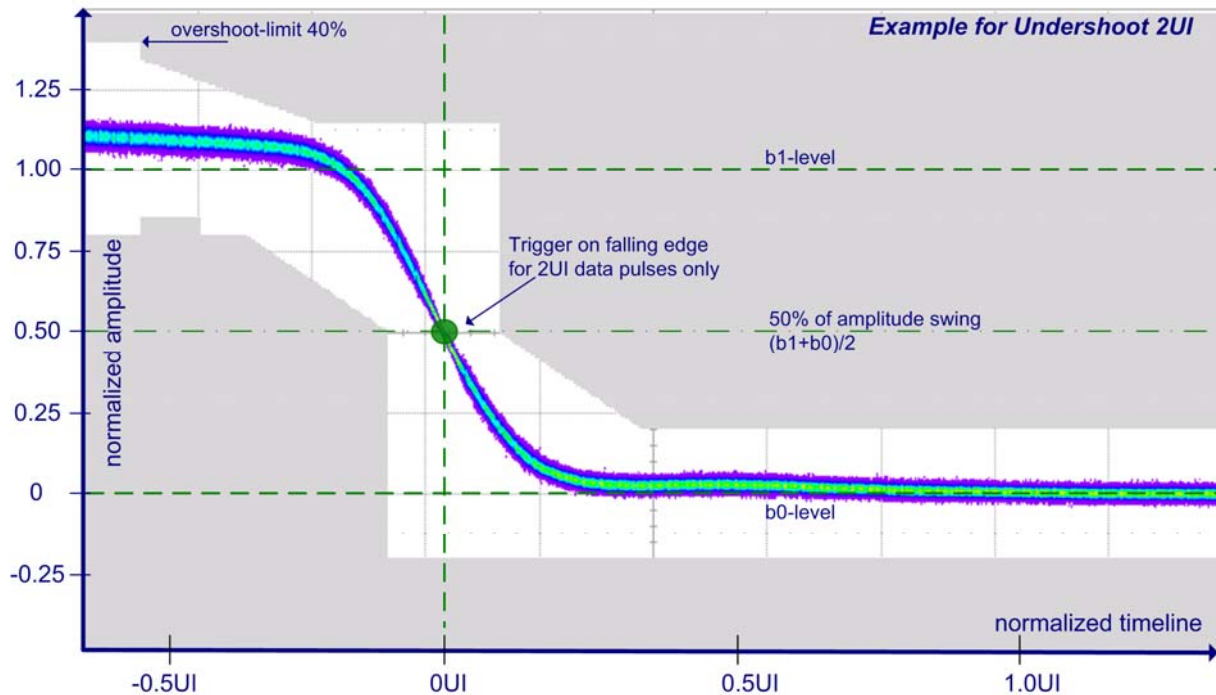


Figure 3-10: Example Undershoot 2UI

Example Undershoot 4UI:

Horizontally, 4 UIs are displayed. According to the requested timing extremes of -2.63 UI (A_U , K_U) and 1.37 UI (J_U , T_U) given in the mask parameters, the zero-point is set to 6.58 divisions.

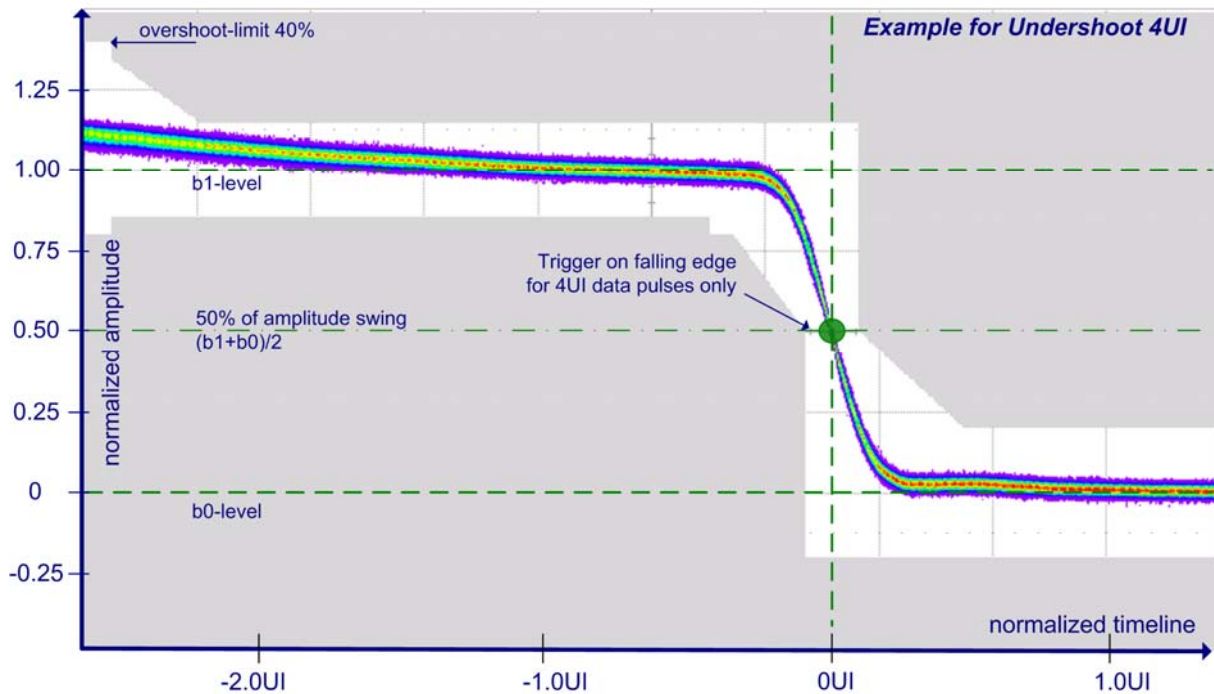


Figure 3-11: Example Undershoot 4UI

3.8 Transition times @SP2

The transition times (rise and fall) are detected as the time of an edge when transitioning through the level range of 20% and 80% of the optical amplitude (b1, b0, see section 3.5). Therefore, b0/b1 detection needs to be performed beforehand.

The amplitude threshold levels are given:

$$20\% - threshold = [(b1 - b0) * 0.2] + b0$$

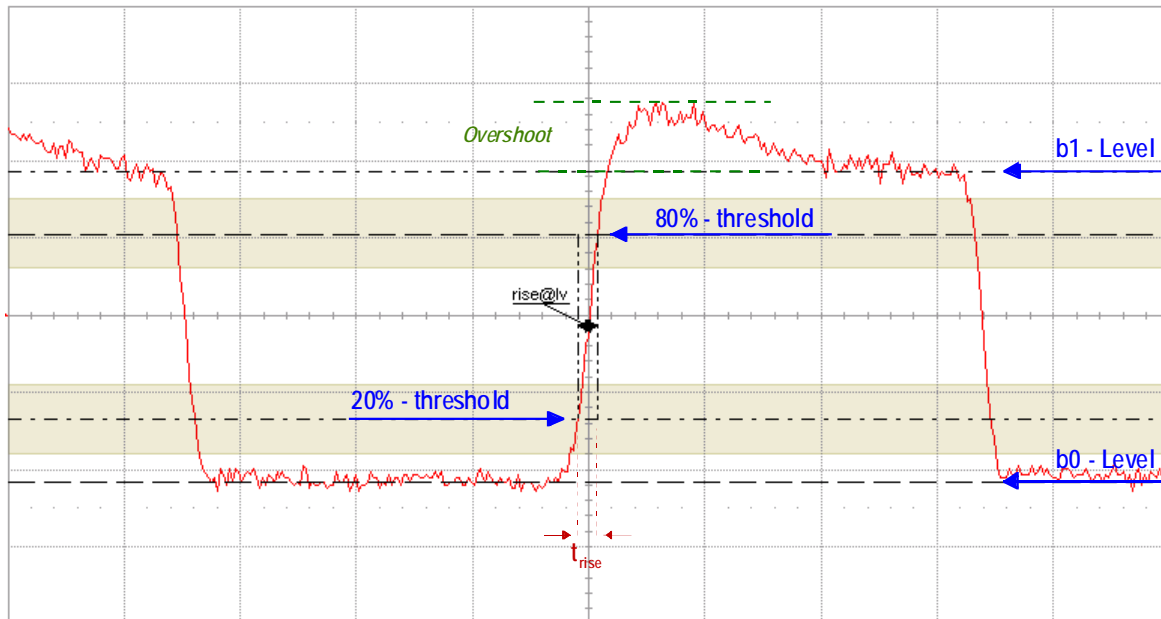
$$80\% - threshold = [(b1 - b0) * 0.8] + b0$$


Figure 3-12: Example for detection of rise-time

Measured transition times have to be smaller than the specified limit in [3]. It is recommended to use the MOST150 stress pattern as data signal.

3.9 Creating a Stimulus for SP3

Measuring jitter at SP4 requires reasonable stimulus signals at SP3. When creating this stimulus signal, all possible impacts coming from various sources need to be considered.

- The SP2 signal may vary within the specified limits
 - Transition times, t_r and t_f may be different
 - Pulse shape, overshoot and undershoot
 - Extinction ratio
 - Alignment Jitter, Transferred Jitter
- The transport medium POF between SP2 and SP3 may further provide a limitation in bandwidth; for long fibers (up to 15 m) the following impacts are expected:
 - Degradation of transition time
 - Inter Symbol Interference ISI
 - Duty Cycle Distortion, in case of overshoot and/or Duty Cycle Distortion on the input signal.
 - A model is given in the specification [3] which enables to approximate the impact of the bandwidth limitation on an SP2 output signal.
- In case of short fibers the bandwidth limitation is negligible, but
 - Extreme Pulse Shapes, within the specified SP2 limits have to be considered.
- A main impact comes with the attenuation due to the transport medium
 - An input power range as specified for an OEC has to be characterized.

These distortions will appear in any combination and may have influence on an OEC's jitter performance. The severity of these distortions mainly depends on the way the OEC is designed; some distortions will be easily compensated while other distortions may worsen the jitter performance directly. Therefore, it is not easily possible to define one "worst case stimulus", which includes maximum stress for all types of OECs. Even for particular OEC designs, there might be several aspects to be investigated using specific stimuli. Therefore, it is in the responsibility of the FOT supplier to create the worst case stimuli for their particular OEC design.

Later in this document, test setups are defined for acquiring SP4 jitter, which contribute to simplification. Low input power at SP3 is assumed to be caused by longer fibers and is therefore combined with worst case POF bandwidth limitation. For high input power, a short link is assumed and the POF bandwidth limitation aspect is excluded from the measurement.

4 Measurement of Phase Variation

4.1 Basics

Measurement of Phase Variation

Phase Variation describes data stream noise and distortion in the time domain. Based on spectral content of the variation, Sub-categories of Phase Variation are defined.

Phase Variation	Spectral limits
Wander	DC up to 10 Hz
Transferred Jitter (T_j)	Jitter with 10 Hz up the limit given by the Jitter Filter
Alignment Jitter (A_j)	Jitter with spectral content above the limit given by the Golden PLL

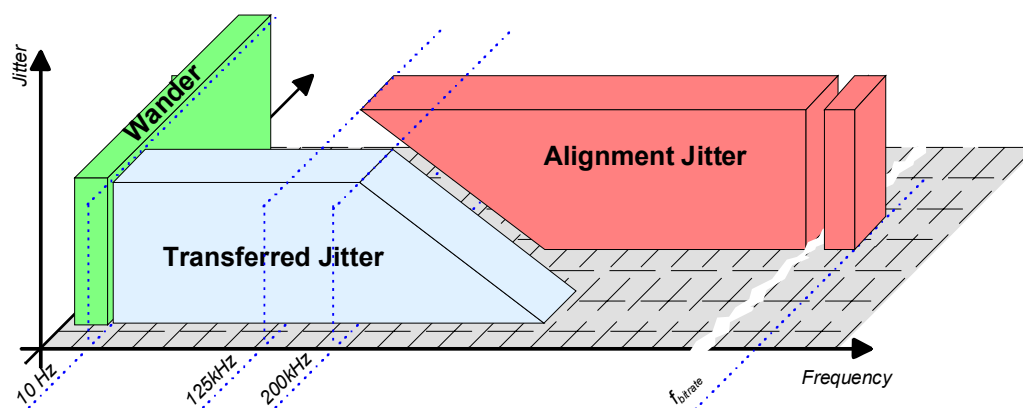


Figure 4-1: Sub-categories of Phase Variation

The need for separating T_j and A_j is founded in the synchronous approach of the MOST network. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node will recover the clock for sampling the input data out of the received data stream. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain correlation in phase between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). The PLL enables the capability of tracking of Phase variations. Phase variation in a lower spectral range on an incoming data stream will be compensated by aligning the clock's phase accordingly. Therefore, low frequency jitter will not impact the data recovery. However, the clock for generating the output data, which is derived from the recovered input clock, will be affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter cannot be tracked by the PLL and will lead to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum Alignment Jitter A_j) to be tolerated is defined with the eye masks for each specification point.

The dynamic characteristics of a PLL for a MOST node are covered by the physical layer specification with two definitions:

“Golden PLL”:

The “Golden PLL” is a model, given in the form of a transfer function representing a low pass filter. The “Golden PLL” serves two purposes.

1. It is used as a measurement tool for generating a time base which is required for forming eye diagrams and determining A_j at each SP along a link. The golden PLL must take data in from the measured SPs and generate a UI-clock. Based on the recovered UI-clock an eye diagram is drawn. Eye masks, defined for each SP give the limits for A_j respectively.
2. The “Golden PLL” describes the behavior of a NIC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass (or higher) will be tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass may lead to misalignment. The “Golden PLL” in combination with the eye mask for SP4 receiver tolerance describes the minimum A_j tolerance of a NIC’s receive section.

“Jitter Filter”:

The Jitter Filter is a model, given in the form of a transfer function representing a low pass filter. It serves two purposes.

1. It is used as a measurement tool for extracting Transferred Jitter (T_j) out of the total jitter.
2. Additionally, it describes the worst case jitter transfer characteristic over a NIC. Jitter below the spectral range described by the low-pass may be tracked by a PLL. The data stream being generated by this NIC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

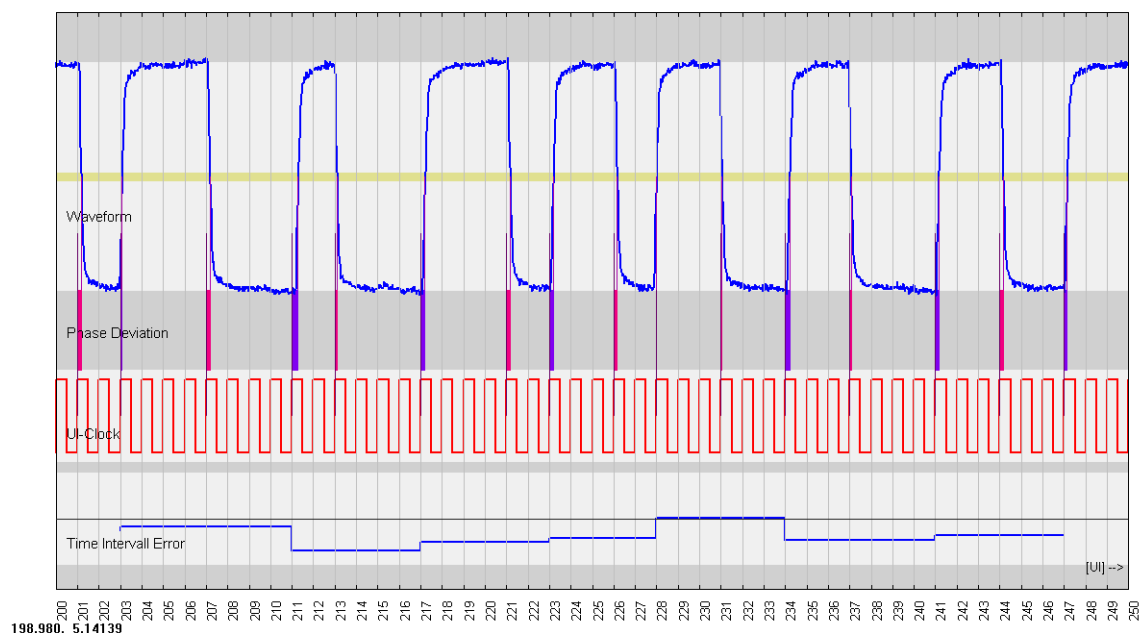
4.2 Measuring Alignment Jitter

The following table describes a procedure for detecting A_j out of a measured data stream. Oscilloscopes appropriate for the jitter measurements are Digital Sampling Oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	<p>A probe (electrical or optical probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data steam ("waveform") is sampled into the scope's memory.</p> <p>For electrical interfaces SP1 and SP4 masks are defined in absolute amplitude. The SP2 mask is given in a relative scheme, which requires a normalization of the waveform or an adaption of the mask to the particular amplitude (see section 3.5 and 3.7).</p>
Clock recovery	<p>The DCA-coded MOST150 data stream contains clock and data. In a first step the clock must be extracted.</p> <p>Data-pulses range from 2 UI to 6 UI yielding 5 different pulse widths (2, 3, 4, 5, 6 UI). The required clock has a cycle-time of 1 UI, which is twice the bit rate (i.e., for F_s 48 kHz, the bit rate is 147.45 Mbit/s, the UI-clock is 294.91 MHz).</p> <p>A method of extracting the UI-clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST150 specifies that the "Golden PLL" is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p>

Example:

- UI-clock is fitted in frequency and phase to the waveform
- remaining phase deviations are marked in the diagram
- phase deviations for rising edges are shown in the "Timing-Interval Error" graph

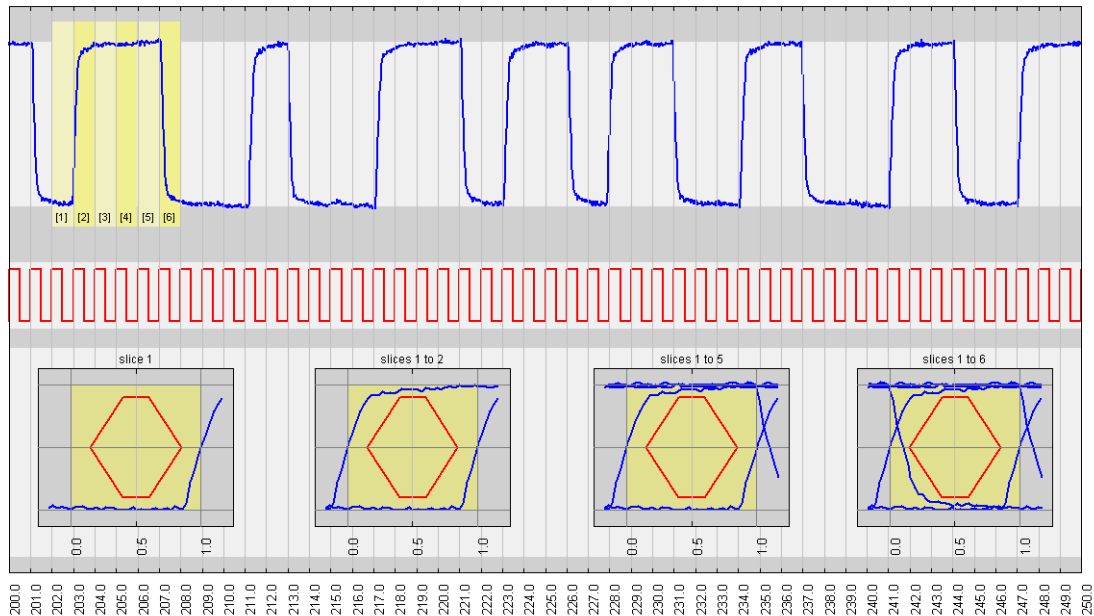


Note: In many oscilloscopes, visualization of the recovered UI-clock is not possible.

Applying Low Pass filter given by "Golden PLL"	<p>Once a first derivate of the UI-clock is approximated, there may still be phase differences between rising data-edges and the recovered UI-clock, called "Time Interval Errors". Applying the low-pass filter (given by the "Golden PLL" model) to the sequence of consecutive "Time Interval Errors" results in a filtered phase-deviation sequence. This sequence represents the minimum capability of the NIC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI-clock need to be compensated by the sequence of filtered Phase-deviations.</p> <p>The resulting new UI-clock, which is used for further calculations, now represents the base UI-clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. However, modulation capability is limited in spectrum given by the "golden PLL" model.</p>
Calculating Alignment Jitter	<p>Alignment Jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI-clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over run-time in a graph result in an "A_J-Track" which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an "A_J-Jitter-Histogram".</p>
Forming the Eye	<p>For drawing the eye diagram, the waveform is sliced in intervals of 1 UI length aligned with the UI-clock. The sliced waveform segments plus some overhead (i.e., 0.25 UI on both sides) are overlaid in one graph.</p> <p>Notes:</p> <ul style="list-style-type: none"> • <i>As shown in the diagram below, each transition is drawn twice, one time on the left side and secondly on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram.</i> • <i>Duty cycle distortion DCD, if it exists, will shift the eye towards the mask. In the shown example, LOW pulses are shorter than HIGH pulses. The UI-clock is referenced to rising edges which causes the rising edges to be adjusted to the UI-borders, while the falling edges are shifted by the amount of the DCD.</i>

Example:

- slice-sections are marked in the waveform graph
- sliced waveform segments are overlaid in a single diagram
- temporary results are shown



Pass/Fail-Test using Eye masks	<p>Signal integrity is checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error.</p> <p>The masks are defined by hexagons with points A, B, C, D, E and F. Points A and D are limiting A_J while B, C, E, F build constraints for amplitude and pulse-shape.</p>
Bit Error Rate	<p>The requested BER of 10^{-9} requires an eye diagram showing at least 10^9 bits without violation of the mask!</p> <p>1 Bit = 2 UI → at least $2 \cdot 10^9$ hits are required</p> <p>Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is in the responsibility of the user.</p>

Table 4-1: Measuring Alignment Jitter

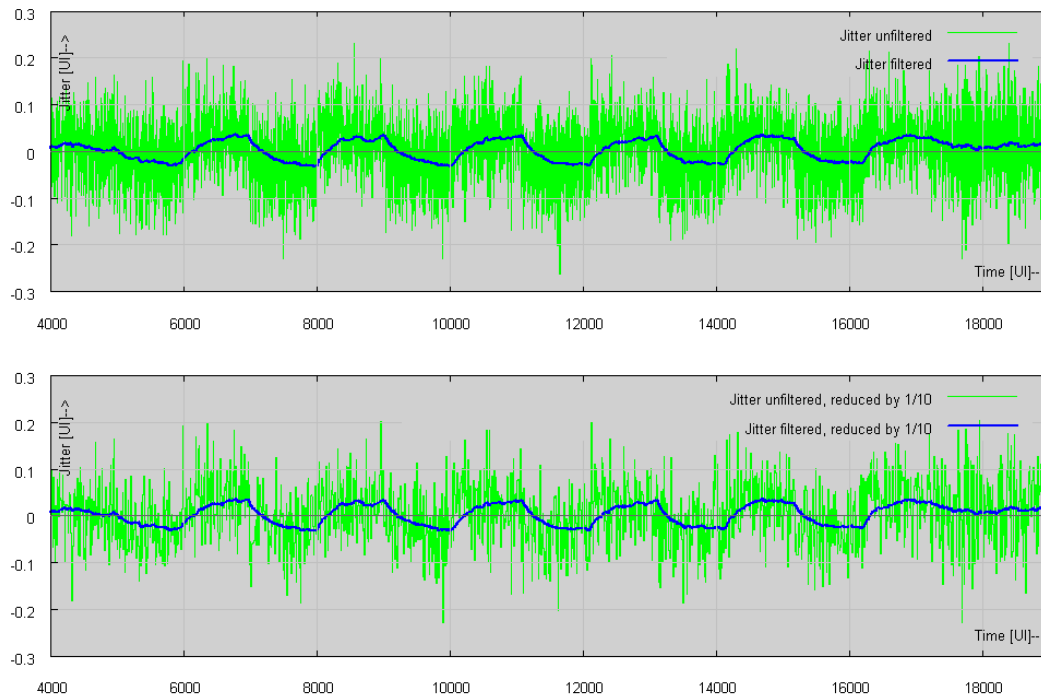
4.3 Measuring Transferred Jitter

The following table describes a procedure how to detect T_j out of a measured data stream. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	<p>For this measurement, the maximum available sampling memory of the oscilloscope has to be used. A probe (electrical or optical probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution (see b1/b0 detection, scaling channel/mask). A sequence of the data stream ("waveform") is sampled into the scope's memory.</p> <p>T_j is defined in the spectrum from 10 Hz (beyond Wander) and 200 kHz. The resolution of an oscilloscope low frequency jitter is limited by the size of memory.</p> <p>Note: <i>Even Oscilloscopes with very deep memory will hardly achieve 10 Hz resolution.</i></p>
Clock recovery	<p>Similar to the A_j Measurement procedure, the clock must be extracted. Clock separation is provided by an oscilloscope internal function.</p> <p>Similar to the A_j Measurement procedure, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency, the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p> <p>In contrast to the A_j Measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. However, smallest deviations in the detected bit-rate may grow up to a significant phase mismatch over the length of the acquired waveform and therefore affect further results. To enable a robust measurement procedure it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz).</p>
Extracting Transferred Jitter	<p>Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI-clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant, because only these deviations are tracked by the PLL and impact the recovered clock's phase.</p> <p>Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over run-time in a graph result in a "Jitter-Track".</p> <p>Successive phase deviations appear in pulse time intervals (2, 3, 4, 5, 6 UI), which correspond to the theoretical maximum jitter frequencies up to 150 MHz. With respect to the focused spectral range 10 Hz to 200 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process.</p> <p>In the next step, this "Jitter Track" (optionally reduced) needs to be low-passed, using the transfer function given with the "Jitter Filter" definition, which results in the "Filtered Jitter".</p>

Example:

- First graph: successive phase deviations are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")
- Second graph: successive phase deviations but reduced by factor 10 are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")



Calculating Transferred Jitter

Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using root-mean-square method RMS.

$$RMS = \sqrt{\frac{1}{N} \sum_{i=1}^N v_i^2}$$

In case filtered jitter contains a DC-component or Wander (i.e., caused by a constant phase mismatch between clock and data), it is tolerable to calculate the Standard Deviation instead of RMS.

Note: This option is only applicable if the spectral content of eliminated jitter component, expressed by the mean-value, is below 10 Hz.

$$StdDev = \sqrt{\frac{1}{N} \sum_{i=1}^N (v_i - mean)^2}$$

Table 4-2: Measuring Transferred Jitter

4.4 Test Setups

4.4.1 Relevant Eye Mask for Components and Modules

Link Quality describes the minimum Alignment Jitter performance of components and modules along a single link. Receiver tolerance describes the minimum Alignment Jitter tolerance of a NIC and the maximum tolerable alignment jitter that may occur in any place in the network. Therefore components and modules have to comply with Alignment Jitter Limits given in Link Quality tables for SP1 to SP4.

4.4.2 SP4 Jitter Measurement (A_j & T_j)

There are various impacts that determine the characteristic of an input signal @ SP3 to be considered for jitter measurements @ SP4. Besides the pulse shape and timing distortion of an SP2-output signal, especially the attenuation of that signal along the optical link is relevant. The jitter performance of an "OEC-under-test" needs to be checked over the complete sensitivity range.

Also, in combination with fiber length, the impact of fiber bandwidth shall be considered. Therefore, two setups, representing extreme impact of fiber bandwidth, are recommended for jitter measurements @ SP4: A first setup for low input power and a second one for high input power @SP3.

Low input power indicates a link using a long fiber (up to 15 meters) with several inline couplers. In addition to the low input power, the impact due to the bandwidth limitations of the POF needs to be considered. The setup uses a light source followed by a mode mixer (according to JIS 6863 [9]). The mode mixer ensures a numerical aperture of $NA=0.5$ (EMD-condition) independent of the characteristic of the light source. Signal degradation due to bandwidth limitation of the fiber is implemented by practically using 15 m of POF, which is the maximum specified fiber length.

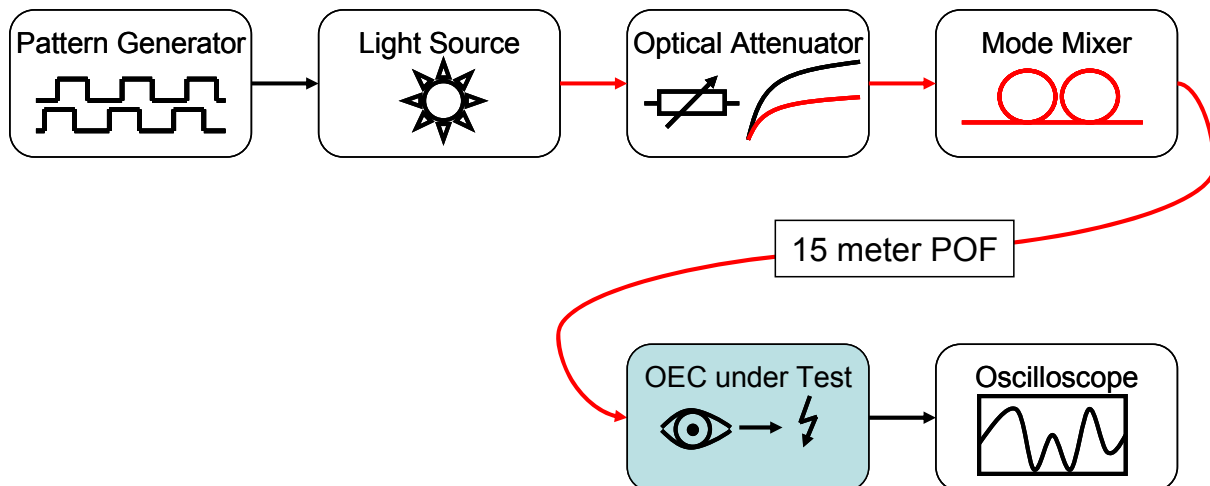


Figure 4-2: SP4 Jitter Measurement Setup with long optical link

Note: The bandwidth limitation due to POF given in the MOST specification was calculated for NA 0.5 in uniform distribution. However, the mode mixer in the shown setup creates an equilibrium distribution, which results in a lower impact on signal characteristics.

SP4 Jitter measurement, Setup for low input power at SP3		
Input power range	Min. sensitivity limit (-22 dBm) of the OEC up to at least -20 dBm	
Pattern-Generator	Providing MOST stress pattern Capability for generating dynamic jitter within jitter extremes for SP2 (in combination with the "Light Source" – jitter may be generated by the Pattern Generator or by the light source)	
Light source "high BW"	Pulse Shape representing a "high bandwidth emitter"	
	Transition time t_r, t_f	< 1.00 ns
	Overshoot	> 1.25 of Normalized Amplitude
	Extinction Ratio	10 to 12 dB
Light source "low BW"	Pulse Shape representing a "low bandwidth emitter"	
	Transition time t_r, t_f	between 1.00 ns and 0.5 UI
	Overshoot	No overshoot
	Extinction Ratio	10 to 12 dB
Attenuation-Tool	Preferably attenuation via gray filter, not via air gap	
Mode-Mixer	According to JIS 6863 [9]	
Fiber	15 m POF	
OEC under test	Variation of VCC, considering operating temperature range	

Table 4-3: SP4 Jitter measurement, Setup for low input power at SP3

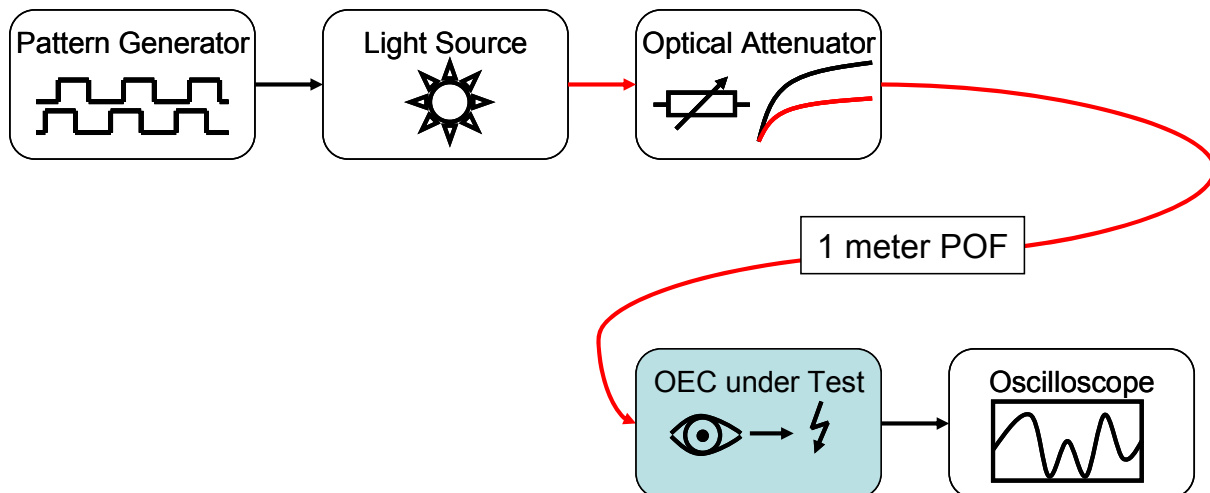


Figure 4-3: SP4 Jitter Measurement Setup with short optical link

High input power indicates a link using a short fiber without inline couplers. The impact due to bandwidth limitations of POF is negligible. The setup uses a light source, which shall provide fast transition times and overshoot, followed by short piece of fiber.

SP4 Jitter measurement, Setup for high input power at SP3		
Input power range	Max. sensitivity limit (-2 dBm) of the OEC down to at least -6dBm	
Pattern-Generator	Providing MOST stress pattern Capability for generating dynamic jitter within jitter extremes for SP2 (in combination with the "Light Source" – jitter may be generated by the Pattern Generator or by the light source)	
Light source "high BW"	Pulse Shape representing a "high bandwidth emitter"	
	Transition time t_r, t_f	< 1.00 ns
	Overshoot	> 1.25 of Normalized Amplitude
	Extinction Ratio	10 to 12 dB
Attenuation-Tool	Preferably attenuation via gray filter, not via air gap	
Fiber	1 m POF	
OEC under test	Variation of VCC, considering operating temperature range	

Table 4-4: SP4 Jitter Measurement, Setup for high input power at SP3

4.4.3 SP2 Jitter Measurement (A_j & T_j)

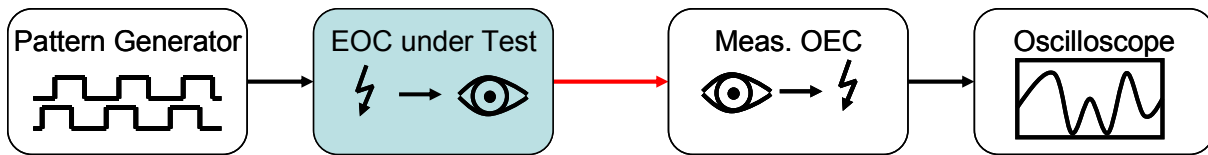


Figure 4-4: SP2 Jitter Measurement Setup

SP2 Jitter measurement	
Pattern-Generator	Providing MOST stress pattern Capability for generating dynamic jitter within jitter extremes for SP1
EOC under test	Variation of VCC, considering operating temperature range
Measurement OEC	Bandwidth according to section 1.3, High-speed OEC

Table 4-5: SP2 Jitter Measurement

4.5 Crosstalk

In serial digital communication systems, electromagnetic and/or optical crosstalk can cause a reduction in receiver sensitivity. This section outlines a way to determine and quantify the crosstalk induced penalty with measurement equipment used for MOST oPhy measurements. The crosstalk measurement is based on the setup for the receiver's jitter performance vs. optical input power. Crosstalk is expected to be generated by the transmitter which is placed close to the receiver. The test shall be used for SMD transceivers as well as for connector assemblies combining THM transmitters and THM receivers into transceiver modules. The crosstalk penalty is determined by comparison of the jitter performance of the receiver with the transmit section of the transceiver (TX) ON vs. OFF.

Measurement Setup:

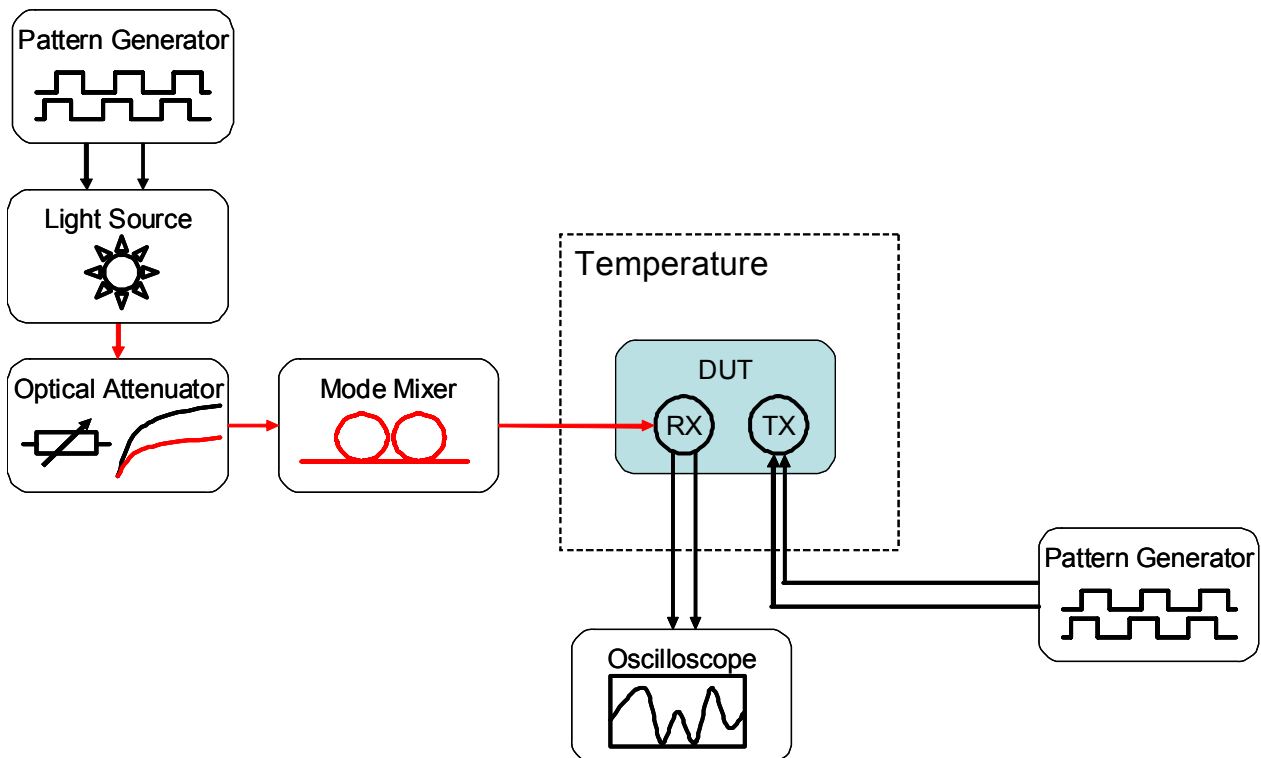


Figure 4-5: Crosstalk measurement setup

There is no crosstalk immunity limit defined in the MOST physical layer specification; however, all requests for A_j and T_j have to consider this stress level. Therefore, a products datasheet (SMD transceiver or THM module) has to consider the potential crosstalk impact. The following procedure shows a method for quantifying the crosstalk penalty, if it exists.

Procedure:

- Two pattern sources are required. Both sources deliver square-wave-signals (equivalent 2 UI) with slightly different frequency for creating uncorrelated phase relationship between both signals. The difference in frequency will shift the phase of the TX-pattern relative to phase of the receiver pattern. A potential source of distortion (e.g. an edge of the TX-pattern) will hit the receiver at any phase.
- The evaluation is based on detection of random jitter. Due to the single frequency pattern there is no data dependent jitter expected, other deterministic jitter sources (application related) need to be eliminated for this test. Jitter can be measured as an RMS-figure or visualized by histograms or eye diagrams.
- The test is performed at the low sensitivity level of the receiver, with variation of VCC and temperature. For simplification, a single scenario creating the absolute worst case is sufficient.
- A jitter measurement is performed first without TX-activity and then with TX activated. In case of a visible impact, the input power may be increased to reach the identical jitter level. The difference in power gives the relevant information.

5 Power Up / Power Down

5.1 Basics

The chapter defines several possible test setups and sequences needed to exercise as many functional EOC and OEC requirements as possible and also provides guidelines for the interpretation of results.

All test sequences must be performed for the minimum, typical, and maximum of Operating Supply Voltage according to Operating Conditions given in section 1.2.

All test sequences must be performed for the minimum, typical, and maximum temperature specification.

When testing Modules (EOC and OEC in one case) crosstalk effects should be considered: when testing the one – the other must be active!

Some of the parameters defined by the Power Up / Power Down chapter of the Physical Layer Sub-specification could be measured directly (t_{STATF} , t_{LVDSV4} , etc.), others however (t_{ON2} , t_{OFF2} , t_{ON4} , etc.) define relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured directly this chapter defines test sequences including a timeout, which represents the maximal (resp. minimal) time interval allowed for the respective parameter. The end of this is marked in the signal charts (e.g., Figure 5-2) as Action Point (Δ) and appoints the time for a state validity evaluation.

E.g., $t_{ON2(max)}$ time after the Reset signal goes HIGH start evaluating SP2 signal quality to check compliance to the requirements for “Valid Most Data”.

Measuring Electrical parameters such as LVTTTL or LVDS compliance is beyond the scope of this document and will not be discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

5.2 Measuring EOC Parameters

5.2.1 Measuring EOC Parameters – Test Setup

The diagram below outlines how a setup for measurement of the EOC performance could look like.

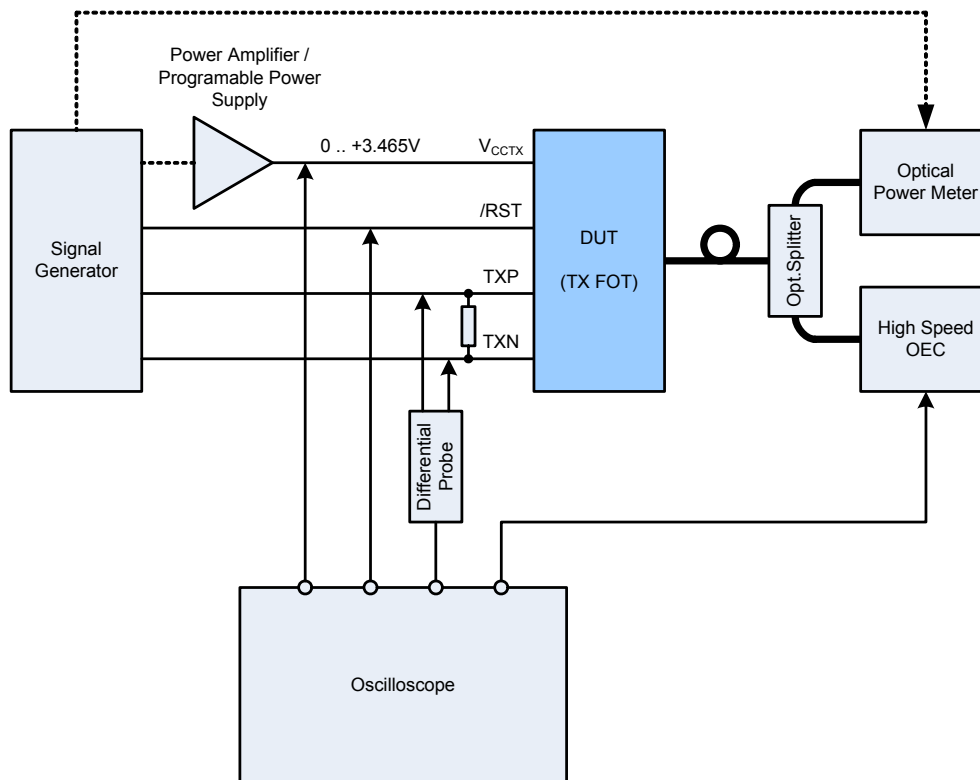


Figure 5-1: Setup for Measuring EOC ON/OFF Parameters

The main parts of the setup are:

- **DUT:** The DUT (Device Under Test) is fitted according to the manufacturer's recommended setup.
- **Signal Generator:** used to produce the stimuli (Test Patterns), produce the trigger signal for the optical power meter and control the EOC Power Supply.
- **Optical splitter:** with well defined split ratio. Alternatively the test can be performed in two stages (OFF-ON test and ON-OFF test), where the Optical Power Meter can be connected directly to the DUT for the first stage, respectively the High Speed OEC for the second. In this case optical splitter is not needed.
- **Optical Power Meter:** to measure the average optical power output of the DUT. Peak Hold functionality is beneficial.
- **High Speed OEC:** to convert the optical signal to electrical.
- **Oscilloscope:** to capture input and output signals data. Note: SP1 signal is differential signal: the usage of active high-speed differential probe is recommended
- **Power Amplifier/ Programmable power supply:** to turn the EOC power supply on and off and to provide the desired supply voltage.

5.2.2 Measuring EOC Parameters – Signal Charts

The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the pre-requisites for the corresponding tests the EOC parameters.

The EOC parameter testing requires two different types of test sequences:

- In the first sequence ON/OFF behavior is controlled by signal content of SP1 while /RST is LVTTTL High (Figure 5-2).
- In the second sequence On/OFF behavior is controlled by /RST signal (Figure 5-3).

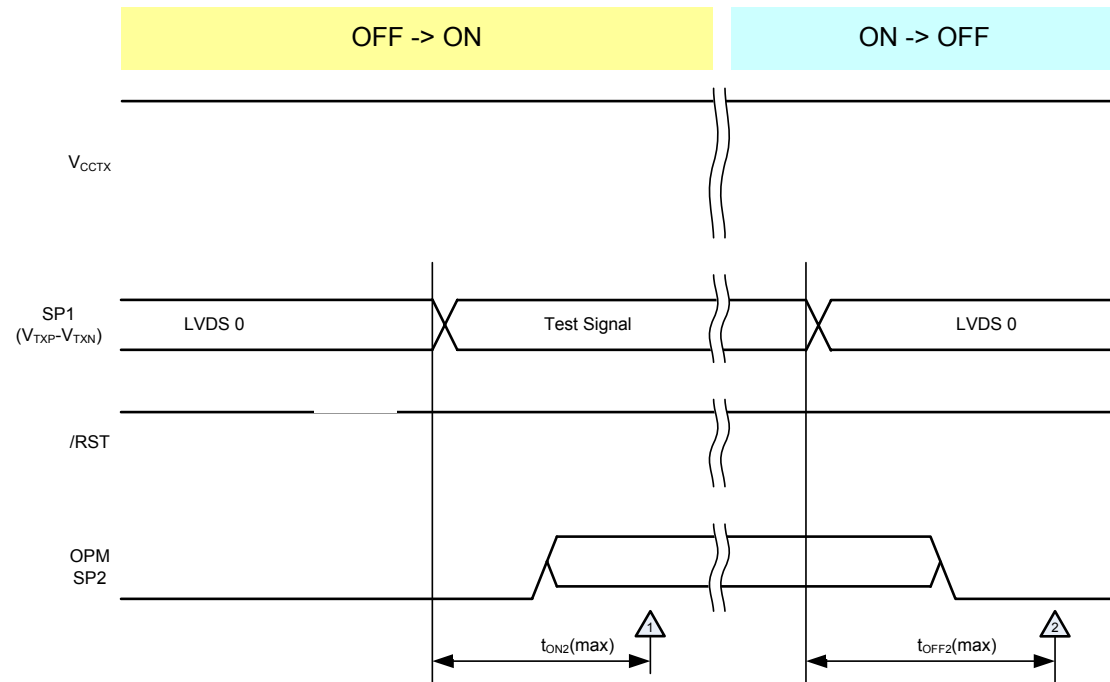


Figure 5-2: Measuring EOC Parameters: EOC Signal Chart No. 1

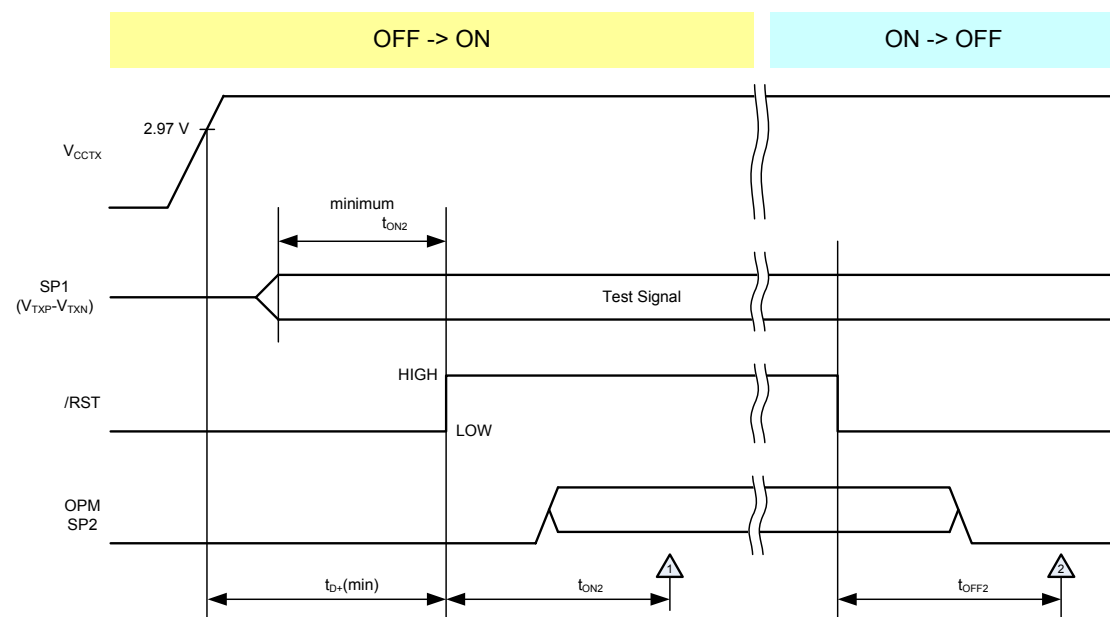


Figure 5-3: Measuring EOC Parameters: EOC Signal Chart No. 2

5.2.3 Measuring EOC Parameters – Test sequences

5.2.3.1 EOC Test Sequence #1 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 5-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	LVDS "0"
Initial State: Output	SP2 (Optical)	Average output power below $P_{OFF2}(\max)$
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	EOC shall remain in OFF state with no average output power on SP2 above $P_{OFF2}(\max)$ at any time	

Table 5-1: EOC Test Sequence #1

This test sequence exercises the transition detection mechanism of the EOC. It is required that the EOC must remain in OFF state being supplied with input signal with frequency within F_{OFF1} requirements.

An Optical Power Meter must monitor the SP2 output before, during, and after the test to ensure the OFF state requirement $P_{opt2} < P_{OFF2}(\max)$ is met.

5.2.3.2 EOC Test Sequence #2 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 5-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Initial State: Output	SP2 (Optical)	Average output power below $P_{OFF2}(\max)$
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	12 MHz square wave pattern, LVDS compliant
Output / Expected behavior	EOC shall transition to ON state within time $t_{ON2}(\max)$	

Table 5-2: EOC Test Sequence #2

This test sequence exercises the transition detection mechanism of the EOC. It is required that the EOC must perform transition detection at its input and remain in or transition to ON state being supplied with signal with frequency within F_{ON1} requirements. In this particular test the $F_{ON1}(\min)$ compliance is checked.

Another requirement being checked is the maximal allowed duration for the transition from OFF to ON state. The MOST150 oPhy Automotive Physical Layer Sub-Specification [3] states that the EOC must be in ON state not later than $t_{ON2}(\max)$ time after all ON conditions are met. In this case it is the time of the first rising edge of the Test Stimulus.

Since there is no directly measurable marker to notify the EOC entering ON state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{ON2}(\max)$ – marked as Action Point 1 in the EOC Signal Chart Figure 5-2) a check of ON state requirements is started.

For this test, since the input is no MOST data, only the optical power output of the SP2 interface is checked.

5.2.3.3 EOC Test Sequence #3 - ON-to-OFF by SP1 Signal

Signal Chart	Figure 5-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	12 MHz LVDS compliant square wave
Initial State: Output	SP2 (Optical)	Average output power within P_{opt2}
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	EOC shall transition to OFF state within time $t_{OFF2}(max)$	

Table 5-3: EOC Test Sequence #3

This test sequence exercises the transition detection mechanism of the EOC. It is required that the EOC must transition to OFF state being supplied with signal with frequency within F_{OFF1} requirements.

Another requirement being checked is the maximal allowed duration for the transition from ON to OFF state. The MOST150 oPhy Automotive Physical Layer Sub-Specification [3] states that the EOC must be in OFF state not later than $t_{OFF2}(max)$ time after one or more OFF conditions are met. In this case, it is the time of the last falling edge of the 12 MHz square wave signal.

Since there is no directly measurable marker to notify the EOC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{OFF2}(max)$ – marked as Action Point 2 in the EOC Signal Chart Figure 5-2), a check of OFF state requirements is started.

The Optical Power Meter must start monitoring the SP2 output after the time marked as Action Point 2 to ensure the OFF state requirement $P_{opt2} < P_{OFF2}(max)$ is met.

To trigger the start of the optical power measurement the signal generator could assert trigger signal to the optical power meter $t_{OFF2}(max)$ after switching the test signal to LVDS "0", e.g., to initiate measurement of the optical power. Peak-hold function of the optical power meter will ensure short light blips are not "averaged" away.

5.2.3.4 EOC Test Sequence #4 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 5-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Initial State: Output	SP2 (Optical)	Average output power below $P_{OFF2}(\max)$
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	LVDS compliant Stress Pattern with nominal bit rate (BR)
Output / Expected behavior	EOC shall transition to ON state within time $t_{ON2}(\max)$	

Table 5-4: EOC Test Sequence #4

This test sequence exercises the transition detection mechanism of the EOC. It is required that the EOC must perform transition detection at its input and remain in or transition to ON state being supplied with signal with frequency within F_{ON1} requirements. In this particular test, the $F_{ON1}(\min)$ compliance is checked.

Another requirement being checked is the maximal allowed duration for the transition from OFF to ON state. The MOST150 oPhy Automotive Physical Layer Sub-Specification [3] states that the EOC must be in ON state not later than $t_{ON2}(\max)$ time after all ON conditions are met. In this case, it is the time of the first rising edge of the Test Stimulus.

Since there is no directly measurable marker to notify the EOC entering ON state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{ON2}(\max)$ – marked as Action Point 1 in the EOC Signal Chart Figure 5-2) a check of ON state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality must be checked. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP2 signal quality. To assist the capture of the SP2 data in ON state, the signal generator could assert trigger signal to the oscilloscope $t_{ON2}(\max)$ after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 100 μs .

5.2.3.5 EOC Test Sequence #5 - ON-to-OFF by SP1 Signal

Signal Chart	Figure 5-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2 (Optical)	Average output power within P_{opt2}
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	LVDS “0”, DC to 10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	EOC shall transition to OFF state within time $t_{OFF2}(max)$	

Table 5-5: EOC Test Sequence #5

This test sequence exercises the transition detection mechanism of the EOC. It is required that the EOC must transition to OFF state being supplied with signal with frequency within F_{OFF1} requirements.

Another requirement being checked is the maximal allowed duration for the transition from ON to OFF state. The MOST150 oPhy Automotive Physical Layer Sub-Specification [3] states that the EOC must be in OFF state not later than $t_{OFF2}(max)$ time after one or more OFF conditions are met. In this case it is the time of the last falling edge of the 12 MHz square wave signal.

Since there is no directly measurable marker to notify the EOC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{OFF2}(max)$ – marked as Action Point 2 in the EOC Signal Chart Figure 5-2) a check of OFF state requirements is started.

The Optical Power Meter must start monitoring the SP2 output after the time marked as Action Point 2 to ensure the OFF state requirement $P_{opt2} < P_{OFF2}(max)$ is met.

To trigger the start of the optical power measurement the signal generator could assert trigger signal to the optical power meter $t_{OFF2}(max)$ after switching the test signal to LVDS0, e.g., to initiate measurement of the optical power. Peak-hold function of the optical power meter will ensure short light blips are not “averaged” away.

5.2.3.6 EOC Test Sequence #6 - OFF-to-ON by /RST Signal

Signal Chart	Figure 5-3	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL Low
	SP1 (V _{TXP} -V _{TXN})	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2 (Optical)	Average output power below P _{OFF2} (max)
Test Signal: Inputs	/RST	LVTTL High
Output / Expected behavior	EOC shall transition to ON state within time t _{ON2} (max)	

Table 5-6: EOC Test Sequence #6

This test sequence exercises the reset mechanism of the EOC. It is required that the EOC must transition to ON state within a time t_{ON2}(max) after the /RST signal has been driven low (and SP1 signal within F_{ON1}).

Another requirement being checked is the minimal allowed time for the /RST to be driven high after the power supply crosses the V_T(min) voltage. There are two aspects for treating this parameter:

The first is the power supply application aspect; the reset generator providing the signal must be designed to ensure the /RST signal does not transition to LVTTL High before t_{D+}(min) time has passed since the VCCTX measured on the EOC power supply pins crossed V_T.

The second is the EOC parameter aspect; the MOST150 oPhy Automotive Physical Layer Sub-Specification [3] states that when being supplied with an operating voltage within V_{CCTXGR}, the internal circuitry of the EOC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+}. By driving the reset signal High at the t_{D+}(min) time it is checked if the EOC complies to that specification.

Since there is no directly measurable marker to notify the EOC entering ON state event, an indirect method is used for testing the t_{ON2}(max) compliance: After the maximal allowed time has passed (end of t_{ON2}(max) – marked as Action Point 1 in the EOC Signal Chart Figure 5-3) a check of ON state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality must be checked. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP2 signal quality.

5.2.3.7 EOC Test Sequence #7 - ON-to-OFF by /RST Signal

Signal Chart	Figure 5-3	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2 (Optical)	Average output power within P _{opt2}
Test Signal: Inputs	/RST	LVTTL Low
Output / Expected behavior	EOC shall transition to OFF state within time t _{OFF2} (max)	

Table 5-7: EOC Test Sequence #7

This test sequence exercises the reset mechanism of the EOC. It is required that the EOC must transition to OFF state within a time t_{OFF2}(max) after the /RST signal has been driven low and it must stay in OFF state (with P_{opt2} < P_{OFF2}(max)) as long as /RST is driven low.

Since there is no directly measurable marker to notify the EOC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of t_{OFF2}(max) – marked as Action Point 2 in the EOC Signal Chart Figure 5-3) a check of OFF state requirements is started.

The Optical Power Meter must start monitoring the SP2 output after the time marked as Action Point 2 to ensure the OFF state requirement P_{opt2} < P_{OFF2}(max) is met. A trigger signal from the signal generator may be used to activate the Optical Power Meter.

5.3 Measuring OEC Parameters

5.3.1 Measuring OEC Parameters – Test Setup

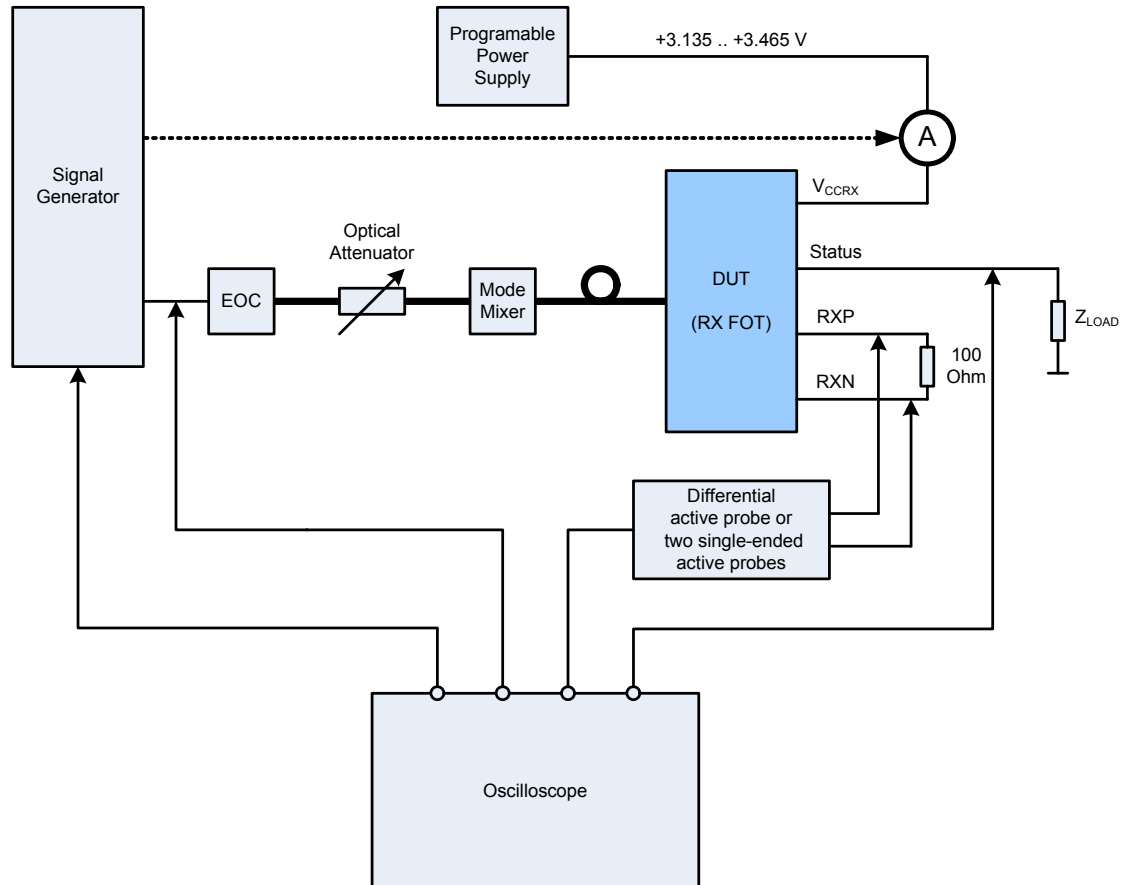


Figure 5-4: Setup for Measuring OEC ON/OFF Parameters

Physical Layer Specification defines a set of functional requirements and performance parameters that OEC has to meet. The above diagram outlines how a setup for measurement of the performance of OEC could look like.

The main parts of the setup are:

- DUT: The DUT (Device Under Test) is fitted according to the manufacturer's recommended setup and is powered constantly during the test(s).
- Signal Generator: used to produce the test patterns and produce trigger signal for the oscilloscope.
- EOC/Optical Attenuator/Mode Mixer: to convert the electrical signal to optical and shape it to the requirements of the specification.
Note: If applicable, the stimulus is performed according to the setups given in Table 4-3 and Table 4-4. For power ranges outside the operating range any light source can be used.
- Oscilloscope: to capture input and output signals data.
Note: SP4 signal is differential signal; the usage of an active high-speed differential probe is recommended.
- (Micro-)Ampere meter: to measure the current consumption of the OEC device (in OFF state).

5.3.2 Measuring OEC Parameters – Signal Charts

The signal chart represents the graphical view of test sequence. It shows the location of the action points and provides the pre-requisites for the corresponding tests of the OEC parameters.

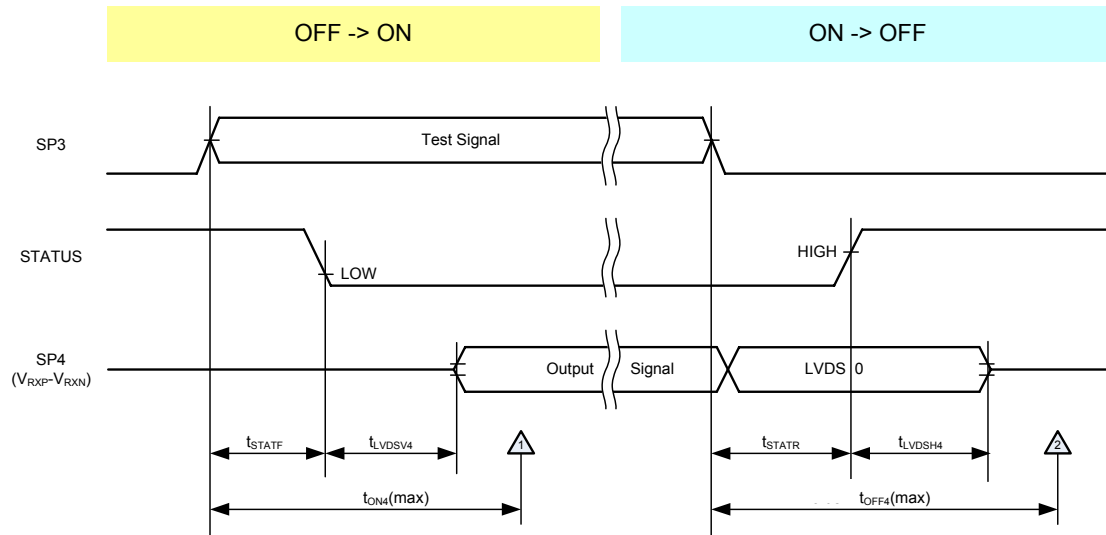


Figure 5-5: Measuring OEC Parameters: OEC Signal Chart No. 1

5.3.3 Measuring OEC Parameters – Test sequences

5.3.3.1 OEC Test Sequence #1 - OFF-to-ON

Signal Chart	Figure 5-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3 (Optical)	P _{opt3} (avg) < P _{OFF3} (max)
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{RXN})	Disabled
Test Signal: Inputs	SP3 (Optical)	Continuous 10 kHz Square Wave P _{opt3} (avg) = -22 ... -2 dBm
Output / Expected behavior	OEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that I _{CCR_X} > I _{CCSLEEP} (MAX)	

Table 5-8: OEC Test Sequence #1

This test sequence exercises the transition detection and wakeup mechanism of the OEC. It is required that the OEC must remain in OFF state being supplied with input signal with frequency within F_{OFF3} requirements (assuming all other ON state requirements are met).

The OEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, I_{CCSLEEP}. During the Test Signal application the OEC is allowed to consume more than I_{CCSLEEP}.

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing with Test Signals with multiple optical power levels, but at minimum the minimal and maximal values must be tested.

5.3.3.2 OEC Test Sequence #2 - OFF-to-ON

Signal Chart	Figure 5-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3 (Optical)	P _{OPT3} (avg) < -50 dBm
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{R_{XN}})	Disabled
Test Signal: Inputs	SP3 (Optical)	Continuous 12 MHz Square Wave P_{opt3} (avg) = -35 dBm
Output / Expected behavior	OEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that I _{CCR_X} > I _{CCSLEEP} (MAX)	

Table 5-9: OEC Test Sequence #2

This test sequence exercises the transition detection and wakeup mechanism of the OEC. It is required that the OEC must remain in OFF state being supplied with input signal with average optical power of less than P_{OFF3}(max) (assuming all other ON state requirements are met).

The OEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, I_{CCSLEEP}. During the Test Signal application the OEC is allowed to consume more than I_{CCSLEEP}.

For power ranges outside the operating range, any light source can be used.

5.3.3.3 OEC Test Sequence #3 - OFF-to-ON

Signal Chart	Figure 5-5	
Initial State: Inputs	$V_{CCR\bar{X}}$	According to operating conditions
	SP3 (Optical)	$P_{opt3} \text{ (avg)} < -50 \text{ dBm}$
Initial State: Outputs	STATUS	LVTTL High
	SP4 ($V_{RXP}-V_{RXN}$)	Disabled
Test Signal: Inputs	SP3 (Optical)	12 MHz Square Wave burst with duration $\leq t_{STATF}(\text{min})$ $P_{opt3} \text{ (avg)} = -22 \dots -2 \text{ dBm}$
Output / Expected behavior	OEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that $I_{CCR\bar{X}} > I_{CCSLEEP}(\text{MAX})$	

Table 5-10: OEC Test Sequence #3

This test sequence exercises the transition detection and wakeup mechanism of the OEC. It is required that, when all ON state requirements are met, the OEC must still remain in OFF state for at least $t_{STATF}(\text{min})$ time.

The OEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, $I_{CCSLEEP}$. During the Test Signal application the OEC is allowed to consume more than $I_{CCSLEEP}$.

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing with Test Signals with multiple optical power levels, but at minimum the minimal and maximal values must be tested.

5.3.3.4 OEC Test Sequence #4 - OFF-to-ON

Signal Chart	Figure 5-5	
Initial State: Inputs	V _{CCRX}	According to operating conditions
	SP3 (Optical)	P _{opt3} (avg) < - 50 dBm
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{RXN})	Disabled
Test Signal: Inputs	SP3 (Optical)	12 MHz Square Wave burst with duration > t_{STATF}(min) P_{opt3} (avg) = -22 ... -2 dBm
Output / Expected behavior	OEC shall transition to ON state within time t _{ON4} (max) with: STATUS = LVTTL Low within t _{STATF} (min) to t _{STATF} (max), and valid LVDS levels within t _{LVDSV4} (max)	

Table 5-11: OEC Test Sequence #4

This test sequence exercises the transition detection and wakeup mechanism of the OEC. It is required that, when all ON state requirements are met, the OEC must transition to ON state not earlier than t_{STATF}(min) time, but also not later than t_{ON4}(max).

Another requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.
- SP4 signal Timing: the SP4 signal muss be LVDS compliant not later than t_{LVDSV4}(max) after the STATUS is at LVTTL Low. This could be achieved with an oscilloscope, triggered off the STATUS signal falling edge, capturing the RXP and RXN signals. Only the data after t_{LVDSV4}(max) needs to be evaluated, so a trigger delay needs to be used or removal of the corresponding amount of measurement data needs to be applied.

For this test, since the input signal is no MOST data, only the STATUS signal timing and SP4 LVDS compliance need to be checked.

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing with Test Signals with multiple optical power levels, but at minimum the minimal and maximal values must be tested.

5.3.3.5 OEC Test Sequence #5 - ON-to-OFF

Signal Chart	Figure 5-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3 (Optical)	Continuous 12 MHz Square Wave P_{opt3} (avg) = -2 ... -22 dBm
Initial State: Outputs	STATUS	LVTTL Low
	SP4 (V _{RXP} -V _{R_{XN}})	LVDS Compliant Signal
Test Signal: Inputs	SP3 (Optical)	P_{opt3} (avg) < -35 dBm
Output / Expected behavior	OEC shall transition to OFF state with STATUS = LVTTL High within t _{STATR} (max) and SP4 outputs disabled within t _{OFF4} (max), but not earlier than t _{LVDSH4} (min) after STATUS transitions High. After t _{OFF4} (max) time the current consumption shall be I _{CCR_X} < I _{CCSLEEP} (max)	

Table 5-12: OEC Test Sequence #5

This test sequence exercises the transition detection and shutdown mechanism of the OEC. It is required that the OEC must transition to OFF state being supplied with signal with optical power level within P_{OFF3} requirements (assuming all other ON state requirements are met).

Another requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- SP4 signal Timing:
 - o The SP4 signal must transition to LVDS "0" within t_{STATR}(max) time after application of the Test Signal.
 - o The SP4 signal must maintain LVDS "0" for at least t_{LVDSH4}(min) after STATUS signal transitions to LVTTL High
 - o The SP4 outputs disabled within t_{OFF4}(max) time after application of the Test Signal.
- OEC power supply: t_{OFF4}(max) time after the application of the Test Signal, the OEC power consumption should be less than I_{CCSLEEP}(max).

To trigger the start of the electrical current measurement, the signal generator could assert trigger signal to the ampere meter t_{OFF4}(max) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing from Initial States with multiple SP3 optical power levels, but at minimum the minimal and maximal values must be tested.

5.3.3.6 OEC Test Sequence #6 - OFF-to-ON

Signal Chart	Figure 5-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3 (Optical)	Stress Pattern with nominal bit rate (BR) P _{opt3} (avg) < - 35 dBm
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{R_{XN}})	Disabled
Test Signal: Inputs	SP3 (Optical)	P _{opt3} (avg) = -2 ... -22 dBm
Output / Expected behavior	OEC shall transition to ON state within time t _{ON4} (max) with: STATUS = LVTTL Low within t _{STATF} (min) to t _{STATF} (max), and valid LVDS levels within t _{LVDSV4} (max)	

Table 5-13: OEC Test Sequence #6

This test sequence exercises the transition detection and wakeup mechanism of the OEC. It is required that the OEC must perform transition detection at its input and remain in or transition to ON state, being supplied with signal with average optical power within P_{ON3} and frequency within F_{ON3} requirements. In this particular test the P_{ON3} compliance is checked.

Other requirements being checked are:

- STATUS signal timing – time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.
- SP4 signal Timing – The SP4 signal must be LVDS compliant not later than t_{LVDSV4}(max) after the STATUS is at LVTTL Low. This could be achieved with an oscilloscope, triggered off the STATUS signal falling edge, capturing the SP4 signals single-ended. Only the data after t_{LVDSV4}(max) needs to be evaluated for, so a trigger delay needs to be used or removal of the corresponding amount of measurement data needs to be applied.

Since there is no directly measurable marker to notify the OEC entering compliant ON state, an indirect method is used for the t_{ON4}(max) parameter evaluation: After the maximal allowed time has passed (end of t_{ON4}(max) – marked as Action Point 1 in the Signal Chart Figure 5-5) a check of ON state requirements is started.

For this test, along with STATUS at LVTTL Low requirement check, also the SP4 signal quality must be evaluated. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP4 signal quality. To assist the capture of the SP4 data, the signal generator could assert trigger signal to the oscilloscope t_{ON4}(max) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 10 ms.

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing with Test Signals with multiple optical power levels, but at minimum the minimal and maximal values must be tested.

5.3.3.7 OEC Test Sequence #7 - ON-to-OFF

Signal Charts	Figure 5-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3 (Optical)	Stress Pattern with nominal bit rate (BR) P _{opt3} (avg) = -2 ... -22 dBm
Initial State: Outputs	STATUS	LVTTL Low
	SP4 (V _{RXP} -V _{R_{XN}})	LVDS Compliant Valid MOST Data
Test Signal: Inputs	SP3 (Optical)	P _{opt3} (avg) < - 35 dBm
Output / Expected behavior	<p>OEC shall transition to OFF state with STATUS = LVTTL High within t_{STATR}(max) and SP4 outputs disabled within t_{OFF4}(max), but not earlier than t_{LVDSH4}(min) after STATUS transitions High. After t_{OFF4}(max) time the current consumption shall be I_{CCR_X} < I_{CCSLEEP}(MAX)</p>	

Table 5-14: OEC Test Sequence #7

This test sequence exercises the transition detection and shutdown mechanism of the OEC. It is required that the OEC must transition to OFF state being supplied with signal with optical power level within P_{OFF3} requirements (assuming all other ON state requirements are met).

Other requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- SP4 signal Timing:
 - o The SP4 signal must transition to LVDS "0" within t_{STATR}(max) time after application of the Test Signal.
 - o The SP4 signal must maintain LVDS "0" for at least t_{LVDSH4}(min) after STATUS signal transitions to LVTTL High
 - o The SP4 outputs disabled within t_{OFF4}(max) time after application of the Test Signal.
- OEC power supply: t_{OFF4}(max) time after the application of the Test Signal the OEC power consumption should be less than I_{CCSLEEP}(max).

To trigger the start of the electrical current measurement the signal generator could assert trigger signal to the ampere meter t_{OFF4}(max) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The stimulus is performed according to the setups given in Table 4-3 and Table 4-4.

It is recommended testing from Initial States with multiple SP3 optical power levels, but at minimum the minimal and maximal values must be tested.

6 Detecting Bit rate (Frequency Reference)

The bit rate is detected as follows:

- Take MOST150 stress pattern.
- Set the DUT to act as master via FBlock EnhancedTestability, function PhysicalLayerTest (FktID 0x218).
- Take 10 MSamples @ 10 GSamples/s data using Golden PLL.
- Calculate bit rate.

7 System Performance

The system-level specifications apply to an entire MOST network.

7.1 SP4 Receiver Tolerance

Unlike the link-level tests which use a pattern generator as the signal source, the system-level tests use live data from a fully formed MOST150 ring. Using the same eye diagram methodologies developed in chapter 4, a measurement is taken at SP4 of the TimingMaster node. By taking the measurement in this way, one can quantify the total jitter accumulation around the ring. This measurement is applicable for every node in the network at SP4.

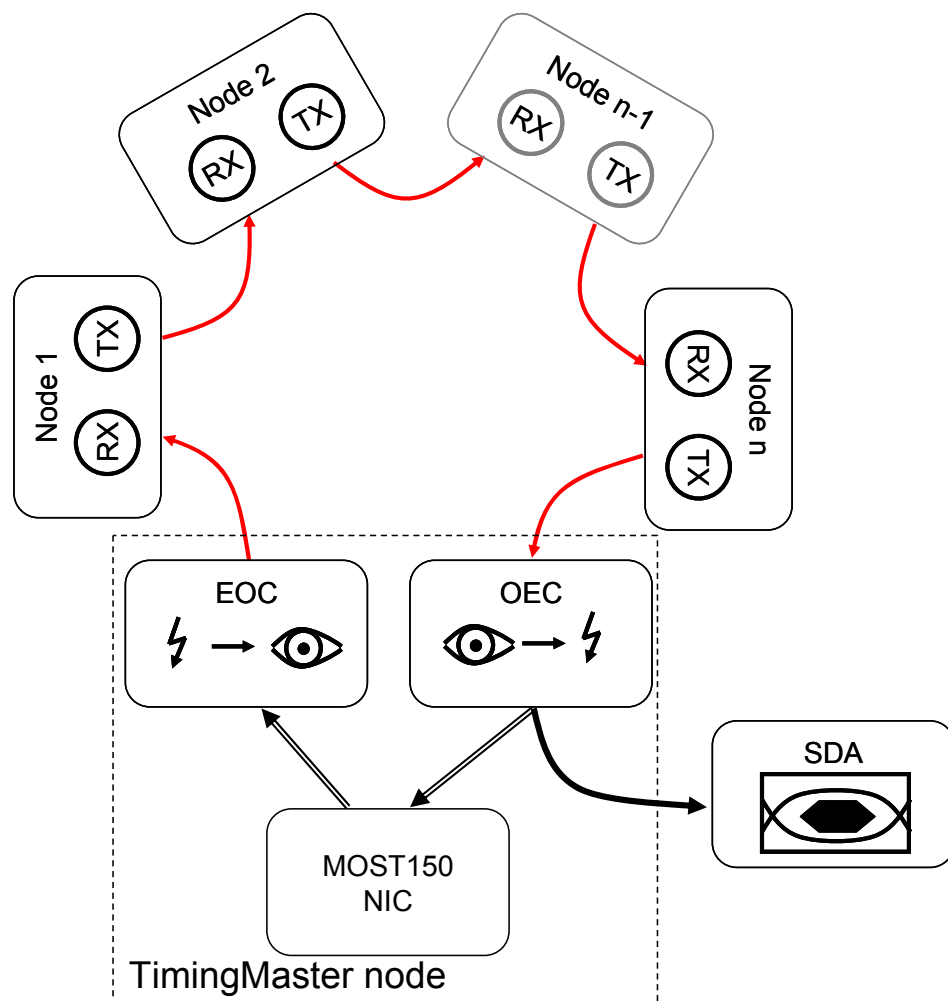


Figure 7-1: SP4 Receiver Tolerance Setup

7.2 Master Delay Tolerance

Master Delay Tolerance is a measure of end-to-end delay and phase variation between SP1 and SP4 of the TimingMaster device. To ensure proper network operation, the total network delay must not exceed the specified maximum.

Following the setup diagram shown in Figure 7-2, the total delay can be measured on an oscilloscope.

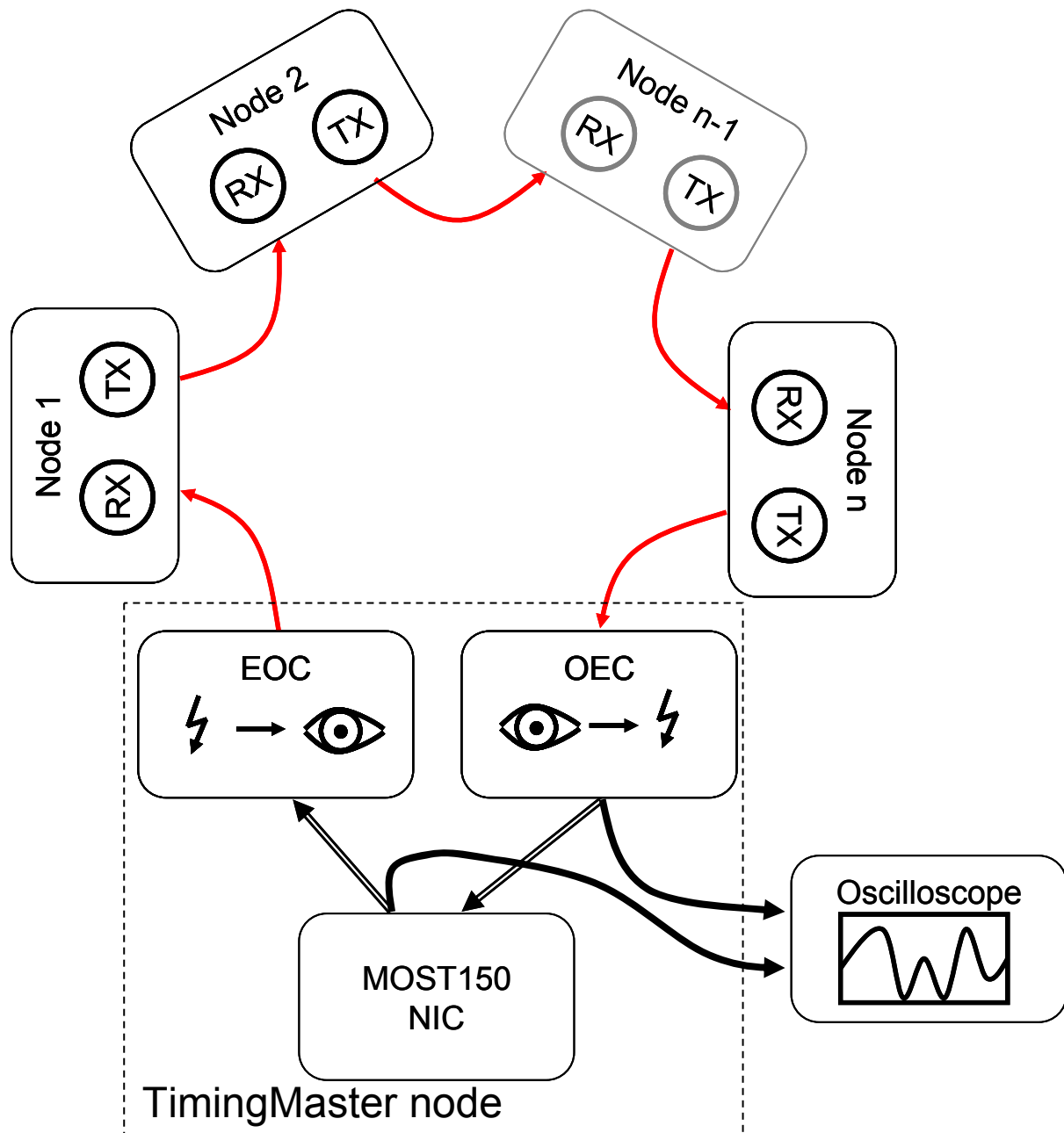
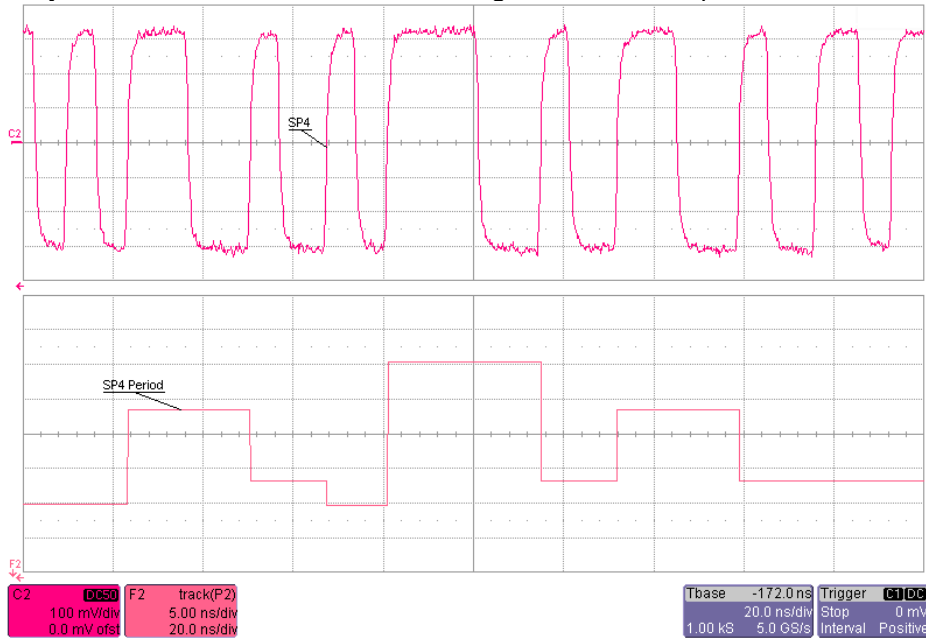
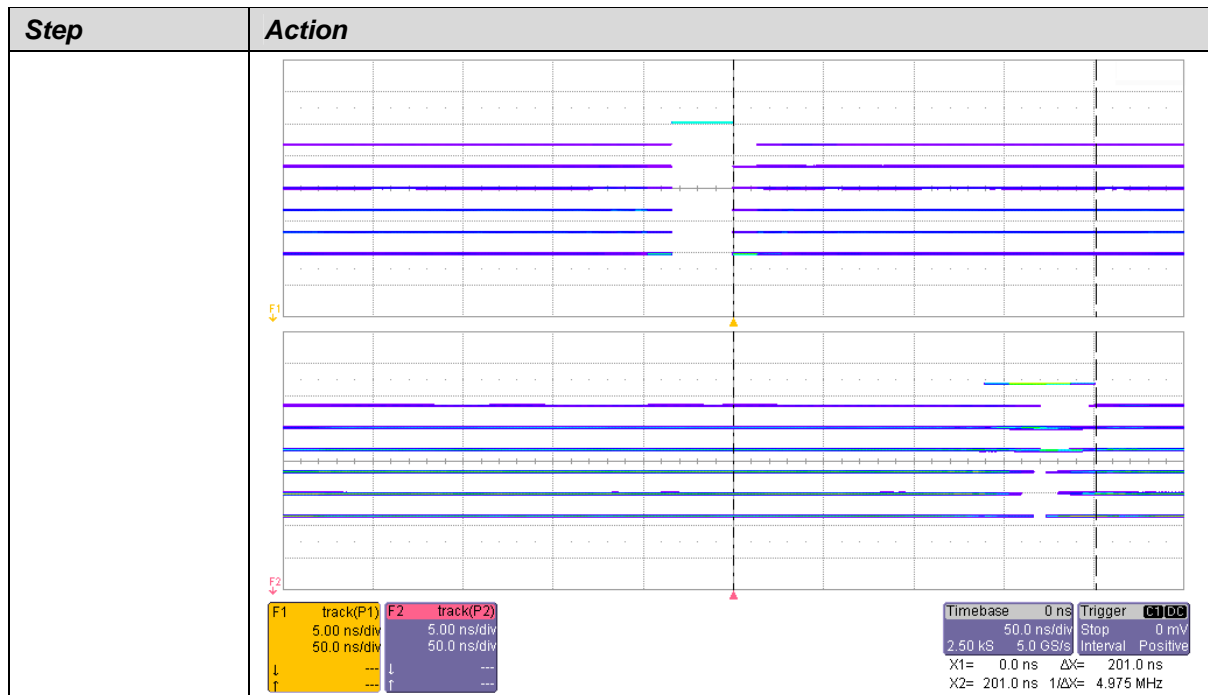


Figure 7-2: Master Delay Tolerance Setup

The following table describes the procedure used to measure the total delay. The oscilloscope used must be able to trigger on a specified period and have software functions for tracking periods. Two high-speed differential probes are required.

Step	Action
Acquiring a waveform	<p>For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP1 of the TimingMaster node. A second differential probe is connected to SP4 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels.</p> <p>The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP1. The interval should be set to $10 \text{ UI} \pm 0.5 \text{ UI}$. The <i>Trigger Mode</i> should be Normal.</p> <p>A sequence of the data stream ("waveform") is sampled into the scope's memory.</p>
Measure period	<p>The MOST150 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay between any two points in the network.</p> <p>Configure the oscilloscope to measure the period of both SP1 and SP4.</p>
Track the period	<p>Configure the oscilloscope to display a "Track" waveform for both SP1 and SP4 period measurements. This should result in two waveforms with time on the y-axis where the line indicates the length of the current period.</p> 
Measure the delay	<p>Configure the oscilloscope display to show only the SP1 and SP4 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP1 and SP4.</p> <p>Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP4 10 UI period. This is the Master Delay.</p>



Appendix A: Measuring optical signals at SP2 using Averaging

Measurement of timing and pulse shape parameters on SP2 signals might be challenging. Noise caused by the high-speed measurement-OECs may overlay with the measured signal and therefore degrade the results. Generation of Noise directly depends on the sensitivity of the particular measurement-OEC and the applied input power. The lower the input power, the higher the noise.

In case the noise source is unambiguously the measurement-OEC and not the EOC under test, noise may be reduced within the measurement process by Averaging. Averaging means: Acquiring multiple waveforms and calculating the statistical mean of amplitude values along the time axis.

Requirements for Averaging:

- A repetitive test-pattern (e.g., MOST Stress-pattern)
- A precise trigger-signal, generated once per pattern

Waveforms are triggered using the precise trigger-signal. The acquired waveforms represent identical pattern-sequences. Data dependencies in timing and pulse shape are caused by the composition of pattern elements; therefore, the acquired waveforms will contain these data dependent effects identically. All non-pattern related impacts (uncorrelated noise sources) will add variations to pulse shape and timing, appearing in a random manner. Calculating the statistical mean of amplitude samples of multiple waveforms along the time axis eliminates the impact of the uncorrelated sources, while variations due to data dependencies will be kept.

When using Averaging for the evaluation of SP2-parameters, noise injected by the measurement-OEC will be attenuated. But Averaging also attenuates signal variations caused by other sources, as long as these variations are not caused by data-dependencies. (i.e., variations due to EOC-internal loops, impact due to EOC-external sources like power supply noise, crosstalk, etc.). Thus, using Averaging implies a high risk to miss details on SP2 performance in case Averaging is the general and single measurement strategy. Usage of Averaging might be helpful as a supplementary measurement procedure but should always be referenced to a non-averaged setup.

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