

MOST

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST50 bPHY Compliance Verification Procedure –
Physical Layer Rev. 1.0
06/2019**

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Contents

1	INTRODUCTION.....	6
1.1	Relevance of Compliance	6
1.2	Related Documents	6
1.3	MOST Link.....	6
1.3.1	Location of Interfaces	6
1.3.2	Control Signals	7
1.4	Limited access to specification points	7
2	PARAMETER-OVERVIEW.....	8
3	LIMITED PHYSICAL COMPLIANCE	9
3.1	Overview.....	9
3.2	Test Setup	9
3.3	Generating test signals for the DUT Input section SP3	10
3.4	Analysis of Test results	10
3.5	Test Flow Overview	11
3.6	Test of multi-node devices with two MNCs in one ECU.....	11
3.7	Test of data recovery at the DUT Receive section.....	12
3.8	Measurement of SP2 output signal of the DUT.....	13
3.9	Measurement of Return Loss	13
3.10	Functional testing of Wake-up and Shutdown	14
4	DIRECT PHYSICAL MEASURING ACCURACY.....	15
5	APPENDIX A: LIMITED PHYSICAL LAYER COMPLIANCE FOR DEVELOPMENT TOOLS.....	16
6	APPENDIX B: SP3 STRESS CONDITIONS.....	16
7	APPENDIX C: INDEX OF FIGURES.....	17
8	APPENDIX D: INDEX OF TABLES	17

Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

Document		Revision
[1]	MOST Specification	3.1
[2]	MOST Basic Physical Specification	1.0
[3]	MOST50 bPhy Automotive Physical Layer Sub-Specification	1.0
[4]	MOST Compliance Requirements	2.3
[5]	MOST50 bPhy Compliance Measurement Guideline	1.0
[6]	FBlock ExtendedNetworkControl	3.1

MOST Document references

Document History

Changes

Change Ref.	Section	Changes
1.0-00		New Issue

1 Introduction

1.1 Relevance of Compliance

Compliance in terms of physical layer means products have to fulfill all specified parameters. This includes electrical parameters and properties as well as signal timing. For verification of these parameters, suppliers of devices, modules and components have to implement suitable processes like product characterization, qualification and end-of-line-testing (considering environmental conditions, stability over lifetime, etc.) There are various industry and automotive standards defining procedures and quality requirements (e.g., ISO 9000, ISO/TS 16949, AEC Q100, AEC Q200).

The process of compliance certification is defined to check performance on a subset of the specified parameters. Therefore, the compliance certification performs only a crosscheck with focus on basic network interoperability. The compliance verification is done on device level. Compliance on chip level is covered through characterization and beyond the scope of this document.

1.2 Related Documents

The MOST Basic Physical Specification [2] in combination with the MOST50 bPHY Automotive Physical Layer Sub-Specification [3] defines all relevant parameters. The MOST50 bPHY Compliance Measurement Guideline [5] describes how to determine and measure parameters. These documents are applicable for MOST devices as well as for modules and components. The process of Compliance Verification is defined in the document MOST Compliance Requirements [4]. It describes how to achieve a compliance certification for MOST subsystems.

Terminology of naming within these documents:

MOST End Product in document [4] = Device in document [3,5]:

Any product within the bounds of scope that is offered for sale or is distributed in an unmodified form to any end user who acquires the product for such end user's personal or commercial use, alone or in combination with any other product.

1.3 MOST Link

1.3.1 Location of Interfaces

Definitions for SP2 describe parameters of an ECU's output signal. Performance criteria for SP2 include EBC and AFE impact on signal quality.

SP3 specification describes the minimum signal quality requirements at the ECU's input interface. Stimulus signal for SP3 can be composed by combination of worst case SP2-performance plus deterioration due to the channel impairment.

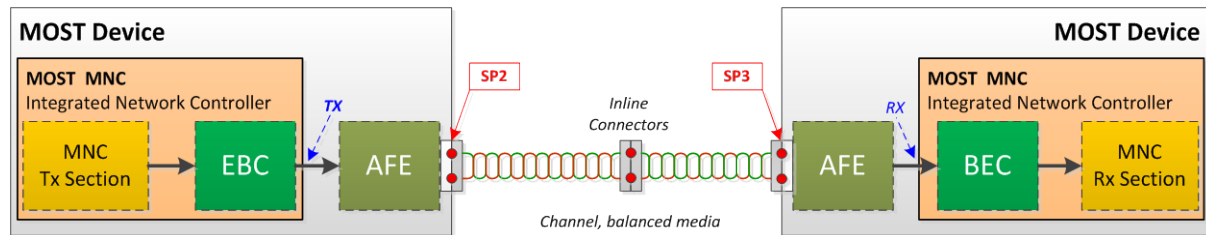


Figure 1-1: Specification Point Locations

Signals that fulfill specified parameters for SP3 can be recovered by the MNC. Signals that exceed specified ranges may cause bit errors. On SP2 of the following MNC (node n+1) a recovered signal is available according to SP2 requirements, timing distortion (except transferred jitter) is eliminated.

1.3.2 Control Signals

Activity on EBC and consequently on SP2 is mainly controlled by functions of higher layer. Beside this, there is a specific requirement for power on/off cycles, which is achieved by adding a /RST input to the EBC.

The BEC provides activity detection. Depending on the characteristics of the input signal (signal amplitude RMS, signal's spectral content) ON/OFF state is signaled by the STATUS line.



Figure 1-2: Control Signals for ON/Off Behavior

1.4 Limited access to specification points

On “device” level MCTHs do not have direct access to TX ports and RX ports at the MNC pins. The MCTH can only access the device at SP2 and SP3. Variation on input parameters can only be applied to SP3 (signal input of the device). Transmitter signal quality can only be measured at SP2. The power supply of MNC, EBC and BEC is fixed by the design of the device and cannot be varied, solely the power supply for the device can be accessed. Considering these circumstances the “limited physical layer compliance” describes a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (refer chapter 3, Limited Physical Compliance).

2 Parameter-Overview

The following table shows the parameters of the MOST50 bPHY Automotive Physical Layer Sub-Specification [3] relevant for Limited Physical Layer Compliance. Indications about the meaning of the parameters for the interfacing components, modules and device (input, output, property) and appropriate measuring methods are given in MOST50 bPHY Compliance Measurement Guideline [5].

Parameters defined in the MOST50 bPHY Automotive Physical Layer Sub-Specification [3] are mandatory parameters for component/module data sheets. The verification of these parameters is done using the procedure of the product characterization.

Table 2-1 shows the specified parameters of the MOST50 bPHY Compliance Measurement Guideline [5] relevant for Limited Physical Layer Compliance. In addition, this table indicates the test conditions which have to be applied during Limited Physical Layer Compliance.

Note: Developers of components or modules have to ensure that their products fulfill the specification under min/max conditions of their input parameters, considering environmental conditions and over lifetime.

	Parameter to be compliant	Limited Physical Layer: Device
SP2		
	RMS signal amplitude	M(TU)
	Alignment Jitter acc. to Eye Mask	M(TU)
	Transferred Jitter via RMS	M(TU)
	Return Loss of ECU-Interface	M (T _{typ.})
SP3		
	Limited Physical Layer Test of Data consistency	C(TUA)
	Return Loss of ECU-Interface	M (T _{typ.})
Procedures: - = No compliance test necessary M = Measure (T=Temperature Range, U=Voltage Range, A=Attenuation) physical measurement of parameter values is requested, for details see [5] C = Sample check (T=Temperature Range, U=Voltage Range, A=Attenuation) Check for Bit errors by using methods and indicators as defined in [6]		

Table 2-1: Compliance procedures for all parameters of specification points.

3 Limited Physical Compliance

3.1 Overview

Limited Physical Layer Compliance refers to MOST devices (refer section 1.4, Limited access to specification points).

An overview of the parameters to be tested and verified is given Table 2-1.

The following diagram shows the required test setup for limited physical layer testing comprising the following equipment:

- Tester Node
- Channel Emulation
- Splitter/Switcher
- Oscilloscope

3.2 Test Setup

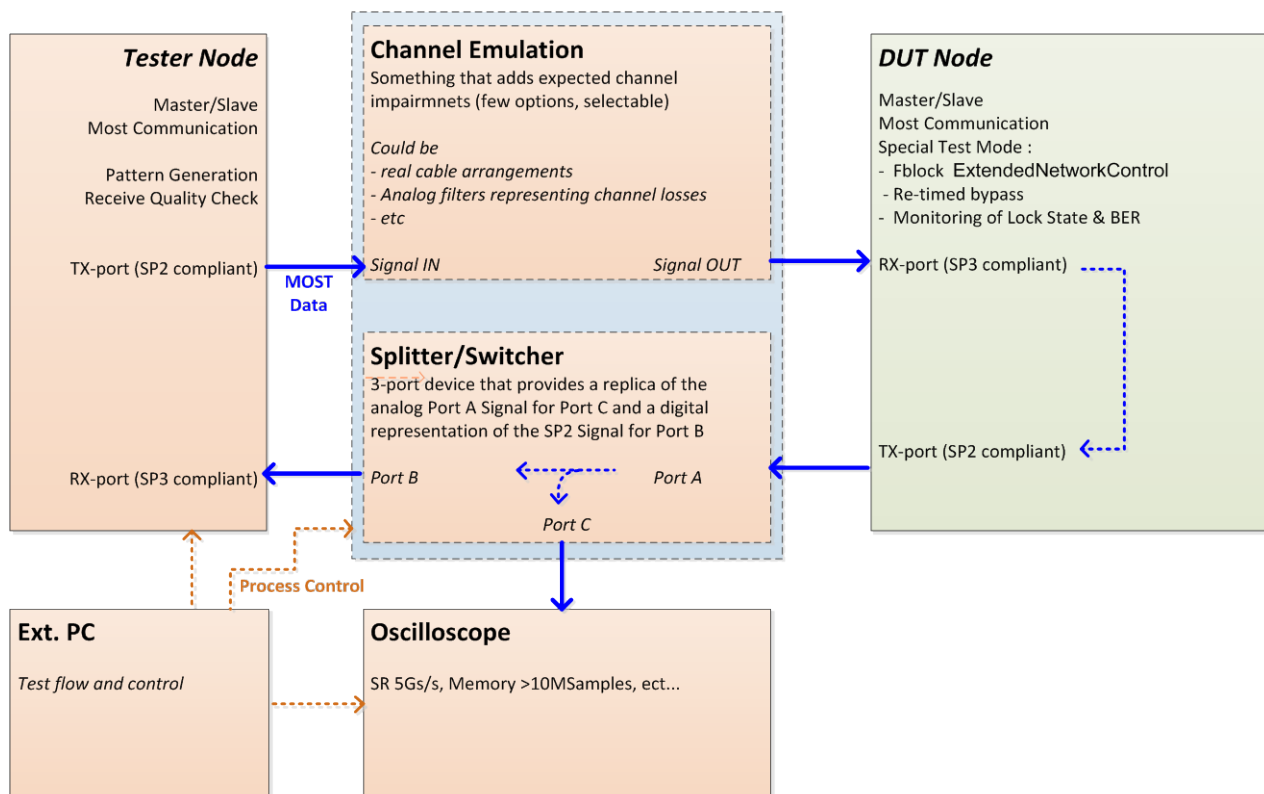


Figure 3-1: Test Setup for Limited Physical Layer Compliance test

Test goals:

- Prove of valid data transmission in presence of various stress scenarios applied to the receive path of the DUT.
- Sample check of Lock condition and Data Error state, acquired by the DUT's receive section (marked with "C" in Table 2-1)
-
- Check of Lock condition and Data Error state, acquired by the Tester Node receive section (marked with "C" in Table 2-1)
- Testing of signal integrity of DUT's signal at SP2.
Test of signal integrity includes measurement of Signal Amplitude RMS, PSD and timing (marked with M in Table 2-1). The test flow shown in section 3.5 requires a closed loop between PhLSTT and DUT, providing functional communication over MOST.
- Functional testing of wake-up and shutdown

3.3 Generating test signals for the DUT Input section SP3

A test signal for testing the DUT's input section may be varied in several instances and combinations of these instances (e. g., timing properties, pulse shape characteristics, data content and interconnect attenuation). Such variations are realized with the Tester Node and the Channel Emulation, which is a mandatory tool-set for Limited Physical Layer Test.

The Tester Node initiates and controls the whole test sequences. The Tester Node controls the DUT using communication via MOST control channel. It addresses the DUT's FBlock Extended Network Control (ENC) which covers all necessary DUT functions for the tests (e.g. "retimed bypass", handling of various error counters). The Tester Node is capable to act as Timing Master or Slave. Besides standard MOST communication, the Tester Node has the capability to send specified stress patterns.

For the test cases, specific stress pattern are combined with channel configurations (variation in link-attenuation and bandwidth limitation) and applied to the DUT's SP3 Interface.

3.4 Analysis of Test results

Error Counters are implemented in the DUT (FBlock Extended Network Control). These counters give a measure for communication errors on the input of a device. These counters are activated during the test sequence. The result can be read after the test.

During the test sequence, the DUT is set in the "retimed bypass" mode. This means that the recovered data on the input side are sampled with the internal clock and transferred to the output. Therefore, as long as there are no bit errors, the worst case stress pattern created by the Tester Node will appear with identical content on the output of the DUT.

3.5 Test Flow Overview

Figure 3-2 depicts an overview of the test flow.

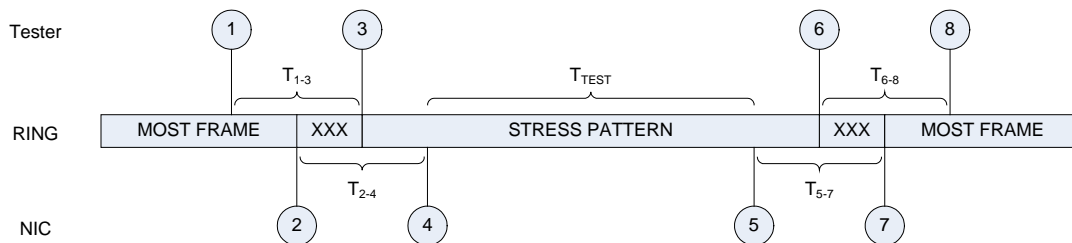


Figure 3-2: Test Flow Overview

- 1 – Tester Node sends command to DUT over MOST (FBlock Extended Network Control) to enter Test Mode.
- 2 – DUT enters Retimed Bypass Mode.
- 3 – Tester Node starts transmitting the Stress Pattern.
- 4 – DUT clears the Error Counter and Lock Log.

... PHYSICAL LAYER STRESS TESTING ...

- 5 – DUT reads back Error Counter and Lock Log.
- 6 – Tester Node switches to MOST Communication Mode.
- 7 – DUT switches back to its original MOST Mode.
- 8 – Tester Node reads back the result.

Switching times (T_{X-Y}) are in the range 10 – 500 ms with accuracy better or equal than 10 ms;

Lead-in / Lead-out: typ. 1000ms (min. 500ms; max. 2000ms).

T_{TEST} time is in the range 1 sec – 1000 sec with accuracy better or equal than 10 ms.

Duration: max. 1000 seconds.

3.6 Test of multi-node devices with two MNCs in one ECU

- Test Setup: Rx@SP3 → MNC 1 → MNC 2 → Tx@SP2
- Procedure:
The MNC 2 (0x402) is set in retimed bypass mode with the value of duration of 1.000.000 ms. Then MNC 1 (0x401) is also set in retimed bypass mode and gives the test result. The bit error result by FBlock Extended Network Control and the bit error result at the Tester Node will be read back with the Physical node address 0x401. Note that the resulting pattern is inverted.

3.7 Test of data recovery at the DUT Receive section

In order to create stress scenarios for the DUT's SP3 interface, the following conditions are varied:

Cable emulation

This influences frequency spectrum and signal strength at SP3.

- | | | |
|--------|---|-------------------------------|
| "Low" | – | low attenuation cable 1 |
| "Mid" | – | medium attenuation cable 2 |
| "Max." | – | max. attenuation cable 3 |
| | | (worst case according to [3]) |

The output signal of the MTCM has to correspond to the following requirements:

- The test setup has to fulfill all parameters for SP3 as specified in [3]
 - The MOST50 Stress Test Pattern as specified in [3] has to be applied.
 - The stress conditions as previously listed have to be applied.
- For more details, see Appendix B: SP3 Stress Conditions.

Table 3-1 shows the test cases

Test case	Attenuation cable	Temperature/ Voltage Range
1	Low attenuation cable 1	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
2	Mid attenuation cable 2	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
3	Max. attenuation cable 3	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
4	Low attenuation cable 1	$T_{\text{max}} / U_{\text{min}}$
5	Mid attenuation cable 2	$T_{\text{max}} / U_{\text{min}}$
6	Max. attenuation cable 3	$T_{\text{max}} / U_{\text{min}}$
7	Low attenuation cable 1	$T_{\text{max}} / U_{\text{max}}$
8	Mid attenuation cable 2	$T_{\text{max}} / U_{\text{max}}$
9	Max. attenuation cable3	$T_{\text{max}} / U_{\text{max}}$
10	Low attenuation cable 1	$T_{\text{min}} / U_{\text{min}}$
11	Mid attenuation cable 2	$T_{\text{min}} / U_{\text{min}}$
12	Max. attenuation cable3	$T_{\text{min}} / U_{\text{min}}$
13	Low attenuation cable 1	$T_{\text{min}} / U_{\text{max}}$
14	Mid attenuation cable 2	$T_{\text{min}} / U_{\text{max}}$
15	Max. attenuation cable 3	$T_{\text{min}} / U_{\text{max}}$

Table 3-1: Summary of Test cases

3.8 Measurement of SP2 output signal of the DUT

According to Table 2-1 the parameters in Table 3-2 below have to be measured for each test case. The tests have to be performed at

1. $T_{23^{\circ}\text{C}} / U_{\text{typ}}$;
2. $T_{\text{min}} / U_{\text{min}}$;
3. $T_{\text{min}} / U_{\text{max}}$;
4. $T_{\text{max}} / U_{\text{min}}$;
5. $T_{\text{max}} / U_{\text{max}}$;

while going from $U_{\text{typ}} \rightarrow U_{\text{min}} \rightarrow U_{\text{max}}$.

Measurement of the DUT-SP2 signal	Setup
Spectral and Amplitude: <ul style="list-style-type: none"> ▪ RMS signal amplitude V_{rms2} ▪ PSD 	<ul style="list-style-type: none"> ▪ MOST50 Stress Test Pattern ▪ MOST50 PSD Test Pattern
Timing: <ul style="list-style-type: none"> ▪ Transferred Jitter via RMS ▪ Alignment Jitter acc. to Eye Mask 	<ul style="list-style-type: none"> ▪ MOST50 Stress Test Pattern ▪ MOST50 Stress Test Pattern

Table 3-2: Summary of measurements at SP2 (DUT)

A detailed description of the measurement is given by the MOST50 bPHY Compliance Measurement Guideline [5].

3.9 Measurement of Return Loss

The Return Loss of ECU Interfaces SP2 and SP3 is measured at the ECU's device connector [3]. For a setup description, refer MOST50 bPHY Compliance Measurement Guideline [5].

Return Loss RL_{SP2} and RL_{SP3} describes impedance matching considering all relevant components. This includes passive components in the AFE as well as active components inside the MNC or passive components inside MNC activated by MNC functionality. To get The ECU into the correct operational mode, follow instructions from MNC supplier.

3.10 Functional testing of Wake-up and Shutdown

For verification of correct design of all physical layer components within devices the wakeup and shutdown functionality shall be checked. Test will be conducted using Setup as described in section 3.2

The tester node is being operated in master mode resp. in slave mode depending on the DUT's intended role.

1. Wake-up:

Starting from DUT in sleep mode (detectable by monitoring of power consumption), a MOST wake-up event is applied to the DUT. The DUT has to generate the MOST signal. The test is only feasible for a DUT that is wakeable via MOST signal. This test is not applied for the PowerMaster either.

Reason: There might be devices that are not wakeable via MOST signal (e.g., typically this may be the case for the PowerMaster in a certain system integration.)

2. Shutdown:

a) If DUT = TimingSlave

Stress Test tool sets Shutdown flag (t_0).

Stress Test Tool switches off modulated signal (t_1)

As shutdown flag has been set, DUT has to follow and switch off modulated signal.

b) If DUT = TimingMaster

Stress Test Tool switches off modulated signal (t_1)

As shutdown flag has not been set, DUT has to set shutdown flag and switch off modulated signal.

Note: Test cases Wake-up and Shutdown are only functional tests (i.e., no measurement of timing).

4 Direct physical measuring accuracy

Requirement for measurement equipment distinguishes the following notions:

1. Requested accuracy
2. Validated measurement uncertainty: (95% confidence interval)
3. Systematic measurement deviation are either negligible or needs to be compensated.

Direct physical measuring accuracy:	
Operating voltage	$\pm 0,25$ V range for Limited Compliance / U_{Batt}
RMS Signal Amplitude	± 7 mV
Timing	<p>Alignment Jitter according to eye mask: Alignment Jitter according to eye mask measurement is a pass / fail test.</p> <p>Accuracy (vertical and horizontal): ± 7 mV steady state amplitude ± 50 ps</p> <p>Transfer Jitter: Accuracy: ± 10 ps.</p>
Attenuation and Return Loss	Return Loss: $\pm 0,9$ dB
Temperature	$\pm 2^{\circ}\text{C}$

Table 4-1: Summary of accuracy of measurement setup

5 Appendix A: Limited Physical Layer Compliance for Development Tools

Development Tools must be listed in MCPL, too. Therefore, tools have to pass Limited Physical Layer Compliance. Based on the functionality of a tool, not all test may be applicable.

The example test plan for a data logger (development tool) looks as follows. E.g., due to a missing FBlock ENC the data consistency cannot be tested during Limited Physical Layer Compliance.

	Parameter to be compliant	Device
	Unlock ET Block	Not tested
	Bit error ET Block	Not tested
	Unlock PhLSTT	Not tested
	Bit error PhLSTT	Not tested
	RMS signal amplitude	passed
	Transfer Jitter (Jtr2) (RMS)	passed
	Alignment Jitter acc. to Eye Mask	passed
	functional Wake-Up	passed
	functional Shutdown	passed
	Return Loss. SP2 and SP3	passed
	Limited Physical Layer Test of Data	Not tested

Figure 5-1: Example Test Plan for a data logger

6 Appendix B: SP3 Stress Conditions

Table 6-1 show shows the definition of the cable models for the SP3 stress conditions.

Cable model	Attenuation @ 10 MHz	Attenuation @ 33 MHz
Cable Model Low	0 .. -1 dB	0 .. -1 dB
Cable Model Mid	-1 .. -2 dB	-2 .. -3 dB
Cable Model High	-2 .. -2.6 dB	-3.9 .. -4.9dB

Table 6-1: Cable Emulations

7 Appendix C: Index of Figures

Figure 1-1: Specification Point Locations	7
Figure 1-2: Control Signals for ON/Off Behavior	7
Figure 3-1: Test Setup for Limited Physical Layer Compliance test	9
Figure 3-2: Test Flow Overview	11
Figure 5-1: Example Test Plan for a data logger.....	16

8 Appendix D: Index of Tables

Table 2-1: Compliance procedures for all parameters of specification points.	8
Table 3-1: Summary of Test cases	12
Table 3-2: Summary of measurements at SP2 (DUT)	13
Table 4-1: Summary of accuracy of measurement setup	15
Table 6-1: Cable Emulations	16

Notes: