

# MOST

Media Oriented Systems Transport

Multimedia and Control  
Networking Technology

**MOST150 cPhy Compliance Verification Procedure –  
Physical Layer Errata4 Rev. 1.0-00E4  
03/2019**

**MOSTCO CONFIDENTIAL**

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## Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

	Document	Revision
[1]	<b>MOST Specification</b>	3.0E2
[2]	<b>MOST Basic Physical Specification</b>	1.0
[3]	<b>MOST150 cPhy Automotive Physical Layer Sub-Specification</b>	1.1
[4]	<b>MOST Compliance Requirements</b>	2.3
[5]	<b>MOST150 cPhy Compliance Measurement Guideline</b>	1.0
[6]	<b>FBlock Enhanced Testability</b>	3.0.4

*MOST Document references*

## Document History

### Changes to 1.0E4 Errata

Change Ref.	Section	Changes
1.0-00E4-001	3.8	Functional testing of wake-up and shutdown instead of Measurement of $t_{WakeUp}$ and $t_{Shutdown}$

### Changes to 1.0E3 Errata

Change Ref.	Section	Changes
1.0-00E3-001	9	Added Appendix E: Test Procedure 2-Port Nodes

### Changes to 1.0E2 Errata

Change Ref.	Section	Changes
1.0-00E2-001	8	Added Appendix D: Compensation Setup for cPhy Duplex (normative).
1.0-00E2-002	4	Return Loss Measurement Uncertainty changed from $\pm 0.3$ dB to $\pm 0.9$ dB.

### Changes to 1.0 Errata

Change Ref.	Section	Changes
1.0-00E1-001	5	Appendix A: Particular Case when DUT implements FBlock 0x0A
1.0-00E1-002	3.5	Test case with noise adder will not be performed.
1.0-00E1-003	7	Tolerance for slow edge (1400 ps) changed from -100 ps to -200 ps

### Changes

Change Ref.	Section	Changes
1.0-00		New Issue

# 1 Introduction

## 1.1 Relevance of Compliance

Compliance in terms of physical layer means products have to fulfill all specified parameters. This includes electrical and coaxial parameters, signal-timing as well as mechanical properties. For verification of these parameters, suppliers of devices, modules and components have to implement suitable processes like product characterization, qualification and end-of-line-testing (considering environmental conditions, stability over lifetime, etc.) There are various industry and automotive standards defining procedures and quality requirements (e.g., ISO 9000, ISO/TS 16949, AEC Q100, AEC Q200).

The process of compliance certification is defined to check a subset of parameters. Therefore the compliance certification performs only a crosscheck with focus on basic network interoperability. The compliance verification is on device level. Compliance on chip level is covered through characterization and beyond the scope of this document.

## 1.2 Related Documents

The MOST Basic Physical Specification [2] in combination with the MOST150 cPhy Automotive Physical Layer Sub-Specification [3] defines all relevant parameters. There are also mechanical drawings, referenced in [3] which are relevant for compliance. The MOST150 cPhy Compliance Measurement Guideline [5] describes how to determine and measure parameters. These documents are applicable for MOST devices as well as for modules and components. The process of Compliance Verification is defined in the document MOST Compliance Requirements [4]. It describes how to achieve a compliance certification for MOST subsystems.

Terminology of naming within these documents:

MOST End Product in document [4] = Device in document [3,5]:

Any product within the bounds of scope that is offered for sale or is distributed in an unmodified form to any end user who acquires the product for such end user's personal or commercial use, alone or in combination with any other product.

## 1.3 MOST Link

### 1.3.1 Location of Interfaces

SP1 describes input parameters for the ECC. It also describes the output parameters of a NIC, including data path between NIC and ECC.

SP2 defines the coaxial output signal.

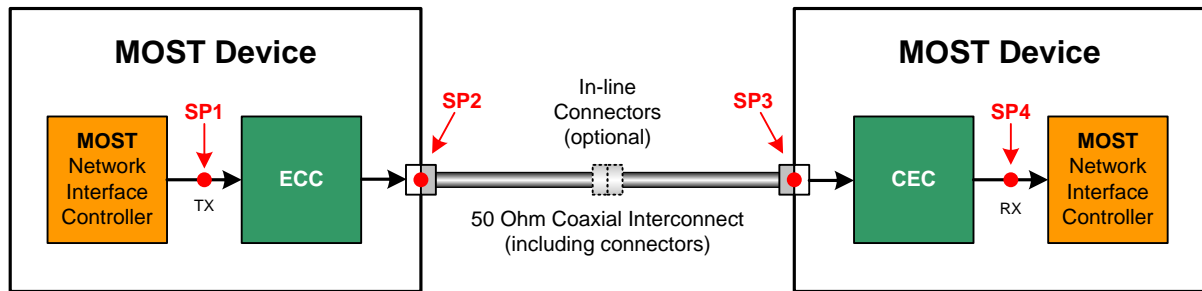


Figure 1-1: Specification Point Locations for Simplex Interconnect

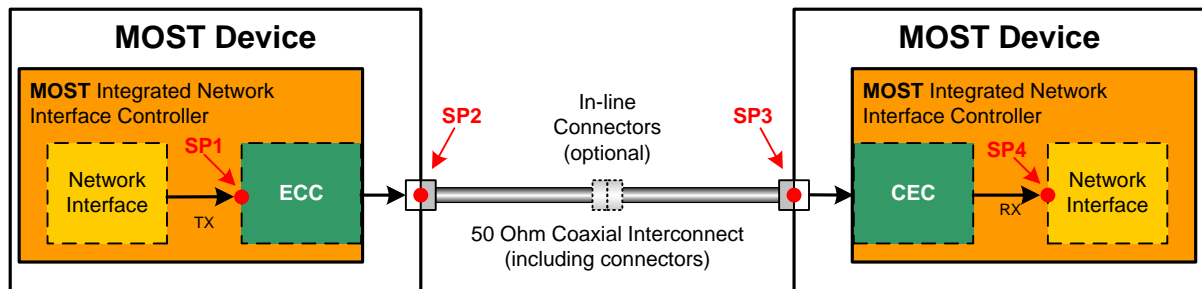


Figure 1-2: Specification Point Locations for Simplex Interconnect with integrated Coaxial Transceivers

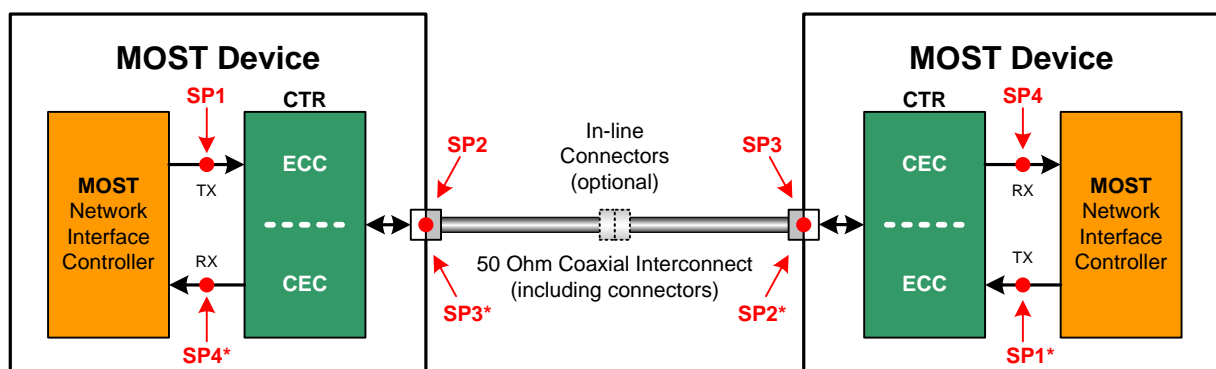


Figure 1-3: Specification Point Locations for Duplex Interconnect

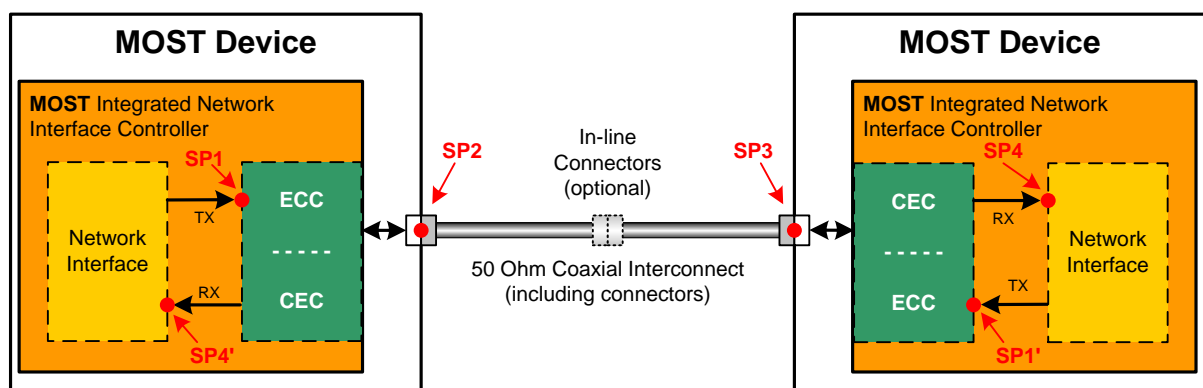


Figure 1-4: Specification Point Locations for Duplex Interconnect with integrated Coaxial Transceivers

SP3 describes the coaxial input interface for the CEC. Signal characteristics at SP3 need to consider worst case coaxial signal according SP2-definition plus deterioration due to the transport media.

SP4 link quality describes the output parameters for CECs including termination.  
SP4 receiver tolerance specifies the input tolerance for NICs and is relevant for system evaluation.

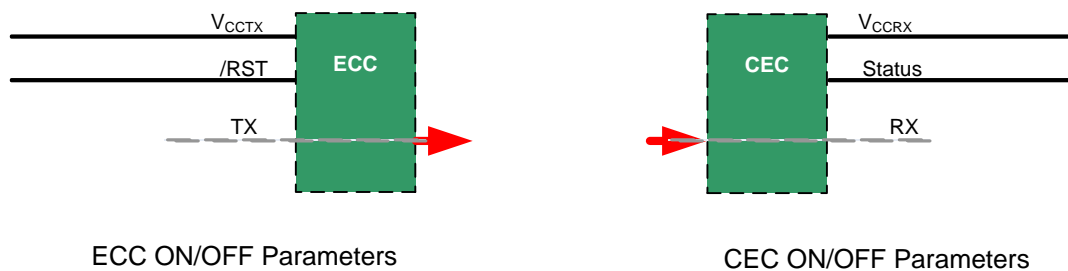
Signals that fulfill the SP4 parameters can be recovered by the NIC, signals outside the ranges may cause bit errors. On TX of the NIC (node n+1) a recovered signal is available according to SP1 requirements, timing distortion (except transferred jitter) is eliminated.

### 1.3.2 Control Signals

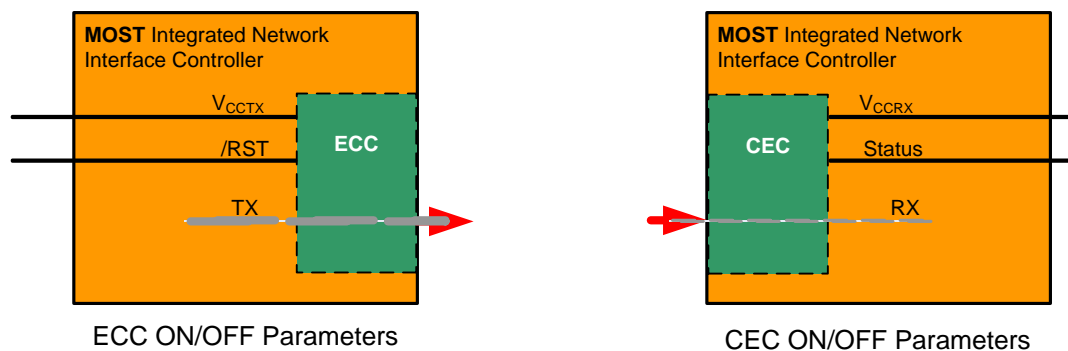
In addition to power supply terminals and data pins, an ECC needs to provide a /RST input. The ECC provides activity detection in order to enable/disable MOST signal. Activity depends on VCC state, data content of SP1 and reset state.

The CEC also provides activity detection. Depending on the characteristics of the input signal (power level, signal content) ON/OFF state is signaled by the Status line.

There exists both a stand-alone and an integrated version of CEC/ECC.



*Figure 1-5: Control Signals for ON/Off Behavior (stand-alone)*



*Figure 1-6: Control Signals for ON/Off Behavior (integrated)*



## 1.4 Limited access to specification points

Verification of parameters at particular SPs requires access to that particular interface. In addition for most of the parameters a stimulation signal at the previous SP is required. Full access to all SPs is only guaranteed on “CE port/EC port” level and “chip” level.

On “device” level MCTHs do not have access to SP1 and SP4. For an MCTH on “device” level only SP2 and SP3 are visible. Therefore variation on input parameters can only be applied at SP3 (coaxial signal input of the device). Parameters can only be measured at SP2. The power supply of NIC, ECC and CEC is fixed by the design of the device and cannot be varied. Considering these circumstances the “limited physical layer compliance” describes a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (refer chapter 3, Limited Physical Compliance).

The MOST specification of **MOST Compliance Requirements** [4] offers the opportunity of testing components and modules according their “covered functionality”. Depending on the partitioning of components within modules or Devices the respective parameters can be verified at single components. These parameters need to be verified on higher product integration levels.

## 2 Parameter-Overview

The following table shows the parameters of the MOST150 cPhy Automotive Physical Layer Sub-Specification [3] relevant for Limited Physical Layer Compliance. Indications about the meaning of the parameters for the interfacing components, modules and device (input, output, property) and appropriate measuring methods are given in MOST150 cPhy Compliance Measurement Guideline [5].

Parameters, defined in the MOST150 cPhy Automotive Physical Layer Sub-Specification [3] are mandatory parameters for component/module datasheets. The verification of these parameters is done using the procedure of the product characterization.

Table 2-1 shows the specified parameters of the MOST150 cPhy Compliance Measurement Guideline [5] relevant for Limited Physical Layer Compliance. In addition, this table indicates the test conditions which have to be applied during Limited Physical Layer Compliance.

**Note:** Developers of components or modules have to ensure that their products fulfill the specification under min/max conditions of their input parameters, considering environmental conditions and over lifetime.

	Parameter to be compliant	Limited Physical Layer: Device
SP2		
	Output $V_{SS}$ steady-state amplitude	M(TU)
	Transition time (rise and fall)	M(TU)
	Alignment Jitter acc. to Eye Mask	M(TU)
	Transferred Jitter via RMS	M(TU)
	Return Loss of ECU-Interface	M ( $T_{typ.}$ ) (only Duplex)
SP3		
	Limited Physical Layer Test of Data consistency	M(TUA)
	Return Loss of ECU-Interface	M ( $T_{typ.}$ ) Simplex, Duplex)

Table 2-1: Compliance procedures for all parameters of specification points.

Legend:

Procedures:

- = No compliance test necessary
- M = Measure (T=Temperature Range, U=Voltage Range, A=Attenuation)

## 3 Limited Physical Compliance

### 3.1 Overview

Limited Physical Layer Compliance refers to MOST devices (refer section 1.4, Limited access to specification points).

Generally, compliance testing requires access to all specification points. In addition various test signals have to be applied to particular interface in order to check worst case performance of components and modules that are connected to that interface. The whole testing has to consider all environment conditions (e.g. specified operating temperature, power supply variations).

An overview of the parameters to be tested and verified is given Table 2-1.

The following diagram shows the required test setup for limited physical layer testing comprising the following equipment:

- Physical Layer Stress Test Tool (PhLSTT)
- MOST Tester Cable Model (MTCM)
  - Attenuator
  - Cable representation
  - Directional coupler
- Oscilloscope

**Test Setup 1 (SIMPLEX):**

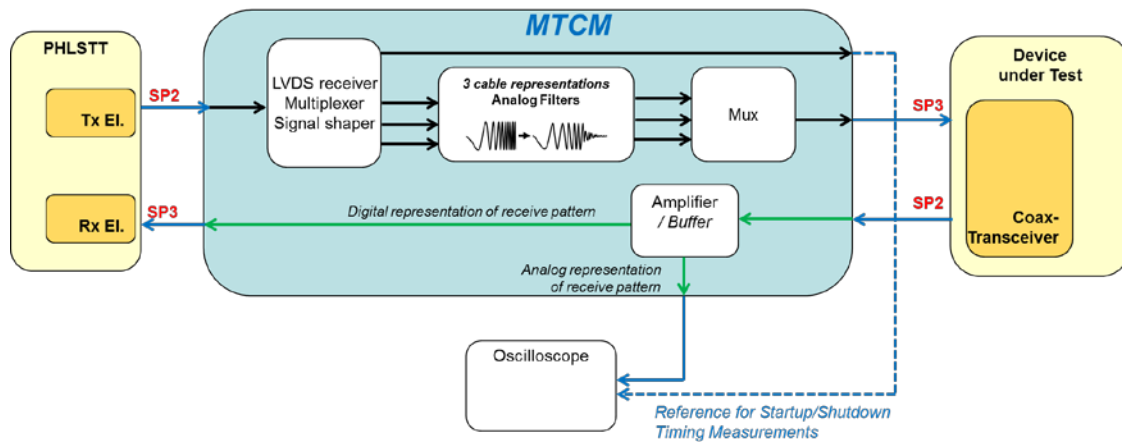


Figure 3-1: Test Setup 1 (SIMPLEX) for Limited Physical Layer Compliance test

**Test Setup 2 (DUPLEX)**

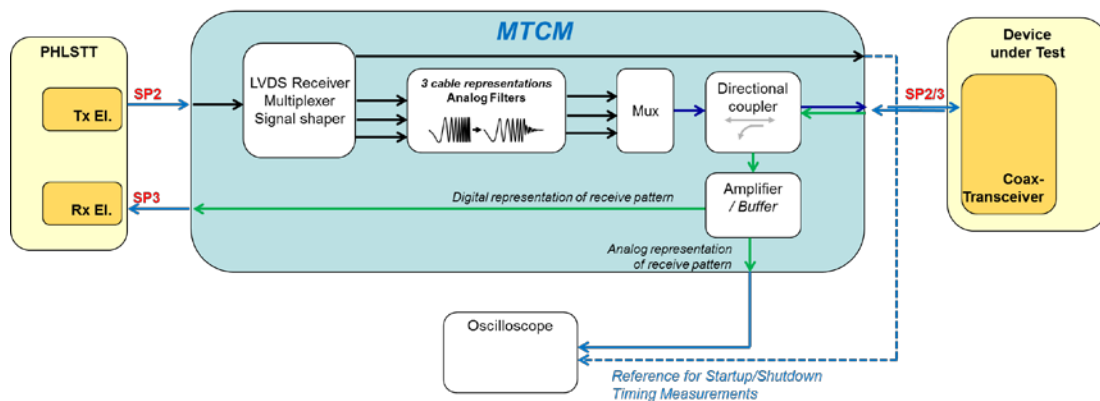


Figure 3-2: Test Setup 2 (DUPLEX) for Limited Physical Layer Compliance test

**Test Setup 1 and 2:**

- Prove of valid data transmission in presence of various stress scenarios applied to the receive path of the DUT.
- Check of data consistency by comparison of the DUT's input and output data stream (in practice executed on PhLSTT, comparison of PhLSTT output and input data stream).
- Check of Lock condition and Data Error state, acquired by the DUT's receive section.
- Measurement at DUT's coaxial output (SP2), Verification of signal integrity of coaxial signal at SP2.

Verification of signal integrity includes measurement of pulse shape and timing characteristics at the DUT's coaxial SP2 interface. The test flow shown in section 3.4 requires a closed loop between PhLSTT and DUT, providing functional communication over MOST.

- Verification of  $t_{WakeUp}$  and  $t_{Shutdown}$ .

## 3.2 Generating test signals for the DUT Input section SP3

A test signal for testing the DUT's input section may be varied in several instances and combinations of these instances (e. g., timing properties, pulse shape characteristics, data content and interconnect attenuation). A subset of such variations is realized with the PhLSTT and the MTCM (MOST Tester Cable Model) which is a mandatory tool for Limited Physical Layer Test.

The PhLSTT initiates and controls the whole test sequences. The PhLSTT controls the DUT using communication via MOST control channel. It addresses the DUT's FBlock Enhanced Testability (ET) which covers all necessary DUT functions for the tests (e.g. "retimed bypass", handling of various error counters). The PhLSTT is capable to act as Timing Master or Slave. Besides standard MOST communication, the PhLSTT has the capability to send a worst case stress pattern.

For the test, the worst case stress pattern is combined with attenuation on the coaxial link and bandwidth limitation due to the transport medium before being applied to the DUT's SP3 Interface.

## 3.3 Analysis of Test results

Error Counters are implemented in the DUT (FBlock Enhanced Testability). These counters give a measure for communication errors on the input of a device. These counters are activated during the test sequence. The result can be read after the test.

During the test sequence, the DUT is set in the "retimed bypass" mode. This means that the recovered data on the input side are sampled with the internal clock and transferred to the output. Therefore as long as there are no bit errors, the worst case stress pattern created by the PhLSTT will appear with identical content on the output of the DUT. This enables a comparison of the data content inside the PhLSTT (Limited Physical Layer Test of Data consistency).

In addition to generation of the signal, it is important to check whether the pattern sent is also correctly recognized by the DUT during the test execution. In order to be able to carry out this check, the DUT is set in a special bypass mode; the "Retimed Bypass Mode". This mode forwards the received pattern in unmodified form. In this way, the pattern at the output of the DUT can be compared with the pattern applied from the PhLSTT. For this case a pattern comparator is implemented in the PhLSTT. Analysis of the pattern comparator relates to two characteristics: The bit errors occurred and sudden phase shifts in the received signal. Both incidents are counted by the PhLSTT and reported after completion of the test.

## 3.4 Test Flow Overview

Figure 3-3 depicts an overview of the test flow.

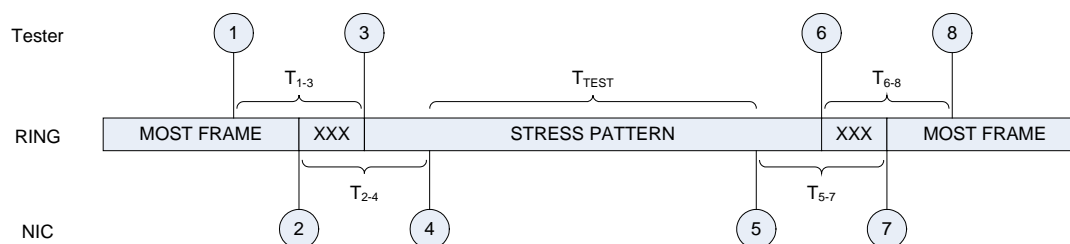


Figure 3-3: Test Flow Overview

- 1 – PhLSTT sends command to DUT over MOST (FBlock Enhanced Testability) to enter Test Mode.
- 2 – DUT enters Retimed Bypass Mode.
- 3 – PhLSTT starts transmitting the Stress Pattern.
- 4 – DUT clears the Error Counter and Lock Log.

... PHYSICAL LAYER STRESS TESTING ...

- 5 – DUT reads back Error Counter and Lock Log.
- 6 – PhLSTT switches to MOST Communication Mode.
- 7 – DUT switches back to its original MOST Mode.
- 8 – PhLSTT reads back the result.

Switching times ( $T_{X-Y}$ ) are in the range 10 – 500 ms with accuracy better or equal than 10 ms;

Lead-in / Lead-out: typ. 1000ms (min. 500ms; max. 2000ms).

$T_{TEST}$  time is in the range 1 sec – 1000 sec with accuracy better or equal than 10 ms.

Duration: max. 1000 seconds.

#### Test of multi-node devices with two NICs:

- Test Setup: Rx@SP3 → NIC 1 → NIC 2 → Tx@SP2
- Procedure:  
The NIC 2 (0x402) is set in retimed bypass mode with the value of duration of 1.000.000 ms. Then NIC 1 (0x401) is also set in retimed bypass mode and gives the test result. The result by ET and the result by the PhLSTT will be read back with the Physical node address 0x401. Note that the resulting pattern is inverted.

## 3.5 Test of data consistency of the DUT

In order to create stress scenarios for the DUT's SP3 interface, the following conditions are varied:

#### Cable emulation

This influences frequency spectrum and signal strength at SP3.

"Low"	–	low attenuation cable 1
"Mid"	–	medium attenuation cable 2
"Max."	–	max. attenuation cable 3
(worst case according to [3])		

SP2 pulse shape	fast edge	(min. SP2 transition time according to [3])
	slow edge	(max. SP2 transition time according to [3])

The output signal of the MTCM has to correspond to the following requirements:

- The test setup has to fulfill all parameters for SP3 as specified in [3]
- The MOST Stress Test Pattern as specified in [3] has to be applied.
- The stress conditions as previously listed have to be applied.  
For more details, see Appendix C: SP3 Stress Conditions.

Table 3-1 shows the test cases for both SIMPLEX and DUPLEX.

Test case	Attenuation cable	SP2 pulse shape	Temperature/ Voltage Range
1	Low attenuation cable 1	slow	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
2	Mid attenuation cable 2	fast	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
3	Max. attenuation cable 3	slow	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
4	Low attenuation cable 1	fast	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
5	Mid attenuation cable 2	slow	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
6	Max. attenuation cable 3	fast	$T_{23^{\circ}\text{C}} / U_{\text{typ}}$
7	Low attenuation cable 1	slow	$T_{\text{max}} / U_{\text{min}}$
8	Mid attenuation cable 2	fast	$T_{\text{max}} / U_{\text{min}}$
9	Max. attenuation cable 3	slow	$T_{\text{max}} / U_{\text{min}}$
10	Low attenuation cable 1	fast	$T_{\text{max}} / U_{\text{min}}$
11	Mid attenuation cable 2	slow	$T_{\text{max}} / U_{\text{min}}$
12	Max. attenuation cable 3	fast	$T_{\text{max}} / U_{\text{min}}$
13	Low attenuation cable 1	slow	$T_{\text{max}} / U_{\text{max}}$
14	Mid attenuation cable 2	fast	$T_{\text{max}} / U_{\text{max}}$
15	Max. attenuation cable3	slow	$T_{\text{max}} / U_{\text{max}}$
16	Low attenuation cable 1	fast	$T_{\text{max}} / U_{\text{max}}$
17	Mid attenuation cable 2	slow	$T_{\text{max}} / U_{\text{max}}$
18	Max. attenuation cable 3	fast	$T_{\text{max}} / U_{\text{max}}$
19	Low attenuation cable 1	slow	$T_{\text{min}} / U_{\text{min}}$
20	Mid attenuation cable 2	fast	$T_{\text{min}} / U_{\text{min}}$
21	Max. attenuation cable3	slow	$T_{\text{min}} / U_{\text{min}}$
22	Low attenuation cable 1	fast	$T_{\text{min}} / U_{\text{min}}$
23	Mid attenuation cable 2	slow	$T_{\text{min}} / U_{\text{min}}$
24	Max. attenuation cable 3	fast	$T_{\text{min}} / U_{\text{min}}$
25	Low attenuation cable 1	slow	$T_{\text{min}} / U_{\text{max}}$
26	Mid attenuation cable 2	fast	$T_{\text{min}} / U_{\text{max}}$
27	Max. attenuation cable 3	slow	$T_{\text{min}} / U_{\text{max}}$
28	Low attenuation cable 1	fast	$T_{\text{min}} / U_{\text{max}}$
29	Mid attenuation cable 2	slow	$T_{\text{min}} / U_{\text{max}}$
30	Max. attenuation cable 3	fast	$T_{\text{min}} / U_{\text{max}}$

Table 3-1: Summary of Test cases (SIMPLEX and DUPLEX)

### 3.6 Measurement of SP2 output signal of the DUT

According to Table 2-1 the parameters in Table 3-2 below have to be measured for each test case. The tests have to be performed at

1.  $T_{23^{\circ}\text{C}} / U_{\text{typ}}$  ;
2.  $T_{\text{min}} / U_{\text{min}}$  ;
3.  $T_{\text{min}} / U_{\text{max}}$  ;
4.  $T_{\text{max}} / U_{\text{min}}$  ;
5.  $T_{\text{max}} / U_{\text{max}}$  ;

while going from  $U_{\text{typ}} \rightarrow U_{\text{min}} \rightarrow U_{\text{max}}$ .

Measurement of the DUT-SP2 signal	Setup
<ul style="list-style-type: none"> <li>Output steady-state amplitude <math>V_{\text{SS2}}</math></li> </ul>	Test Setup 1 / Test Setup 2
Timing: <ul style="list-style-type: none"> <li>Transferred Jitter via RMS</li> <li>Alignment Jitter acc. to Eye Mask</li> <li>Transition times (rise-/fall-times (<math>t_{r2}</math>, <math>t_{f2}</math>))</li> </ul>	Test Setup 1 / Test Setup 2

Table 3-2: Summary of measurements at SP2 (DUT)

**Note:** All measurements have to be done with the stress pattern.

A detailed description of the measurement is given by the MOST150 cPhy Compliance Measurement Guideline [5].

### 3.7 Measurement of Return Loss

The Return Loss of ECU-Interface is measured at the device connector [3].

SIMPLEX: Only at SP3 ( $RL_{\text{SP3}}$ )

Setup: Refer to Measurement Guideline.

DUPLEX: At SP2/SP3 ( $RL_{\text{SP2\_SP3}}$ )

Setup: Refer to Measurement Guideline

## 3.8 Fuctional Testing of Wake-up and Shutdown

For verification of correct design of all physical layer components within devices the wake-up and shutdown functionality shall be checked using Test Setup 1 or Test Setup 2, respectively. The tester is in master mode resp. in slave mode depending on the DUT.

### 1. Wake-up:

Starting from DUT in SleepMode (detectable by monitoring of power consumption), a MOST wake-up event is applied to the DUT. The DUT has to generate the MOST signal. The test is only feasible for a DUT that is wakeable via MOST signal. This test is not applied for the PowerMaster either.

*Reason: There might be devices that are not wakeable via MOST signal (e.g., typically this may be the case for the PowerMaster in a certain system integration.)*

### 2. Shutdown:

#### a) If DUT = TimingSlave

Measure  $t_{\text{Shutdown}}$ :

Stress Test tool sets Shutdown flag ( $t_0$ ).

Stress Test Tool switches off modulated signal ( $t_1$ )

As shutdown flag has been set, DUT has to follow and switch off modulated signal.

#### b) If DUT = TimingMaster

Stress Test Tool switches off modulated signal ( $t_1$ )

As shutdown flag has not been set, DUT has to set shutdown flag and switch off modulated signal.

*Note: Test cases Wake-up and Shutdown are only functional tests (i.e., no measurement of timing).*



## 4 Direct physical measuring accuracy

Requirement for measurement equipment distinguishes the following notions:

1. Requested accuracy
2. Validated measurement uncertainty: (95% confidence interval)
3. Systematic measurement deviation are either negligible or needs to be compensated.

Direct physical measuring accuracy:	
Operating voltage	$\pm 0,25$ V-range for Limited Compliance / $U_{Batt}$
Signal Amplitude	$\pm 7$ mV steady state amplitude
Timing	<p><b>Transition time:</b> Mean value, Accuracy: <math>\pm 50</math> ps In case of discrepancies the measurement has to be performed with different UI classes.</p> <p><b>Alignment Jitter according to eye mask:</b> Alignment Jitter according to eye mask measurement is a pass / fail test. Accuracy: <math>\pm 7</math> mV steady state amplitude <math>\pm 50</math> ps</p> <p><b>Transfer Jitter:</b> Accuracy: <math>\pm 10</math> ps.</p> <p><b>Timing for <math>t_{WakeUp}</math>, <math>t_{Shutdown}</math> :</b> 0,5 ms</p>
Attenuation and Return Loss	Return Loss: $\pm 0,9$ dB
Temperature	$\pm 2^{\circ}\text{C}$

Table 4-1: Summary of accuracy of measurement setup

## 5 Appendix A: Particular Case when DUT implements FBlock 0x0A

The FBlock with FBlockID 0x0A (ExtendedNetworkControl) contains the functions PhysicalLayerTest (0x220) and PhysicalLayerTestResult (0x221).

If the node implements an FBlock with FBlockID 0x0A, the Limited Physical Layer Test of data consistency has to use the functions of FBlock 0x0A.

### PhysicalLayerTest (0x220)

This function starts the physical layer test on a MOST Port.

#### Format of Function

Function classes: Unclassified Method

FBlock	Function	OPType	Parameter
ExtendedNetworkControl (0x0A)	PhysicalLayerTest (0x220)	Start	<a href="#">PortNumber</a> , <a href="#">Type</a> , <a href="#">LeadIn</a> , <a href="#">Duration</a> , <a href="#">LeadOut</a>
		Error	<a href="#">ErrorCode</a> , <a href="#">ErrorInfo</a>

#### Parameter

##### PortNumber

Number of MOST Port the test is performed on.

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Byte			1	none

##### Type

Indicates the type of physical layer test. The device is switched back to its original mode after the physical layer test is finished and the MOST network has been started up again.

Basis data type	Range of values	Code	Symbolic Name	Description
Enum	0x01...0x02	0x01	RetimedBypassTimingMaster	RetimedBypassTimingMaster
		0x02	RetimedBypassTimingSlave	RetimedBypassTimingSlave

##### LeadIn

Lead in time of physical layer test

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Word			1	ms

**Duration**

---

Duration time of physical layer test

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Long		50...4294967295	1	ms

**LeadOut**

---

Lead out time of physical layer test

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Word			1	ms

## PhysicalLayerTestResult (0x221)

This function returns the result for the tested MOST Port, after the physical layer test has been finished.

### Format of Function

Function classes: Unclassified Property

FBlock	Function	OPType	Parameter
ExtendedNetworkControl (0x0A)	PhysicalLayerTestResult (0x221)	Get	-
		Status	<a href="#">PortNumber</a> , <a href="#">LockStatus</a> , <a href="#">ErrorCounterValue</a>
		Error	<a href="#">ErrorCode</a> , <a href="#">ErrorInfo</a>

### Parameter

#### PortNumber

Number of MOST Port the test was performed on. If the handle is invalid, 0xFF is returned.

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Byte			1	none

#### LockStatus

Indicates if an unlock has occurred during the physical layer test

Basis data type	Bit #	Code	Description
Boolean	Bit 0	True	True
		False	False

#### ErrorCounterValue

Number of detected coding errors occurred during physical layer test

Basis data type	Exp.	Range of values	Step	Unit
Unsigned Word			1	none

## 6 Appendix B: Limited Physical Layer Compliance for Development Tools

Development Tools must be listed, too. Applicable parts have to pass Limited Physical Layer Compliance. The example test plan for a data logger (development tool) looks as follows. E.g., due to a missing FBlock ET the data consistency cannot be tested during Limited Physical Layer Compliance.

	Parameter to be compliant	Device
	Output $V_{SS}$ Steady-state amplitude	passed
	Unlock ET Block	Not tested
	Bit error ET Block	Not tested
	Unlock PhLSTT	Not tested
	Bit error PhLSTT	Not tested
	Rise time ( $tr_2$ )	passed
	Fall time ( $tf_2$ )	passed
	Transfer Jitter ( $Jtr_2$ ) (RMS)	passed
	Alignment Jitter acc. to Eye Mask	passed
	Bit rate	passed
	T_Wakeup	passed
	T_shutdown	passed
	Return Loss	passed
	Limited Physical Layer Test of Data consistency	Not tested

Figure 6-1: Example Test Plan for a data logger

## 7 Appendix C: SP3 Stress Conditions

Table 7-1 show shows the definition of the cable models.

Cable model	DC Loss [dB]	FSkin [Hz/dB <sup>2</sup> ]	Attenuation Conformance Corridor [dB]	Input V <sub>ss</sub> [mV] into Cable model
Cable Model Low	low loss test cable	low loss test cable	±1	420 (- 30)
Cable Model Mid	0.1 (+0.1; - 0.0 )	15.0x10 <sup>6</sup> (±1.0x10 <sup>6</sup> )	±1	360 (±15)
Cable Model High	0.5 (+0.0; - 0.1)	9.2x10 <sup>6</sup> (+1.0x10 <sup>6</sup> ; -0.0)	±1	300 (+ 30)

Table 7-1: Cable Models

Table 7-2 show shows the definition of the cable models.

SP2 pulse shape	Rise/Fall time [ps]
fast edge	700 (+100)
slow edge	1400 (- 200)

Table 7-2: SP2 pulse shape

## 8 Appendix D: Compensation Setup for cPhy Duplex (normative)

### 8.1 Introduction

The Compliance test setup requires usage of a directional coupler to measure SP2 performance. The directional coupler is not an ideal component and provides some impedance mismatch to the measurement system. In presence of a signal, transmitted from the PhLSTT through the MCTM to the DUT, the impedance mismatches between MCTM and DUT (including the components directional coupler, cable, DUT AFE) may create reflections. These reflections may compromise the DUT's output signal at SP2. In order to improve measurement accuracy, a crosstalk compensation is required.

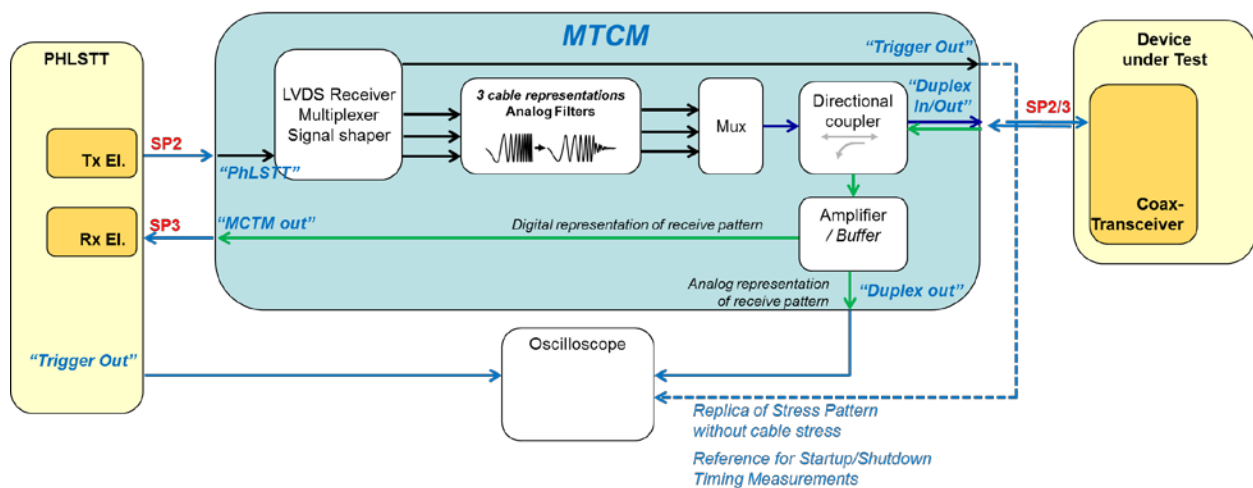


Figure 8-1: Test Setup 2 (DUPLEX) – Compensation setup

Two general scenarios need to be distinguished:

Scenario A: DUT = Timing Slave:

The PhLSTT is the Timing Master and thus PhLSTT provides the network clock reference.

Scenario B: DUT = Timing Master, therefore the PhLSTT is a Timing Slave.

The DUT actually provides the network clock reference.

During the process of determining the compensation the PhLSTT must be delivering the network clock reference. The resulting pattern later needs to be resampled and transferred to the DUT's clock domain.

#### 8.1.1 Related Documents

The MOST150 cPhy Compliance Measurement Guideline [5] describes how to determine and measure parameters. The process of Compliance Verification is defined in the document MOST150 cPhy Compliance Verification Procedure Physical Layer [3].

## 8.2 Compensation Method for Setup related Reflections

The MOST150 cPhy Compliance test setup allows to test a DUT under pre-defined stress and to check data consistency as well as SI performance on the DUT's data output (SP2).

The setup consists of PhLSTT, MCTM, oscilloscope and DUT.

Impedance mismatches, especially between DUT SP2/3 interface and MCMT (directional coupler, Cable) cause reflections which overlay with the DUT's output signal and degrade SI performance measured on the oscilloscope.

### 8.2.1 Scenario A: DUT as TimingSlave

In scenario A with PhLSTT as TimingMaster and DUT as TimingSlave an efficient compensation method is introduced to reduce the impact of the reflection on the measured data signal.

The operation in this scenario is as follows:

- The PhLSTT generates the network timing.
- The TimingMaster clock is generated from a crystal in the PhLSTT.
- The DUT recovers the Timing Master clock received from the PhLSTT.

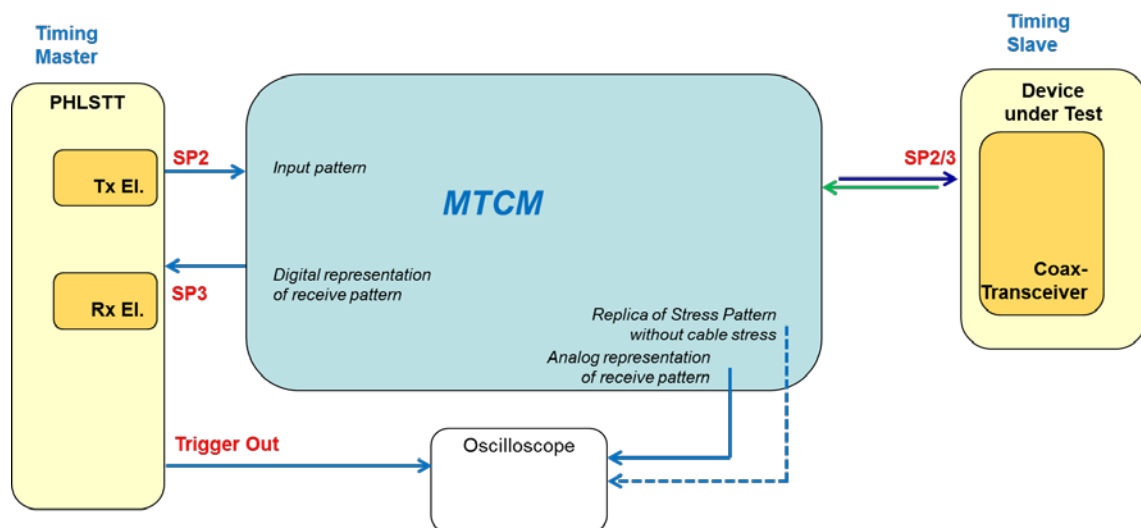


Figure 8-2: Test Setup 2 (DUPLEX) - DUT as TimingSlave

For the reflection compensation the reflection pattern need to be acquired:

- The PhLSTT sends the test pattern through the MCTM to the DUT.
- The Timing Master clock is created from the PhLSTT crystal.
- The DUT is kept unpowered. A resistive termination on the DUT is available in unpowered mode. Therefore the appropriate reflection based on the mismatches of the Setup and the particular DUT will be produced.
- In this configuration, the MOST network is “open”, the PhLSTT works in pattern generator mode.
- The reflection pattern can be measured through the directional coupler of the MCTM and will be stored as a waveform on the scope.
- Averaging is recommended for the reflection pattern measurement.
- Measurement is triggered off by the start of pattern signal from PhLSTT.



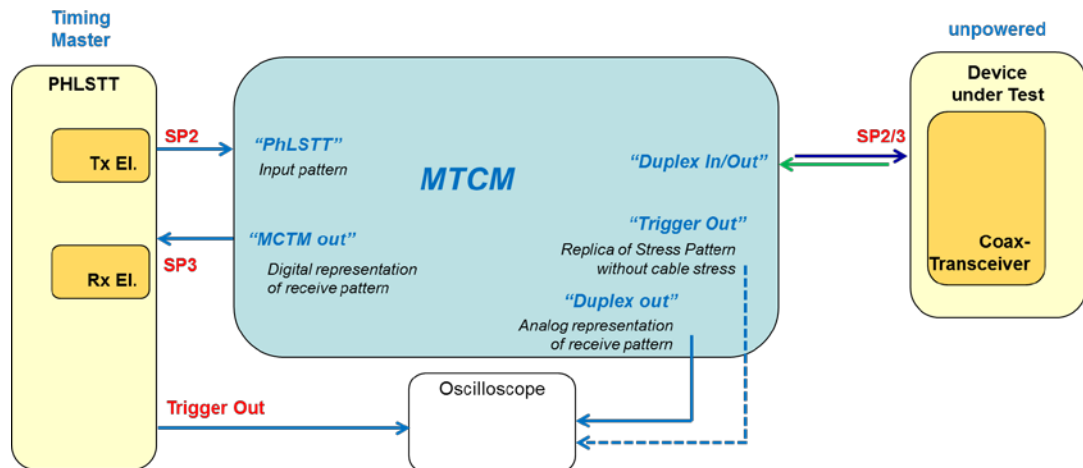


Figure 8-3: Test Setup 2 (DUPLEX) – acquisition of reflection pattern

In normal operation (DUT powered, DUT in retimed bypass mode, ring is closed), The SP2 pattern visible on the scope is overlaid with the reflections. During Compliance testing, with test pattern applied and measurement again triggered off by the start of pattern Signal, the previous reflection pattern can be subtracted from the SP2 data pattern.

## 8.2.2 Scenario B: DUT as Timing Master

In scenario B the PhLSTT acts as the TimingSlave and the DUT as the TimingMaster.

The operation in this scenario is as follows:

- The DUT generates the network timing.
- The TimingMaster clock is generated from a crystal in the DUT.
- The PhLSTT recovers the TimingMaster clock received from the DUT.

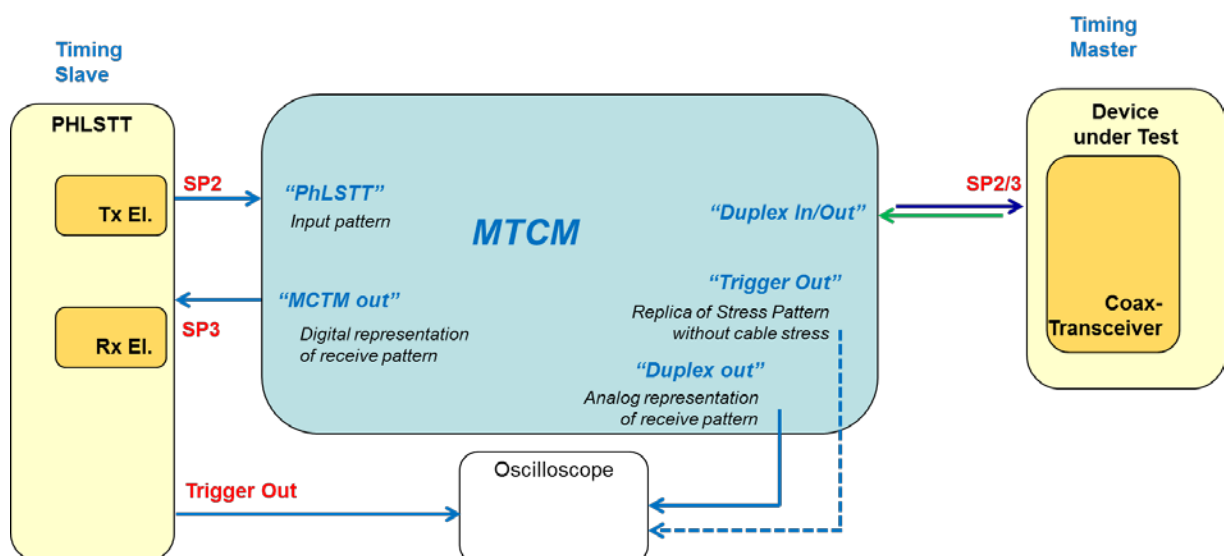


Figure 8-4: Test Setup 2 (DUPLEX) - DUT as TimingSlave

For the reflection compensation the reflection pattern is acquired and pre-processed:

**MOST150 cPhy Compliance Verification Procedure – Physical Layer Errata4**

- The PhLSTT will be set to TimingMaster mode, the TimingMaster clock is created from the PhLSTT crystal.
- The PhLSTT sends the test pattern through the MCTM to the DUT.
- The DUT is kept unpowered. A resistive termination on the DUT is available in unpowered mode. Therefore the appropriate reflection based on the mismatches of the setup and the particular DUT will be produced.
- In this configuration, the MOST network is “open”, the PhLSTT works in pattern generator mode.
- The reflection pattern can be measured through the directional coupler of the MCTM and will be stored as a waveform on the scope.
- The measurement is triggered off the start of pattern signal from the PhLSTT.
- Averaging is recommended for the reflection pattern measurement.

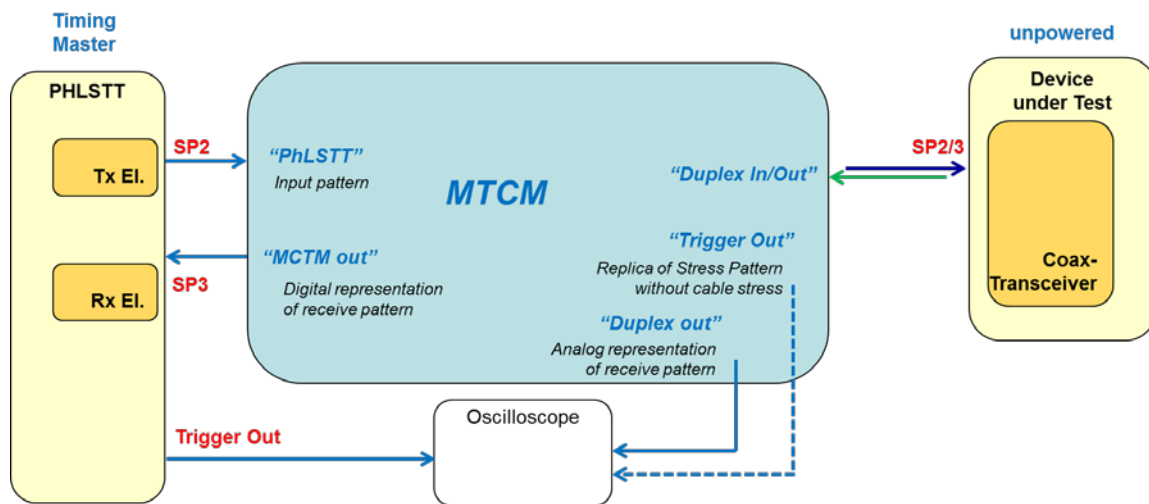


Figure 8-5: Test Setup 2 (DUPLEX) – acquisition of reflection pattern

Additionally and before starting the test of the DUT:

- The stress pattern from the PhLSTT is additionally acquired at the “Trigger Out” connector of the MCTM for timing reference purposes.
- Both acquisitions should be taken at the same time and with same trigger (one-shot). If averaging is used (recommended), the last acquisition of PhLSTT stress pattern shall be stored.

Back in normal operation (DUT powered, DUT in retimed bypass mode, DUT as TimingMaster, PhLSTT as TimingSlave, ring is closed), the stress pattern produced by the PhLSTT follows the network clock (derived from the DUT). The previously measured reflection pattern however is based on crystal /reference clock from the PhLSTT. This requires to process a resampling procedure on the reflection pattern to transfer it to the DUT's network clock time base.

Resampling adjusts the time axis of the pattern measured with the PhLSTT crystal time base to that of the DUT's crystal. (Reference clock frequency deviations are tolerated up to 200ppm).

During Compliance testing, resampling procedure needs to be operated for each acquisition of DUT Data Signal!

- Acquire Data
- Resample procedure
- Apply resampled reflection on Acquired Data
- Analyze data (TIE, Eye, rise time, etc.)
- Repeat from a) ... [if needed]

*NOTE: Performing the resampling procedure once on an initial DUT reference acquisition showed low efficiency in the compensation performance. This is caused by the bit rate detection which is part of the TIE process (TIE in oscilloscope, similar process is performed in Resample SW). The number of acquired transitions is too low for a stable frequency measurement. Repeated acquisitions show minor variation in bit rate of the same DUT. This causes the resampled reflection pattern to not perfectly match the reflection on the acquired pattern.*

Resampling can be achieved by an external SW application (external from oscilloscope SW but can run on the scope PC).

## 9 Appendix E: Test Procedure 2-Port Nodes

### Additional information to Section 3.1 - Enhanced test setups for 2-port nodes

Daisy chain topology involve nodes providing 2 ports. For testing such nodes, the test setup and test procedure as known from single port nodes and described in section 3.1 need to be adapted.

Port 0 testing follows procedures shown in section 3.1 for single port nodes. During this test, port 1 needs to be left unconnected.

For port 1 testing a modified test setup and an enhanced test procedure are required. The modifications are applicable for both modes of operation, SIMPLEX and DUPLEX. Figure 9-1 and Figure 9-2 depict the modified test setups for port 1 testing:

- connect port 0 to PHLSTT optical port of PHLSTT through an optical-to-coaxial converter
- optical PHLSTT port is used to configure the test and to provide timing reference to the DUT for the whole test cycle
- during configuration phase, port 1 needs to be kept inactive, no input data at port 1
- during test phase, PHLSTT provides stress pattern
  - o port 0 receives stress pattern over an unstressed link
  - o port 1 receives stress pattern over stressed link according to the test plan

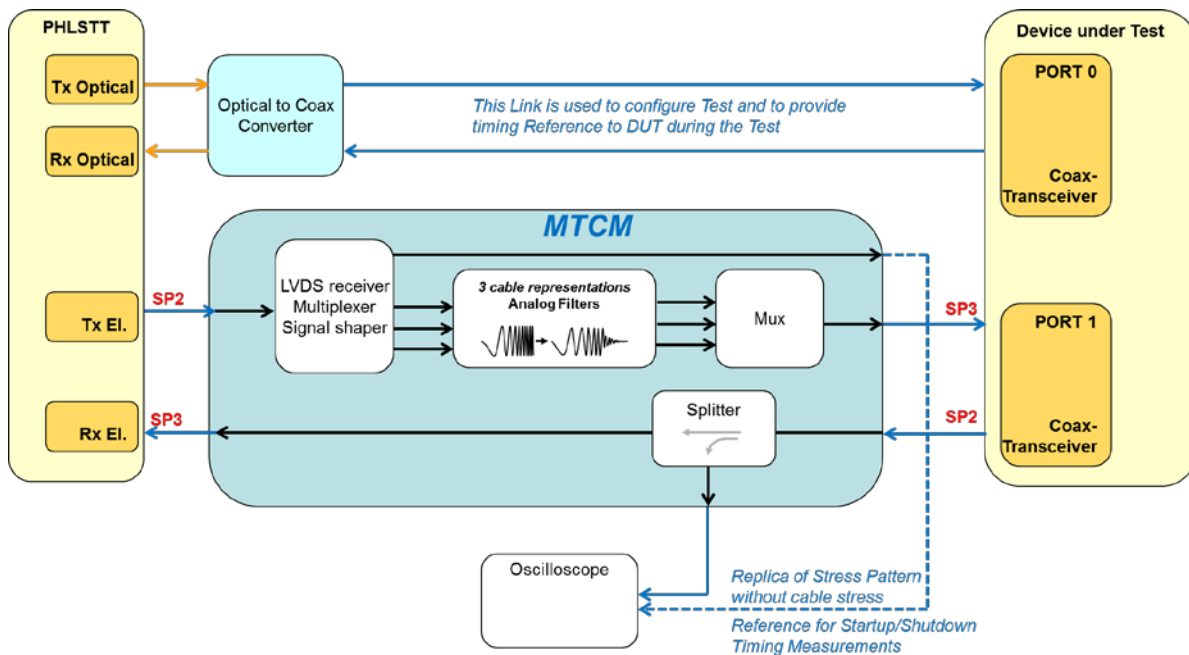


Figure 9-1: Test Setup 1 (SIMPLEX, 2-port) for Limited Physical Layer Compliance test

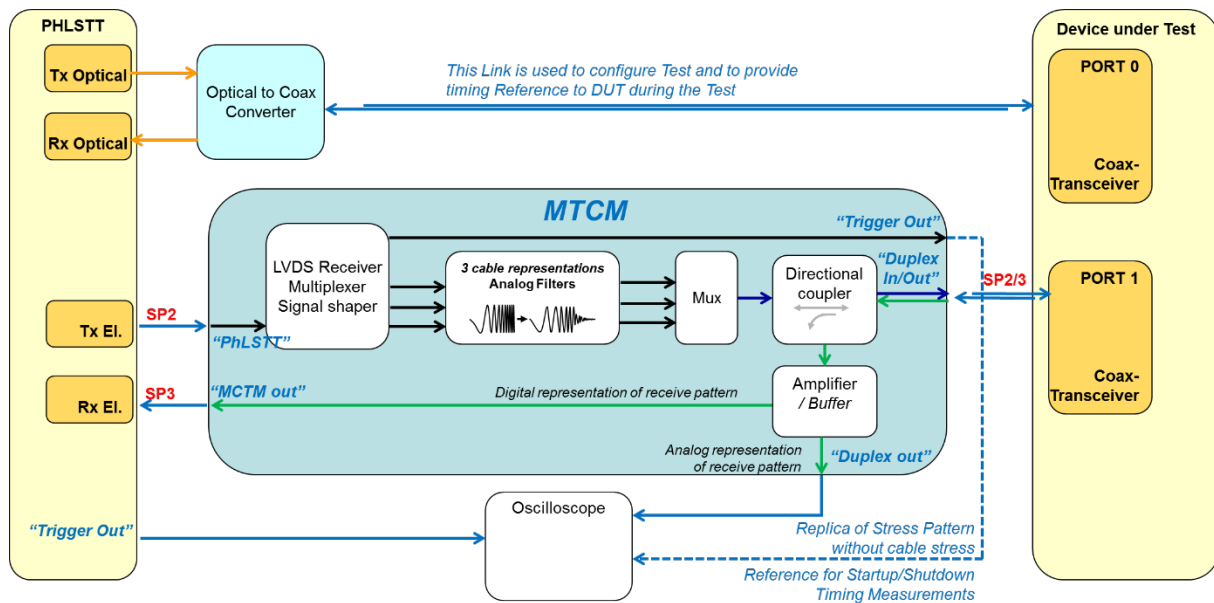


Figure 9-2: Test Setup 2 (DUPLEX, 2-port) for Limited Physical Layer Compliance test

### **Additional information to section 3.4 - Enhanced test flow for 2-port nodes**

Test flow of port 0 of a 2-port node follows exactly the flow shown for single port nodes. Figure 9-3 depicts an overview of the test flow.

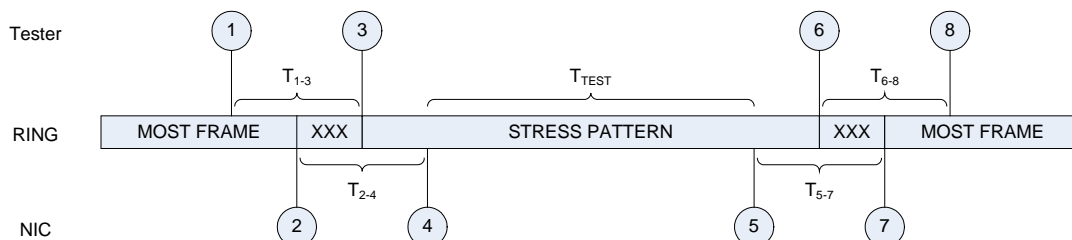


Figure 9-3: Test Flow Overview (2-port, port0)

- 1 – PhLSTT sends command to DUT port 0 over MOST (FBlock 0x0A - ExtendedNetworkControl ENC) to enter Test Mode, port 1 is left unconnected.
- 2 – DUT enters Retimed Bypass Mode for port 0.
- 3 – PhLSTT starts transmitting the Stress Pattern.
- 4 – DUT clears the Error Counter and Lock Log for port 0.  
... PHYSICAL LAYER STRESS TESTING...
- 5 – DUT reads back Error Counter and Lock Log for port 0.
- 6 – PhLSTT switches to MOST communication mode.
- 7 – DUT switches back to its original MOST mode.
- 8 – PhLSTT reads back the result via port 0.

Test flow of port 1 of a 2-port node is based on above test flow but with modifications:

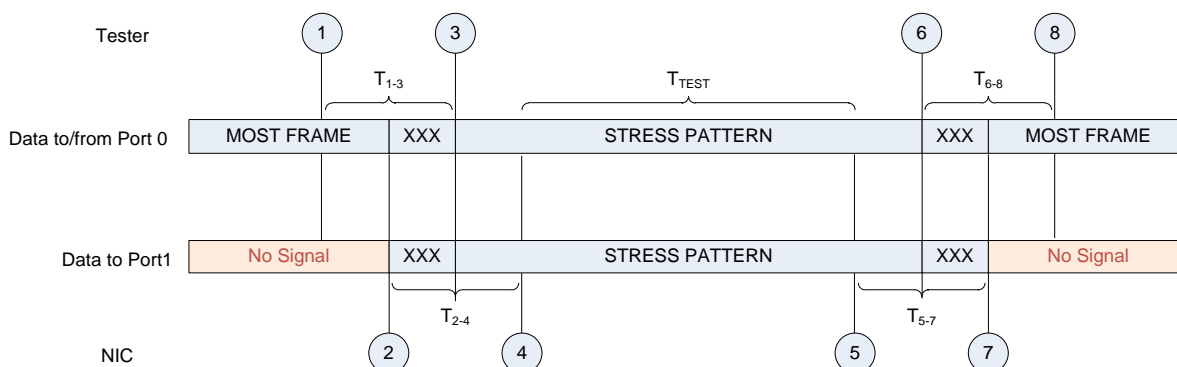


Figure 9-4: Test Flow Overview (2-port, port1)

- 1 – PhLSTT sends command to DUT port 0 over MOST (FBlock 0x0A - ExtendedNetworkControl) to enter test mode from port 1.
- 2 – DUT enters Retimed Bypass Mode for port 1.
- 3 – PhLSTT starts transmitting the Stress Pattern to both DUT ports.
- 4 – DUT clears the Error Counter and Lock Log for port 1.  
... PHYSICAL LAYER STRESS TESTING...
- 5 – DUT reads back Error Counter and Lock Log for port 1.
- 6 – PhLSTT switches to MOST communication mode.
- 7 – DUT switches back to its original MOST mode.
- 8 – PhLSTT reads back the port 1 result via port 0.

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