

MOST

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST150 Compliance Measurement
Guideline
Draft Rev 1.0
10/2015**

MOSTCO CONFIDENTIAL

See page 3 for the terms of disclosure



Legal Notice

COPYRIGHT

© Copyright 1999 - 2015 MOST Cooperation. All rights reserved.

LICENSE DISCLAIMER

Nothing on any MOST Cooperation Web Site, or in any MOST Cooperation document, shall be construed as conferring any license under any of the MOST Cooperation or its members or any third party's intellectual property rights, whether by estoppel, implication, or otherwise.

CONTENT AND LIABILITY DISCLAIMER

MOST Cooperation or its members shall not be responsible for any errors or omissions contained at any MOST Cooperation Web Site, or in any MOST Cooperation document, and reserves the right to make changes without notice. Accordingly, all MOST Cooperation and third party information is provided "AS IS". In addition, MOST Cooperation or its members are not responsible for the content of any other Web Site linked to any MOST Cooperation Web Site. Links are provided as Internet navigation tools only.

MOST COOPERATION AND ITS MEMBERS DISCLAIM ALL WARRANTIES WITH REGARD TO THE INFORMATION (INCLUDING ANY SOFTWARE) PROVIDED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT. Some jurisdictions do not allow the exclusion of implied warranties, so the above exclusion may not apply to you.

In no event shall MOST Cooperation or its members be liable for any damages whatsoever, and in particular MOST Cooperation or its members shall not be liable for special, indirect, consequential, or incidental damages, or damages for lost profits, loss of revenue, or loss of use, arising out of or related to any MOST Cooperation Web Site, any MOST Cooperation document, or the information contained in it, whether such damages arise in contract, negligence, tort, under statute, in equity, at law or otherwise.

FEEDBACK INFORMATION

Any information provided to MOST Cooperation in connection with any MOST Cooperation Web Site, or any MOST Cooperation document, shall be provided by the submitter and received by MOST Cooperation on a non-confidential basis. MOST Cooperation shall be free to use such information on an unrestricted basis.

TRADEMARKS

MOST Cooperation and its members prohibit the unauthorized use of any of their trademarks. MOST Cooperation specifically prohibits the use of the MOST Cooperation LOGO unless the use is approved by the Steering Committee of MOST Cooperation.

SUPPORT AND FURTHER INFORMATION

For more information on the MOST technology, please contact:

MOST Cooperation

Administration
Emmy-Noether-Str. 14
D-76131 Karlsruhe
Germany

Tel: (+49) (0) 721 966 50 00

E-mail: contact@mostcooperation.com

Web: www.mostcooperation.com



This Specification is Confidential Information of the MOST Cooperation. It may only be disclosed to member companies. Member companies wishing to discuss these Specifications with suppliers or other third parties must ensure that a commercially standard form of non-disclosure agreement has been previously executed by the party receiving such Specifications. Use of these Specifications may only be for purposes for which they are intended by the MOST Cooperation. Unauthorized use or disclosure is a violation of law.

© Copyright 1999 - 2015 MOST Cooperation
All rights reserved

MOST is a registered trademark

Contents

BIBLIOGRAPHY	6
DOCUMENT HISTORY	7
TERMINOLOGY AND ABBREVIATIONS	8
1 GENERAL REMARKS.....	9
1.1 Introduction.....	9
1.2 Operating Conditions	9
1.3 Measurement Tools, Requested Accuracy	10
2 ELECTRICAL CHARACTERISTICS	11
2.1 Test according to LVDS	11
2.2 Test according to LVTTTL.....	11
3 SPECIFIC CHARACTERISTICS FOR COAXIAL INTERFACES AND COMPONENTS	12
3.1 High / Low Detection @SP2	12
3.2 Transition times @SP2	13
3.3 Steady State Amplitude @SP2	13
3.4 Attenuation of Coaxial Interconnect	13
3.4.1 Impact of Attenuation on Data Signal	17
3.5 Return Loss of connectors and couplers	18
3.6 Characteristic impedance of coaxial cable.....	18
3.7 Return Loss of Coaxial Interconnect	18
3.8 Return Loss of PCB Interfaces	20
3.9 Creating a Stimulus for SP3.....	22
3.9.1 Creating a Stimulus for SP3 for Simplex Applications	22
3.9.2 Creating a Stimulus for SP3 for Duplex Applications.....	24
4 MEASUREMENT OF PHASE VARIATION.....	27
4.1 Basics.....	27
4.2 Measuring Alignment Jitter.....	29
4.3 Measuring Transferred Jitter	32
5 TEST SETUPS.....	34
5.1.1 Setups for Dual Simplex.....	36
5.1.1.1 SP2 Signal Quality Measurement for Simplex	36
5.1.1.2 SP4 Jitter Measurement (A_j & T_j) for Simplex	37
5.1.2 Setups for Duplex.....	39
5.1.2.1 Directional Couplers	39
5.1.2.2 SP2 Signal Quality Measurement for Duplex.....	41
5.1.2.3 SP4 Jitter Measurement (A_j & T_j) for Duplex.....	42
6 POWER UP / POWER DOWN.....	44
6.1 General considerations	44
6.2 Measuring ECC Parameters	45
6.2.1 Measuring ECC Parameters – Test Setup.....	45
6.2.2 Measuring ECC Parameters – Signal Charts	46
6.2.3 Measuring ECC Parameters – Test sequences.....	47
6.2.3.1 ECC Test Sequence #1 - OFF-to-ON by SP1 Signal.....	47
6.2.3.2 ECC Test Sequence #2 - OFF-to-ON by SP1 Signal.....	48
6.2.3.3 ECC Test Sequence #3 - ON-to-OFF by SP1 Signal.....	49
6.2.3.4 ECC Test Sequence #4 - OFF-to-ON by SP1 Signal.....	50
6.2.3.5 ECC Test Sequence #5 - ON-to-OFF by SP1 Signal.....	51
6.2.3.6 ECC Test Sequence #6 - OFF-to-ON by /RST Signal	52
6.2.3.7 ECC Test Sequence #7 - ON-to-OFF by /RST Signal	53
6.3 Measuring CEC Parameters	54

6.3.1	Measuring CEC Parameters – Test Setup.....	54
6.3.2	Measuring CEC Parameters – Signal Charts	56
6.3.3	Measuring CEC Parameters – Test sequences.....	57
6.3.3.1	CEC Test Sequence #1 - OFF-to-ON	57
6.3.3.2	CEC Test Sequence #2 - OFF-to-ON	58
6.3.3.3	CEC Test Sequence #3 - OFF-to-ON	59
6.3.3.4	CEC Test Sequence #4 - OFF-to-ON	60
6.3.3.5	CEC Test Sequence #5 - ON-to-OFF	61
6.3.3.6	CEC Test Sequence #6 - OFF-to-ON	62
6.3.3.7	CEC Test Sequence #7 - ON-to-OFF	63
7	DETECTING BIT RATE (FREQUENCY REFERENCE)	64
8	SYSTEM PERFORMANCE	65
8.1	SP4 Receiver Tolerance	65
8.2	Master Delay Tolerance	66
APPENDIX A: TBD		68
APPENDIX B: LIST OF FIGURES		69
APPENDIX C: LIST OF TABLES		70

Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

Document		Revision
[1]	MOST Specification	3.0
[2]	MOST Basic Physical Specification	1.0
[3]	MOST150 cPhy Automotive Physical Layer Sub-Specification	1.1
[4]	MOST Compliance Requirements	2.0

MOST Document references

Document		Revision
[5]	IEC 60958-3 Digital audio interface - Part 3: Consumer applications	2006
[6]	TIA/EIA-644-A-2001 Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	2001
[7]	JEDEC No. JESD8C.01 Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits	
[8]	EN50289-1-8 Communication cables - Specifications for test methods Part 1-8: Electrical test methods - Attenuation	2002
[9]	EN50289-1-11 Communication cables - Specifications for test methods Part 1-11: Electrical test methods – Characteristic impedance, input impedance, return loss	2002
[10]	ISO 20860-2 Road vehicles - 50Ohm impedance radio frequency connection system interface - Part 2: Test procedures	2009

Other Documents

Document History

Revision 0.1

Change Ref.	Chapter	Changes
0V1_001	All	Initial draft version.

Terminology and Abbreviations

Abbreviation	Explanation
AFE	Analog Frontend
AJ	Alignment Jitter
AWG	Arbitrary Waveform Generator
CTR	Coaxial Transceiver
CEC	Coaxial Electrical Converter
CE _{port}	Coaxial Electrical port (combination of AFE and CEC)
ECC	Electrical Coaxial Converter
EC _{port}	Electrical Coaxial port (combination of AFE and ECC)
NIC	Network Interface Controller
NI	Network Interface
PG	Pattern Generator
PLL	Phase Lock Loop
SDA	Serial Data Analyzer
SMD	Surface Mount Device
SP	Specification Point
TJ	Transferred Jitter
UI	Unit Interval

1 General Remarks

1.1 Introduction

This document *MOST150 cPhy Compliance Measurement Guideline* specifies basic measurement methods, relevant for verifying compatibility of networks, nodes, modules, and components with the requirements specified in the documents *MOST Basic Physical Specification [2]* and *MOST150 cPhy Automotive Physical Layer Sub-Specification [3]*.

This document shows basic measurement principles and setups for all specified parameters in [3]. There might be other options for determining parameters, which are more suitable for characterization and end-of-line testing in the supply chain. Selection and definition of an appropriate test strategy is in the responsibility of the supplier. However, all used measurement procedures shall provide measurement traceability to the basic principles shown in this document.

For the majority of parameters, the specification [3] is defined as an interface specification. Parameters and the requested performance ranges are stated for components sending into the interface. The same performance ranges need to be considered as input tolerances for components being connected to the interface as receiver. For verification of output performance of a component that sends into an interface, the input variations have to be considered – if they exist.

The process of compliance verification is defined in the MOST document *MOST Compliance Requirements [4]*. It describes how to achieve compliance certification for MOST subsystems (devices) and components.

For documentation clarity some values of MOST150 cPhy Automotive Physical Layer Sub-Specification [3] are used within this document. In case of discrepancies with the MOST150 cPhy Automotive Physical Layer Sub-Specification [3], the MOST150 cPhy Automotive Physical Layer Sub-Specification [3] shall be deemed the controlling document.

1.2 Operating Conditions

Temperature range for modules or components $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ according to [3].

Voltage range for modules or components $3.3\text{ V} \pm 5\%$ according to [3].

Note that there are functional requirements for the ECC within an extended voltage supply range according to [3].

1.3 Measurement Tools, Requested Accuracy

State-of-the-Art Tools:

- **Digital Oscilloscope**
 - DSO Type
 - ≥ 10 GS/s
 - BW ≥ 1.5 GHz
 - Sampling Memory ≥ 10 MSample
 - Active Probe (single-ended, differential)
- VNA (Vertical Network Analyzer) or alternatively TDR (Time-Domain Reflectometer)
- **Ampere meter:**
 - Accuracy: better than 2 μ A
 - Optionally, Trigger input (for timing measurements)
- **Pattern generator for generating MOST150 stress pattern:**
 - BW 300 Mbit/s
 - Trigger output (for timing measurements)
- **Directional coupler** (for Duplex Setups only)
 - Required performance levels are discussed in chapter 5.1.2.1

Note: Depending on the chosen test-method and method to generate stimuli for the test, further equipment may be needed (e.g. electrical attenuator, discrete filter module to emulate cable transfer function, etc.). Performance requirements of such equipment need to be decided based on the particular use case. Performance variation of such equipment and impact on measurement results due to that, need to be considered.

2 Electrical characteristics

2.1 Test according to LVDS

Testing of devices, modules, or components has to be performed according to the measurement methods and setups specified in [6]. Parameters and their respective limits are derived from [6], with the exceptions defined in [3].

The parameters subject to those exceptions must only comply with limits set by [3] for the purpose of MOST150 cPhy Automotive Physical Layer Sub-Specification [3] compliance. Measurement methods for those parameters are the ones indicated in [6].

2.2 Test according to LVTTTL

Testing of devices, modules, or components has to be performed according to [7].

3 Specific characteristics for Coaxial Interfaces and components

3.1 High / Low Detection @SP2

The cPhy system is not intentionally creating overshoots, nor is excessive ringing expected at SP2-interfaces. Therefore, a state-of-the-art High / Low level detection provided by the majority of the oscilloscopes is expected to yield reliable results with sufficient level of repeatability. However, to ensure non-ambiguous measurements the method described below is recommended and will be applied as a reference procedure to resolve possible discrepancies.

To determine High/Low levels, the MOST150 stress pattern shall be used. At least 500 4UI, 5UI- or 6UI-pulses need to be extracted out of the measured data. Extraction can be done by triggering on pulse-width ranges or by software based selection on a prior acquired waveform. “High” is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired high-pulses. “Low” is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired low-pulses. t_{OSLS} and t_{OSLE} are defined in [3] and shown in Table 3-1.

Measurement Region	Value	Unit
t_{OSLS}	1.00	UI
t_{OSLE}	3.000	UI

Table 3-1: Signal Level Measurement Interval

The measured amplitudes “High” and “Low” are an integral part of further measurements at SP2.

Figure 3-1 provides an example of suggested High / Low detection method

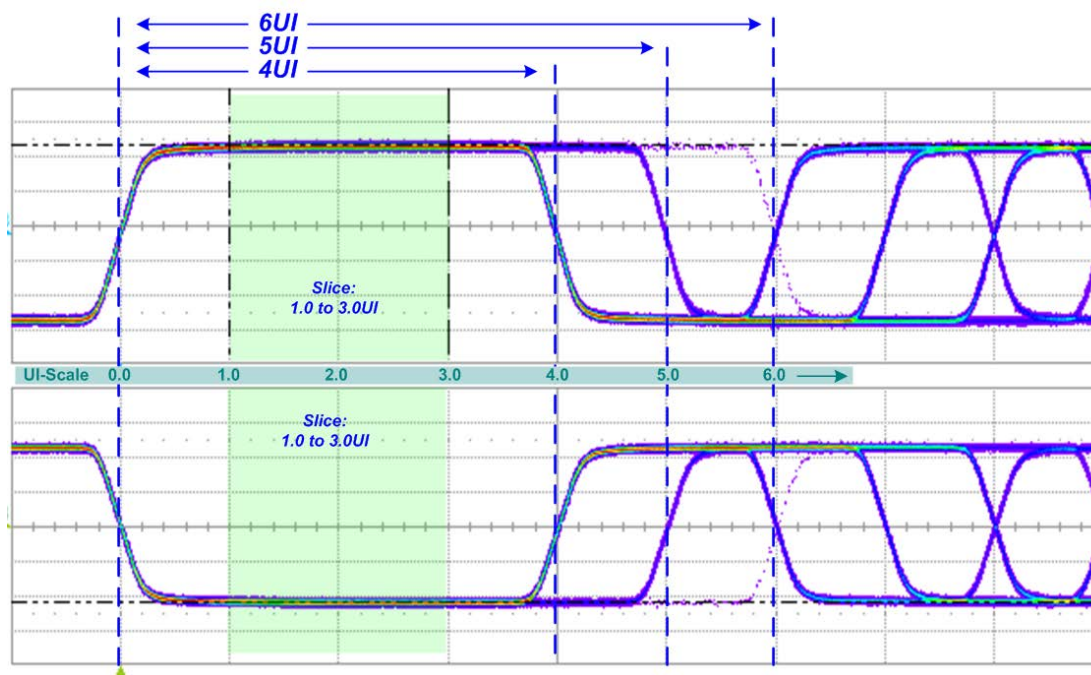


Figure 3-1: Detection of “high” and “low”

3.2 Transition times @SP2

In cPhy systems at SP2 interfaces, overshoots and excessive ringing are not expected. Therefore, a state-of-the-art 20%-80% Transition Time detection, provided by the majority of the oscilloscopes is expected to yield reliable result. However, to ensure non-ambiguous measurements the method described below is recommended and will be applied as a reference procedure in case of discrepancies.

The transition times (rise and fall) are detected as the time of an edge when transitioning through the level range of 20% and 80% of the amplitude. Therefore, High/Low detection needs to be performed beforehand (see section 3.1).

The amplitude threshold levels are given:

$$20\% - \text{threshold} = [(High - Low) * 0.2] + Low$$

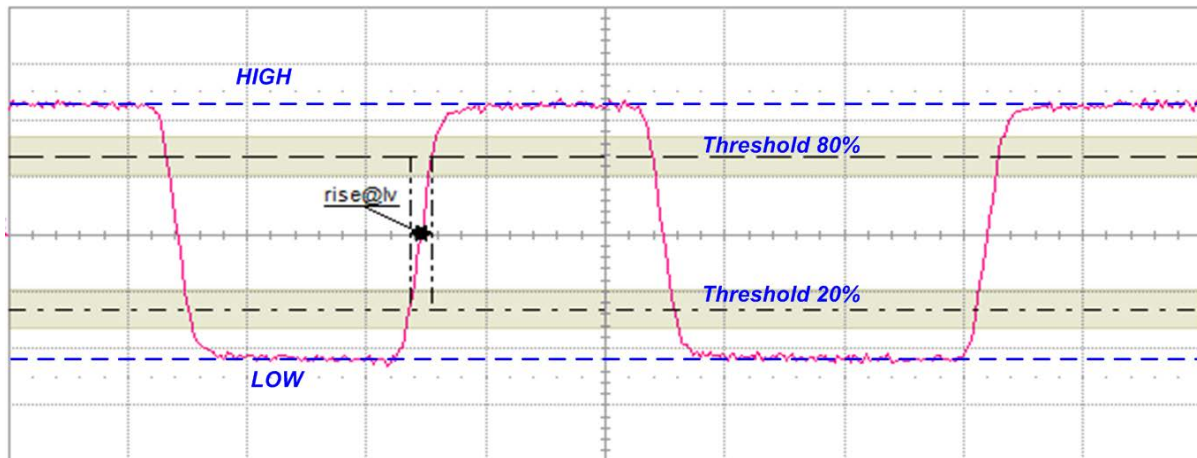
$$80\% - \text{threshold} = [(High - Low) * 0.8] + Low$$


Figure 3-2: Example for detection of rise-time

Measured transition times have to be within the specified limit in [3]. It is recommended to use the MOST150 stress pattern as data signal.

3.3 Steady State Amplitude @SP2

Following the method in section 3.1 of determining High- and Low –State of, the steady state Amplitude is the difference between High and Low.

3.4 Attenuation of Coaxial Interconnect

MOST cPhy specifies the attenuation requirements for a Coaxial Interconnect, formed of one or more cable pieces and the associated couplers and harness connectors. The total length of the Interconnect is limited to a maximum of 15m. The attenuation of such an Interconnect is frequency dependent. The MOST150 cPhy Automotive Physical Layer Sub-Specification [3] document specifies an idealized, frequency dependent attenuation function with 2 coefficients (DCloss, Fskin).

$$Attenuation(f) = -DC_{loss} - \sqrt{\frac{f}{f_{skin}}}$$

Attenuation requirements are limited to the frequency range between 1MHz and 450MHz and the absolute attenuation is allowed to vary, as long as specific requirements (described in the table below) are met.

For evaluating Coaxial Interconnects or components used in such interconnects, the following two requirements need to be verified:

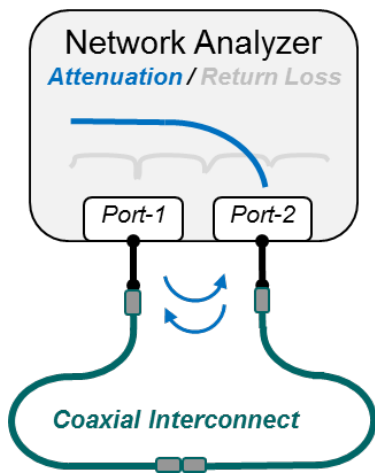
- [Req #1] Coefficient values calculated (as described below) based on attenuation measurements for the Interconnect under test shall be within specified range ($DC_{loss} < 0.5\text{dB}$, $F_{skin} > 9.2 \cdot 10^6$).
- [Req #2] With the evaluated coefficients and the given Attenuation function, an idealized Attenuation Curve can be constructed, which approximates the characteristics of the measured Interconnect. The difference between data-points of the constructed and the measured attenuation curve (residues) shall be smaller than $\pm 1\text{dB}$ (Attenuation Conformance)

Attenuation requirements described above must be guaranteed for the complete temperature range, automotive environmental conditions and over lifetime.

Note: Although attenuation always reduces signal strength, Attenuation in cPhy is specified with positive values (e.g. $DC_{loss} < 0.5\text{dB}$). The negative sign of the parameter is covered with the term "Attenuation". Measurement Equipment (like VNA) most likely will produce negative values instead. Following plots show Attenuation with positive values, to better fit with the way the specification is done.

Test-Procedure:

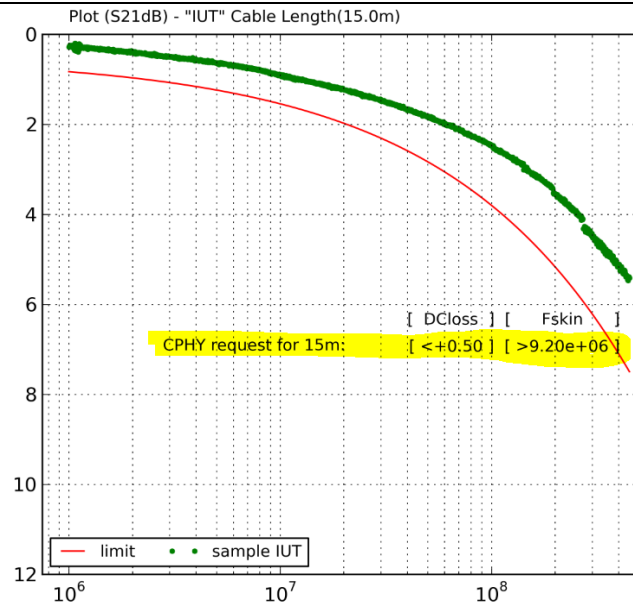
The following table shows the sequence of actions based on an example:

<p>[A] Test Setup</p> <p>The test procedure starts with the measurement of the attenuation characteristic over frequency for an Interconnect Under Test (IUT).</p> <p>This is usually done with a Network Analyzer, using a 2-Port arrangement. The Network Analyzer measures Attenuation from port-1 to port-2 and vice versa.</p> <p>The frequency sweep shall produce at least 40 data points per decade, logarithmically distributed.</p> <p>The measurement procedure shall be performed according to [8]</p>	
---	--

[B] Data Acquisition:

green: acquired data in frequency range 1MHz - 450MHz

red curve marks the cPhy spec. limits: idealized Attenuation characteristic based on worst case coefficients DCloss, Fskin (worst case coefficient values highlighted)



[C] Data Fitting:

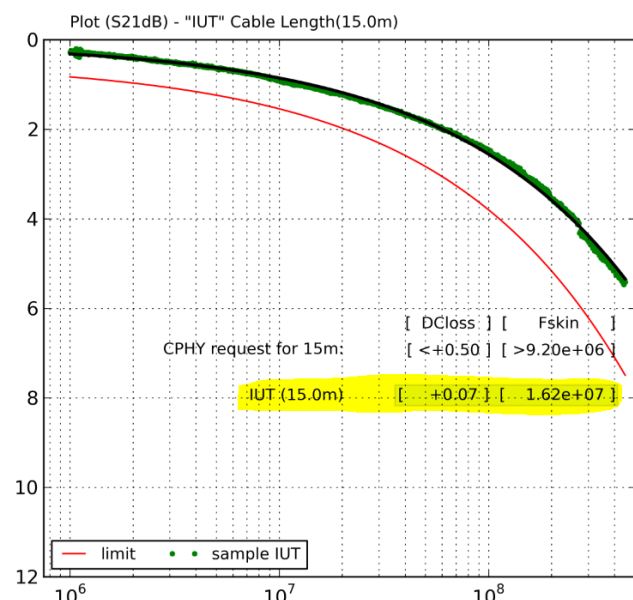
The measured data then are fitted to the given Attenuation function, resulting in values for DCloss and Fskin.

For Parameter fitting, primarily least square fitting algorithm is used. A set of data {xi, yi} as well as a model function, $y = f(x, p)$, need to be provided; p is a vector of parameters ($p=[DCloss, Fskin]$) for the model that need to be found.

The algorithm determines the parameter vector that gives the best fit to the data by minimizing the sum of squares of the residuals.

Highlighted: Calculated coefficients for the example IUT. Those coefficients must be within the limits set by [3] otherwise the IUT is not compliant!

black curve: idealized attenuation curve approximating the measured performance of the IUT (Attenuation function, with coefficients as determined by the fit). Attenuation indicated by the idealize curve (black) must be less than worst case attenuation curve (red)



[Req #1]

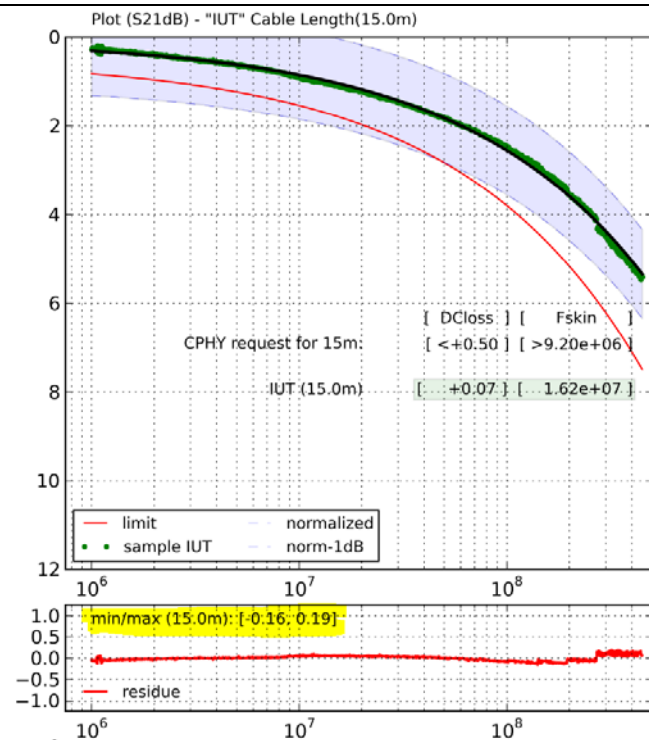
Evaluated coefficients are within specified ranges ✓

[D] Attenuation Conformance

blue area: shows the attenuation conformance corridor, ± 1 dB, around the idealized Attenuation curve for this specific IUT. All the measured sample points (green) must be within that area.

The graph on the bottom shows the residues. Residues, in this context, mean the deviation of measured samples to the idealized curve for every frequency step.

Highlighted: min/max values for Residues found in the population. Those must be within the limits set by [3] otherwise the IUT is not compliant!



[Req #2]

Residues are inside the specified corridor ✓

Note:

The DCloss and FSkin coefficient limits restrict the allowed attenuation span.

The attenuation conformance corridor ensures that the transfer characteristic of the IUT follows closely a transfer function of standard coax-cables. As a result signal passing such interconnect and being consecutively equalized (based on standard coax-cable attenuation function) will maintain a flatness of ± 1 dB.

Particular coaxial interconnect configuration exhibits individual attenuation characteristics and is thus characterized by their respective individual DCloss and FSkin coefficients. The values of those coefficients depend on the cable type used and the total length of each specific interconnects tested. Coaxial interconnect/segments with shorter length have lower attenuation and therefore lower DCloss and larger Fskin. Interconnects with identical configuration, may produce slightly different coefficient sets.

Cable Attenuation varies with temperature. This is mainly contributed to the temperature dependent conductance of the conductor's material (copper). Therefore coefficients for a given Interconnect will vary over temperature. When measuring IUT only at room temperature, margin for full temperature range needs to be considered.

When measuring coaxial interconnects shorter than the maximum length of 15m, evaluated coefficients can be extrapolated to max length. Vice versa, also shorter link attenuation performance can be estimated by extrapolating the coefficients to shorter length.

Extrapolation of coefficient values for various cable length:

DCloss_meas : DCloss, as result of a fit on measured data

Fskin_meas : Fskin, as result of a fit on measured data

Length_DUT : length of measured Interconnect

L : desired length, coefficients are extrapolated to

$$DCloss(L) = DCloss_meas / Length_DUT * L$$

$$Fskin(L) = Fskin_meas / L^2 * Length_DUT^2$$

Example, using coefficient limits

Length_DUT	15	extrapolated --> L	5
DCloss_meas	0,500	Dcloss(L)	0,167
Fskin_meas	9,20E+06	Fskin(L)	8,28E+07

measured == ==> extrapolated

Length_DUT	5	extrapolated --> L	15
DCloss_meas	0,167	Dcloss(L)	0,500
Fskin_meas	8,28E+07	Fskin(L)	9,20E+06

3.4.1 Impact of Attenuation on Data Signal

As specified in section 6.3.1 of [3], the attenuation characteristic of Coaxial Interconnect follows a function of frequency. Therefore, the spectrum of a Data Signal being fed into such channel will be attenuated in a non-uniform manner. Attenuation on higher frequencies will stronger than on lower frequencies. In consequence, transition times will slow down (as they are controlled by the higher components of the relevant spectrum of the data signal). Shorter pulses of the signal may not achieve full amplitude swing anymore. The effect is usually described as Inter-Symbol-Interference (ISI).

The graph in Figure 3-3 gives an example: The SP2-signal (yellow) starts with uniform amplitude on all pulses (V_{ss2} in section 6.2 of [3]). The SP3-Signal (green) shows the resulting signal shape after having past the Coaxial Interconnect (typical Coax Cable, 15m, same cable as used for analysis of link attenuation in section 3.4).

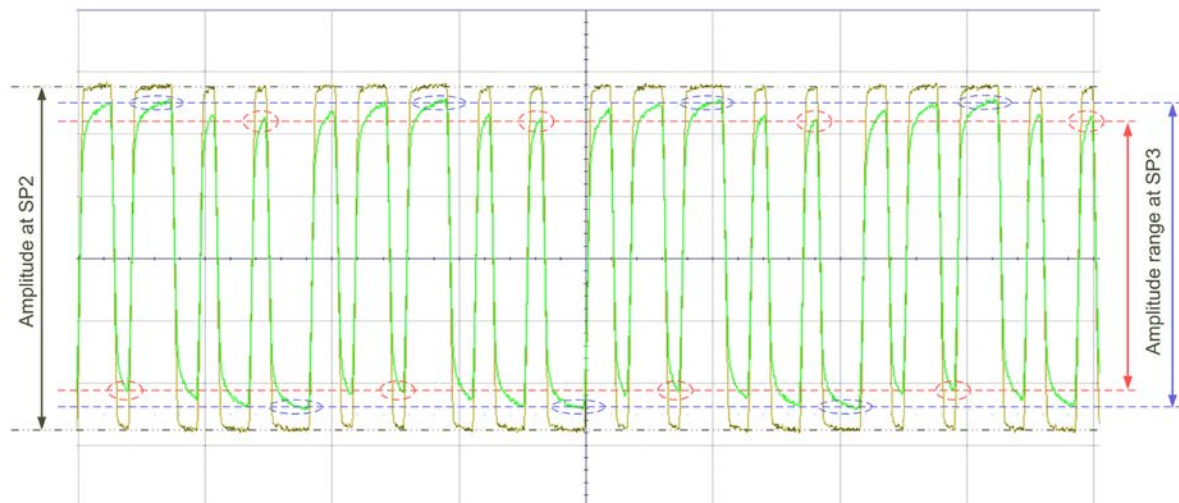


Figure 3-3: Measurement Setup for evaluation Return Loss of coaxial interconnects

3.5 Return Loss of connectors and couplers

This covers all type of connectors in the coaxial link, Inline-couplers, Harness connectors as well as ECU-connectors. Testing of such connectors and couplers shall be performed according to [10]. The Frequency Range of interest for MOST cPhy is defined with 1MHz to 450MHz, which is only a sub-set of the requested bandwidth in [10].

3.6 Characteristic impedance of coaxial cable

Measurement of characteristic impedance of coaxial cables shall be performed according to [9].

3.7 Return Loss of Coaxial Interconnect

A Coaxial Interconnect is formed of one or more cable pieces and the associated couplers and harness connectors. Return Loss of a Coaxial Interconnect characterizes the frequency dependent signal reflection ratio, due to accumulated impedance mismatch throughout the whole length of that interconnect, measured at each of its ends.

Return Loss shall be measured according to [9] in the frequency range of 1MHz to 450Mhz. MOST150 cPhy does not specify specific requirements in resolution or scale of the frequency axis for RL. It is solely in the responsibility of the supplier to apply appropriate settings.

Typically the RL measurement is combined with the Attenuation measurement. The Coaxial Interconnect characteristic is measured in a 2-Port arrangement. The Network Analyzer measures Attenuation and Reflection from both ports.

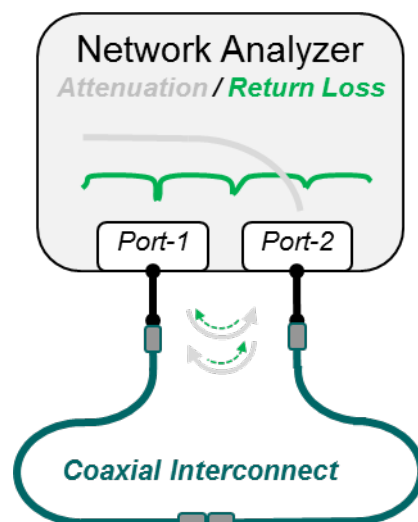


Figure 3-4: Measurement Setup for evaluation Return Loss of coaxial interconnects

Figure 3-5 shows an example plot of a measurement of Return Loss for a Coaxial Interconnect. RL has been measured from both Ports into sides of the Interconnect, resulting in S11 and S22.

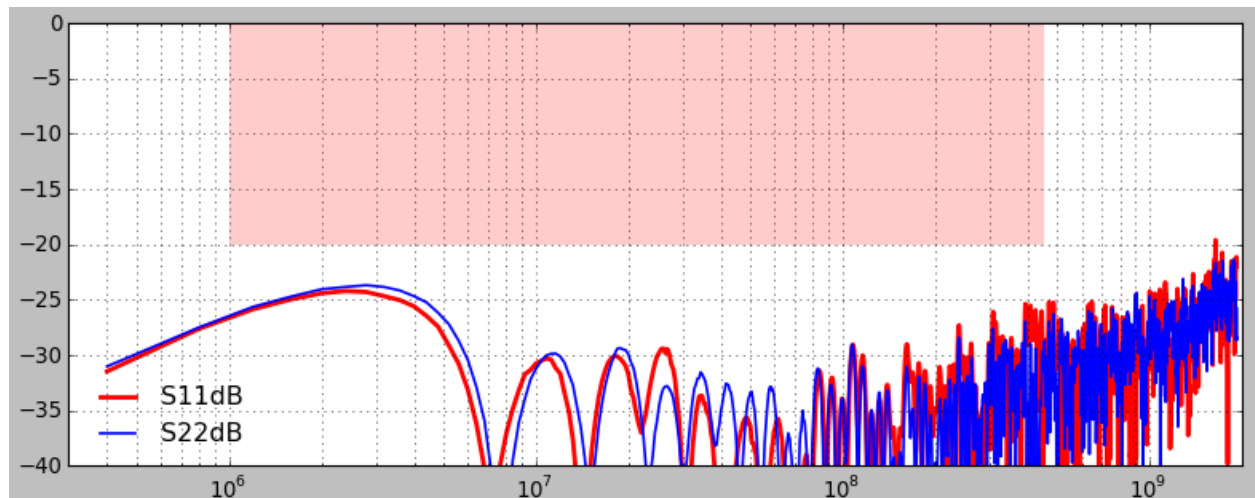


Figure 3-5: Measurement Setup for evaluation Return Loss of coaxial interconnects

3.8 Return Loss of PCB Interfaces

The connection of signals between a Coaxial Cable and a Coaxial Transceiver is realized on the PCB of the ECU. The circuitry, including passive components and PCB-traces is called Analog Frontend. Also this portion of the data link is expected to fit as close as possible to the characteristic line impedance of 50 Ohms. Deviations in impedance matching will cause reflections; Return Loss is the ratio between transmitted and the reflected signal energy.

[3] defines a limit line in the frequency domain; the measurement however can be done in time – or frequency domain. The measurement setup is a 1-port configuration, emitting a signal into a PCB-Interface (e.g. SP3 for Simplex or combined SP2/3 in Duplex) and measuring the reflected energy. The result must be transferred to magnitude in dB-scale and compared with the Limit-Line. CTR in Figure 3-6 means Coaxial Transceiver as used in Duplex applications. It is also meant as a synonym for CEC and ECC for Simplex Applications.

Note: For Return Loss measurement of PCB-Interfaces the ECU must be unpowered!

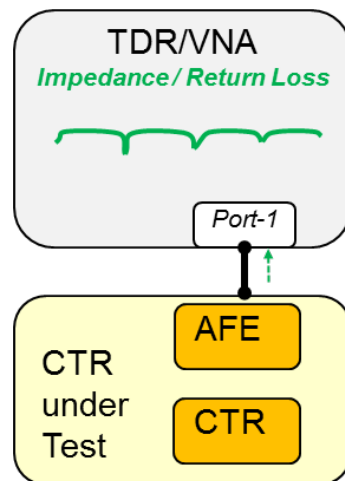


Figure 3-6: Measurement Setup for evaluation Return Loss of PCB Interfaces

MOST150 cPhy does not specify specific requirements in resolution or scale of the frequency axis for RL. It is solely in the responsibility of the supplier to apply appropriate settings. Figure 3-7 shows an example plot of a measurement of Return Loss for a PCB Interface.

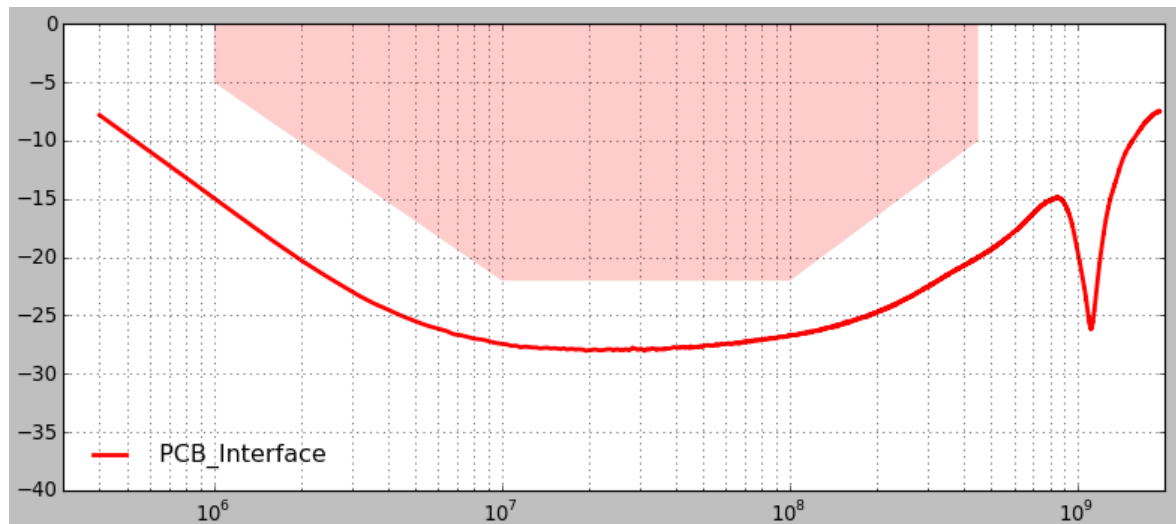


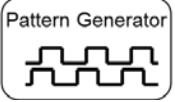
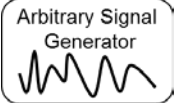
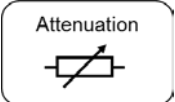
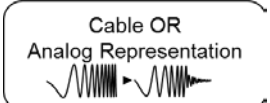
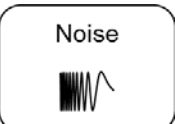
Figure 3-7: Measurement Setup for evaluation Return Loss of PCB Interface

Time-Domain-Reflection (TDR) is another valuable method to evaluate impedance characteristic of such PCB-interfaces. TDR sends a pulse into the DUT and measures response in magnitude and delay. The result usually is a plot of impedance over propagation time. In order to compare with the specified Limit Line (Chapter 6.3.2.2 in [3]) TDR result need to be transferred to frequency domain.

3.9 Creating a Stimulus for SP3

Evaluation of a Coaxial receive portion means to apply *worst case* signals to SP3 and observe the response on the output of the Receiver. This falls under evaluation of Signal Quality. Challenge now is to find out what *worst case* means for a Receiver and how to create such scenarios. Beside such Signal Quality testing also activity detection conditions need to be tested. These tests will need stimuli with lower amplitudes and different patterns than used for Signal Quality

For better visibility, the block-diagrams in this chapter are showing simplified setups. Some general comments are listed below:

<i>graphical symbol</i>	<i>description</i>
	used to create MOST patterns, here mainly for SP2. Such generated Pattern Generator must be able to create Signal following SP2 Signal Quality requirements (single ended output, variation within extreme Pulse Shapes, variation with in extremes of Timing Distortion, adjustable output voltage)
	used to emulate coaxial Signals, which includes signal variations as produced by a coaxial Transmitter in combination with variations added by coaxial interconnects.
	Used in combination with the Pattern Generator or Arbitrary Signal Generator to adjust amplitude. This may need in case limited Voltage adjustment capabilities of the generator.
	used to emulate Attenuation as produced by a coaxial Interconnect. This can be either real cables with known transfer characteristics, analog modules emulating such cable transfer characteristic or combinations of both.
	Used to generate Crosstalk. Such noise will be added to data-signal to evaluate performance of a coaxial receiver under stress (Duplex only)

3.9.1 Creating a Stimulus for SP3 for Simplex Applications

Based on cPhy specification, the following impacts on Signal Quality at SP3 need to be considered:

- Valid MOST signal starts from SP2, all variations permitted by cPhy need to be taken into account (e.g. min/max Amplitude, Transition Times, Jitter, etc.)
- Signal is attenuated when travelling through the interconnect (Attenuation(f))
- Some additional but minor losses will happen at the interface cable to PCB (SP3)

- For activity detection, other patterns (lower frequency content) than valid MOST patterns have to be used. Signal with lower amplitude or additional attenuation may be used for evaluating on/off thresholds

There are 3 basic test-setups which can be used to emulate above listed influences and stress an CEC under test. The following table explains the 3 configurations (A, B, C)

	Emulating ECC	Emulating Wire Harness	CEC under Test
	Pattern Generation / Signal Conditioning	Frequency dependent Attenuation	
	<p>Control on</p> <ul style="list-style-type: none"> - Pattern for Valid Data and activity detection - Amplitude, Transition Times - Output Jitter <p>Control on</p> <ul style="list-style-type: none"> - Frequency dependent Attenuation, emulate various combinations of DCloss and Fskin 		
[A]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10kHz and up to 75MHz MOST Stress Pattern	Use real cables in various combinations, requires pre-selected cables and components	
[B]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10kHz and up to 75MHz MOST Stress Pattern	Use specific circuitry, emulating cable characteristic with analog filters. A few characteristics may be combined on one PCB	
	<p>Control on</p> <ul style="list-style-type: none"> - Pattern for Valid Data and activity detection - Amplitude, Transition Times - Output Jitter - Frequency dependent Attenuation, emulate various combinations of DCloss and Fskin <p>Additional Attenuation may be needed</p>		
[C]	Using an arbitrary waveform generator – combining signal generation with cable emulation: processing various patterns, incl. various signal conditions, adding frequency dependent attenuation Additional Attenuation may be needed!		

Pro / Cons of suggested Simplex setups

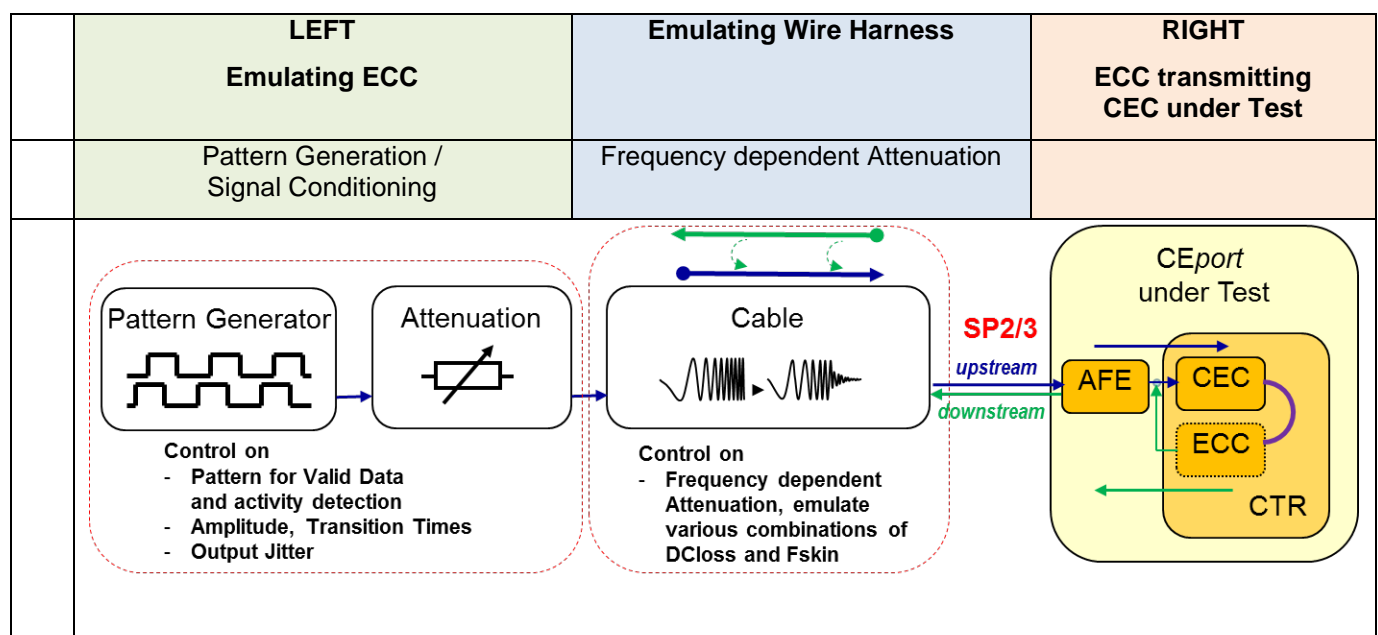
Setup	PRO	CON
[A], [B]	wire harness / cable emulation can be re-used in real network-links, multi node networks, qualification testing, EOL testing, etc.	fixed structure, not adaptable, practically low number of scenarios
[C]	gives best flexibility in generating multiple stress- scenarios, easy adaptation in case new challenging configurations	not usable in real links, no re-use in other test areas.

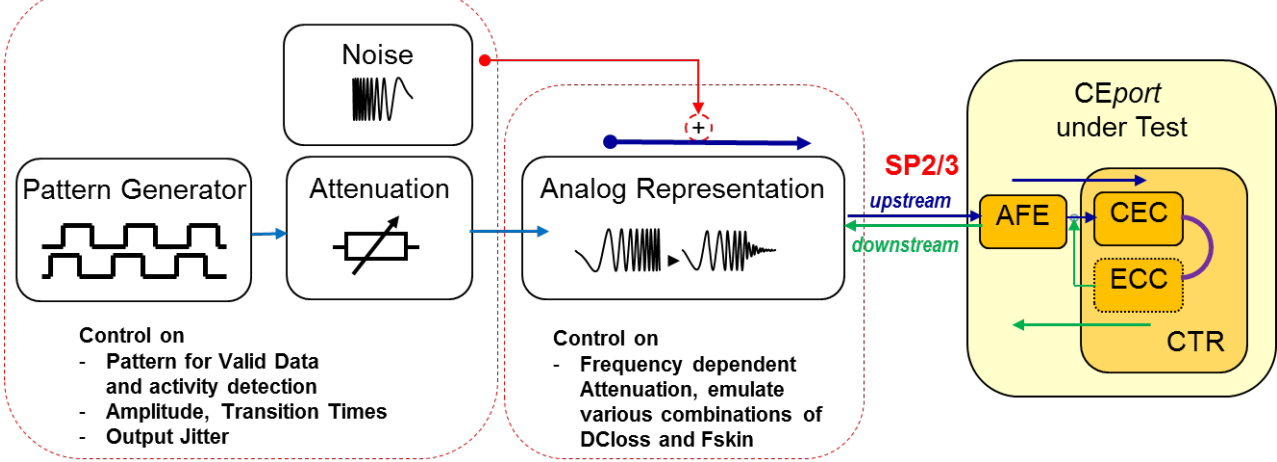
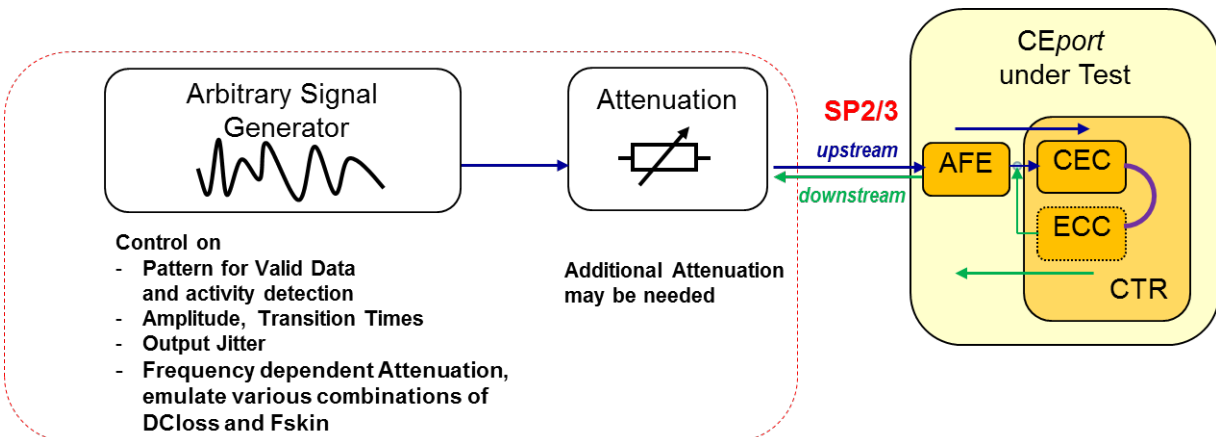
3.9.2 Creating a Stimulus for SP3 for Duplex Applications

Based on cPhy specification, the following impacts on Signal Quality at SP3 need to be considered:

- valid MOST signal starts is being transmitted from the nodes on both sides of the link, all SP2-variations permitted by cPhy need to be taken into account (e.g. min/max Amplitude, Transition Times, Jitter, etc.), oppositional settings for both nodes will be required
- Signals are attenuated when travelling through the interconnect (Attenuation(f))
- Some additional but minor losses will happen at the interface cable to PCB (SP3)
- Impedance mismatches along the link enable reflections. At the location of the mismatches, signal edges from both nodes will trigger reflection, which then will overlay with opposing signal. Amplitude of such crosstalk depends on the grade of impedance mismatch, amplitude and transition time of the triggering signal, as well as the location of the mismatch (attenuation due to the cable). Multiple reflections in one link may overlay constructively or destructively.
- For activity detection, other patterns (lower frequency content) than valid MOST patterns have to be used. Signal with lower amplitude or additional attenuation may be used for evaluating on/off thresholds. Activity detection needs to be tested under presence of crosstalk.

There are 3 basic test-setups which can be used to emulate above listed influences and stress a CEC under test. The following table explains the 3 configurations (A, B, C)



[A]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10kHz and up to 75MHz MOST Stress Pattern	Use real cables in various combinations, requires pre-selected cables and components Impedance mismatches as exists, no possibility to control them	ECC is actively transmitting downstream. Max Amplitude and fast edges are used to trigger max. reflections.
			
[B]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10kHz and up to 75MHz MOST Stress Pattern	Use specific circuitry, emulating cable characteristic with analog filters. A few characteristics may be combined on one PCB Add circuitry that allows overlaying noise/crosstalk, generated by another signal generator. Noise level must be adjusted to levels corresponding with worst case RL figures in cPhy. Noise Signal shall be uncorrelated to the MOST Signal in frequency and phase	ECC is inactive! Crosstalk is solely emulated by the noise source
			
[C]	Using an arbitrary waveform generator – combining Signal generation with cable emulation and Crosstalk emulation: <ul style="list-style-type: none">processing various patterns, incl. various signal conditions,		ECC is inactive! Crosstalk is fully implemented on test pattern

	<ul style="list-style-type: none"> • adding frequency dependent attenuation • adding amplitude noise <p>Additional Attenuation may be needed!</p>	
--	---	--

Pro / Cons for suggested Duplex setups

Setup	PRO	CON
[A]	wire harness / cable emulation can be re-used in real network-links, multi node networks, qualification testing, EOL testing, etc.	fixed structure, not adaptable, practically low number of scenarios fixed crosstalk pattern, grade and location of impedance mismatches is fixed
[B]	wire harness / cable emulation can be re-used in real network-links, multi node networks, qualification testing, EOL testing, etc. limited re-use crosstalk generation, impacts signal in both directions	circuitry itself will create impedance mismatches, these need to be considered as a base impairment of the Duplex link
[C]	gives best flexibility in generating multiple stress- scenarios, easy adaptation in case new challenging configurations	not usable in real links, no re-use in other test areas.

4 Measurement of Phase Variation

4.1 Basics

Measurement of Phase Variation

Phase Variation describes data stream noise and distortion in the time domain. Based on spectral content of the variation, Sub-categories of Phase Variation are defined.

Phase Variation	Spectral limits
Wander	DC up to 10 Hz
Transferred Jitter (T_j)	Jitter with 10 Hz up the limit given by the Jitter Filter
Alignment Jitter (A_j)	Jitter with spectral content above the limit given by the Golden PLL

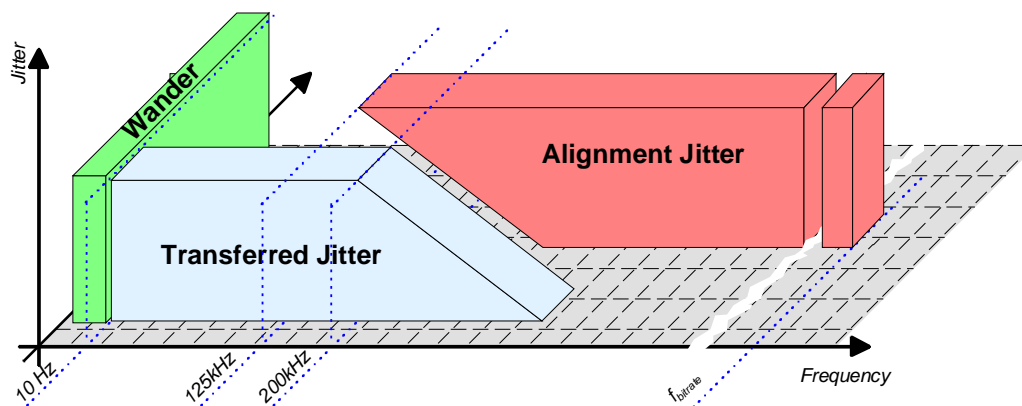


Figure 4-1: Sub-categories of Phase Variation

The need for separating T_j and A_j is founded in the synchronous approach of the MOST network. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node will recover the clock for sampling the input data out of the received data stream. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain correlation in phase between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). The PLL enables the capability of tracking of Phase variations. Phase variation in a lower spectral range on an incoming data stream will be compensated by aligning the clock's phase accordingly. Therefore, low frequency jitter will not impact the data recovery. However, the clock for generating the output data, which is derived from the recovered input clock, will be affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter cannot be tracked by the PLL and will lead to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum Alignment Jitter A_j) to be tolerated is defined with the eye masks for each specification point.

The dynamic characteristics of a PLL for a MOST node are covered by the physical layer specification with two definitions:

“Golden PLL”:

The “Golden PLL” is a model, given in the form of a transfer function representing a low pass filter. The “Golden PLL” serves two purposes.

1. It is used as a measurement tool for generating a time base which is required for forming eye diagrams and determining A_j at each SP along a link. The golden PLL must take data in from the measured SPs and generate a UI-clock. Based on the recovered UI-clock an eye diagram is drawn. Eye masks, defined for each SP give the limits for A_j respectively.
2. The “Golden PLL” describes the behavior of a NIC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass (or higher) will be tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass may lead to misalignment. The “Golden PLL” in combination with the eye mask for SP4 receiver tolerance describes the minimum A_j tolerance of a NIC’s receive section.

“Jitter Filter”:

The Jitter Filter is a model, given in the form of a transfer function representing a low pass filter. It serves two purposes.

1. It is used as a measurement tool for extracting Transferred Jitter (T_j) out of the total jitter.
2. Additionally, it describes the worst case jitter transfer characteristic over a NIC. Jitter below the spectral range described by the low-pass may be tracked by a PLL. The data stream being generated by this NIC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

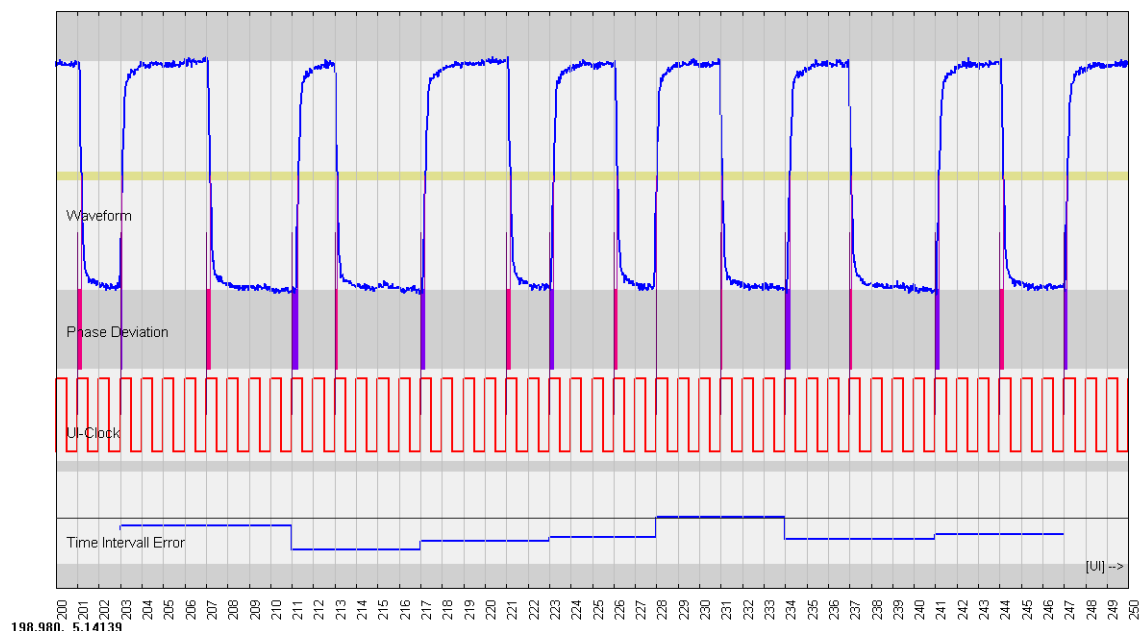
4.2 Measuring Alignment Jitter

The following table describes a procedure for detecting A_j out of a measured data stream. Oscilloscopes appropriate for the jitter measurements are Digital Sampling Oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	A probe (active differential or single-ended probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data stream ("waveform") is sampled into the scope's memory.
Clock recovery	<p>The DCA-coded MOST150 data stream contains clock and data. In a first step the clock must be extracted.</p> <p>Data-pulses range from 2 UI to 6 UI yielding 5 different pulse widths (2, 3, 4, 5, 6 UI). The required clock has a cycle-time of 1 UI, which is twice the bit rate (i.e., for F_s 48 kHz, the bit rate is 147.45 Mbit/s, the UI-clock is 294.91 MHz).</p> <p>A method of extracting the UI-clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST150 specifies that the "Golden PLL" is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p>

Example:

- UI-clock is fitted in frequency and phase to the waveform
- remaining phase deviations are marked in the diagram
- phase deviations for rising edges are shown in the "Timing-Interval Error" graph



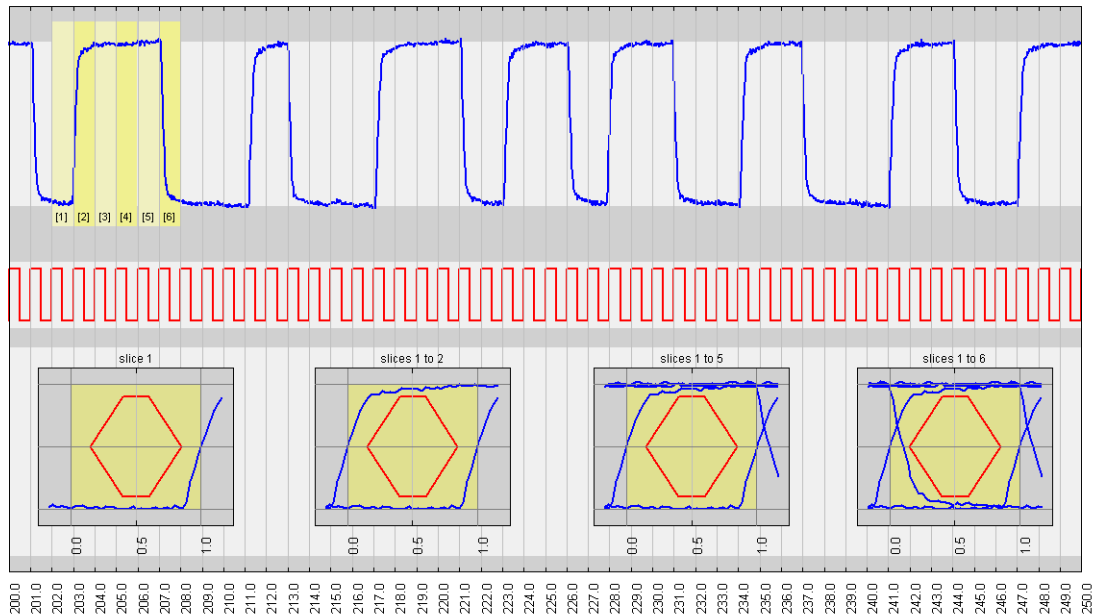
Note: In many oscilloscopes, visualization of the recovered UI-clock is not possible.

Applying Low Pass filter given by "Golden PLL"	Once a first derivate of the UI-clock is approximated, there may still be phase differences between rising data-edges and the recovered UI-clock, called "Time Interval Errors". Applying the low-pass filter (given by the "Golden PLL" model) to the sequence of consecutive "Time Interval Errors" results in a filtered phase-deviation sequence. This sequence represents the minimum
--	--

	<p>capability of the NIC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI-clock need to be compensated by the sequence of filtered Phase-deviations.</p> <p>The resulting new UI-clock, which is used for further calculations, now represents the base UI-clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. However, modulation capability is limited in spectrum given by the “golden PLL” model.</p>
Calculating Alignment Jitter	<p>Alignment Jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI-clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over run-time in a graph result in an “A_J-Track” which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an “A_J-Jitter-Histogram”.</p>
Forming the Eye	<p>For drawing the eye diagram, the waveform is sliced in intervals of 1 UI length aligned with the UI-clock. The sliced waveform segments plus some overhead (i.e., 0.25 UI on both sides) are overlaid in one graph.</p> <p>Notes:</p> <ul style="list-style-type: none"> • <i>As shown in the diagram below, each transition is drawn twice, one time on the left side and secondly on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram.</i> • <i>Duty cycle distortion DCD, if it exists, will shift the eye towards the mask. In the shown example, LOW pulses are shorter than HIGH pulses. The UI-clock is referenced to rising edges which causes the rising edges to be adjusted to the UI-borders, while the falling edges are shifted by the amount of the DCD.</i>

Example:

- slice-sections are marked in the waveform graph
- sliced waveform segments are overlaid in a single diagram
- temporary results are shown



Pass/Fail-Test using Eye masks	<p>Signal integrity is checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error.</p> <p>The masks are defined by hexagons with points A, B, C, D, E and F. Points A and D are limiting A_J while B, C, E, F build constraints for amplitude and pulse-shape.</p>
Bit Error Rate	<p>The requested BER of 10^{-9} requires an eye diagram showing at least 10^9 bits without violation of the mask!</p> <p>1 Bit = 2 UI → at least $2 \cdot 10^9$ hits are required</p> <p>Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is in the responsibility of the user.</p>

Table 4-1: Measuring Alignment Jitter

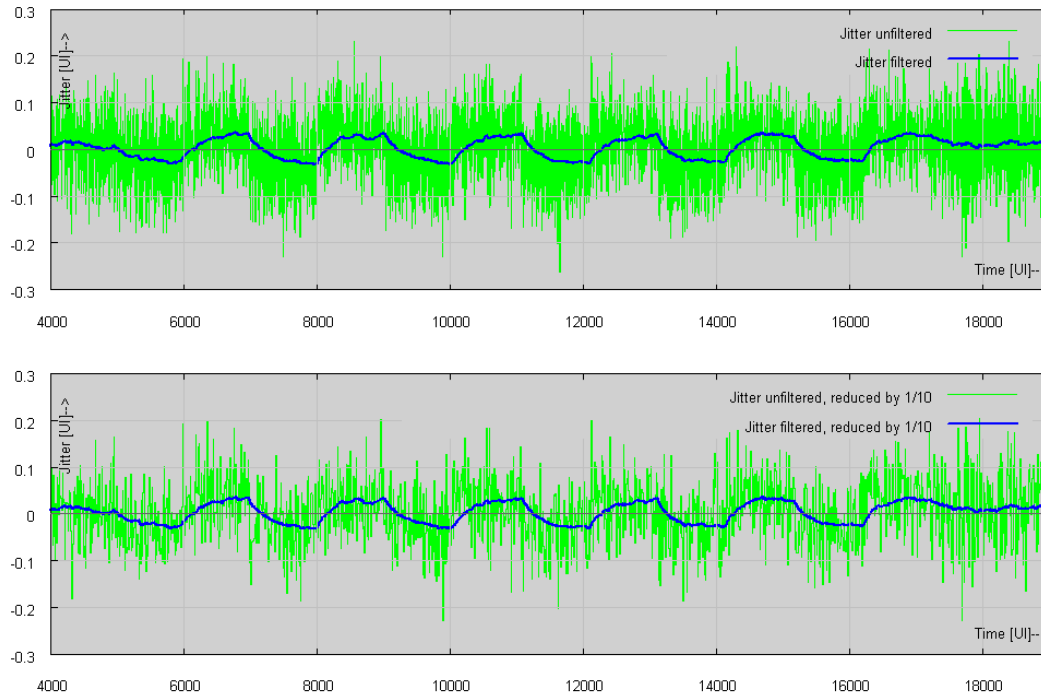
4.3 Measuring Transferred Jitter

The following table describes a procedure how to detect T_j out of a measured data stream. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	<p>For this measurement, the maximum available sampling memory of the oscilloscope has to be used. A probe (active differential or single-ended probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution (see b1/b0 detection, scaling channel/mask). A sequence of the data stream ("waveform") is sampled into the scope's memory.</p> <p>T_j is defined in the spectrum from 10 Hz (beyond Wander) and 200 kHz. The resolution of an oscilloscope low frequency jitter is limited by the size of memory.</p> <p>Note: <i>Even Oscilloscopes with very deep memory will hardly achieve 10 Hz resolution.</i></p>
Clock recovery	<p>Similar to the A_j Measurement procedure, the clock must be extracted. Clock separation is provided by an oscilloscope internal function.</p> <p>Similar to the A_j Measurement procedure, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency, the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p> <p>In contrast to the A_j Measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. However, smallest deviations in the detected bit-rate may grow up to a significant phase mismatch over the length of the acquired waveform and therefore affect further results. To enable a robust measurement procedure it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz).</p>
Extracting Transferred Jitter	<p>Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI-clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant, because only these deviations are tracked by the PLL and impact the recovered clock's phase.</p> <p>Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over run-time in a graph result in a "Jitter-Track".</p> <p>Successive phase deviations appear in pulse time intervals (2, 3, 4, 5, 6 UI), which correspond to the theoretical maximum jitter frequencies up to 150 MHz. With respect to the focused spectral range 10 Hz to 200 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process.</p> <p>In the next step, this "Jitter Track" (optionally reduced) needs to be low-passed, using the transfer function given with the "Jitter Filter" definition, which results in the "Filtered Jitter".</p>

Example:

- First graph: successive phase deviations are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")
- Second graph: successive phase deviations but reduced by factor 10 are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")



Calculating Transferred Jitter

Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using root-mean-square method RMS.

$$RMS = \sqrt{\frac{1}{N} \sum_{i=1}^N v_i^2}$$

In case filtered jitter contains a DC-component or Wander (i.e., caused by a constant phase mismatch between clock and data), it is tolerable to calculate the Standard Deviation instead of RMS.

Note: This option is only applicable if the spectral content of eliminated jitter component, expressed by the mean-value, is below 10 Hz.

$$StdDev = \sqrt{\frac{1}{N} \sum_{i=1}^N (v_i - mean)^2}$$

Table 4-2: Measuring Transferred Jitter

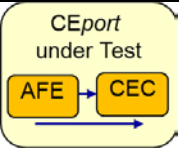
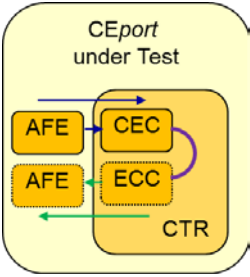
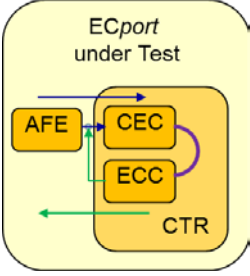
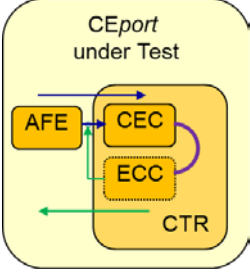
	<p>CEC, the analog frontend AFE, both applied on a PCB. It includes also variations in VCC and ambient temperature.</p> <p>This symbol is used for standalone Transceiver chips in SIMPEX mode</p>
	<p>“CEport under Test” includes the coaxial receiver component CEC, the coaxial transmitter component ECC, the analog frontends AFE, all applied on a PCB. Focus of Evaluation is set on CEport performance. It includes also variations in VCC and ambient temperature.</p> <p>This symbol is used for integrated Transceivers in SIMPEX mode</p>
	<p>symbol “ECport under Test” includes the coaxial transmitter component ECC, the coaxial receiver component CEC, the analog frontend AFE, all applied on a PCB. Focus of Evaluation is set on ECport performance. It includes also variations in VCC and ambient temperature</p> <p>This symbol is used for Transceivers in Duplex mode</p>
	<p>“CEport under Test” includes the coaxial receiver component CEC, the coaxial transmitter component ECC, the analog frontend AFE, all applied on a PCB. Focus of Evaluation is set on CEport performance in Duplex mode. It includes also variations in VCC and ambient temperature.</p> <p>This symbol is used for Transceivers in Duplex mode</p>

Table 5-1: component symbols

5.1.1 Setups for Dual Simplex

In Dual Simplex mode, Signals are transmitted on separate cable per signaling direction

5.1.1.1 SP2 Signal Quality Measurement for Simplex

An ECC realized as a standalone component offers a differential input interface in LVDS technology at SP1 and a single ended output interface at SP2. Signal Quality as a response to the input signal and operating conditions can be directly measured at SP2. The Test setup shown in Figure 5-1 can be used for evaluation of Transition times, Steady State Amplitude and Jitter.

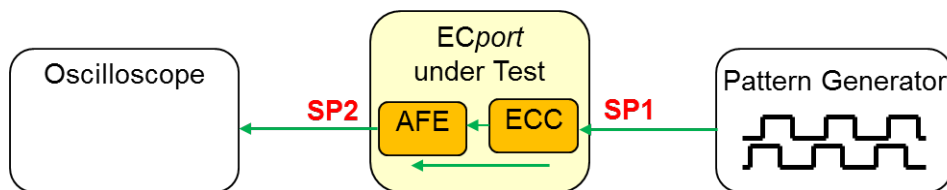


Figure 5-1: SP2 Signal Quality Measurement Setup for Simplex and standalone Transceiver

As described in chapter 4.4.2 of [3], integrated Transceivers do not necessarily offer direct access to SP1. The ECC input signal can be stimulated, by making use of the internal bypass (details see chapter 3.2.10.1 in [1]). As shown in Figure 5-2, in bypass mode the CEC output signal is re-transmitted on the ECC. An ECC provides a re-shaping of the output signal but no re-timing. Therefore the ECC output signal provides the opportunity on direct evaluation of Transition times and Steady State Amplitude. Timing Distortion measured at SP2 includes contribution from of CEC and ECC. A reference of ECC performance shall be measured upfront and the result can be compensated for the ECC impact. An example for such reference measurement is shown in Figure 5-3.

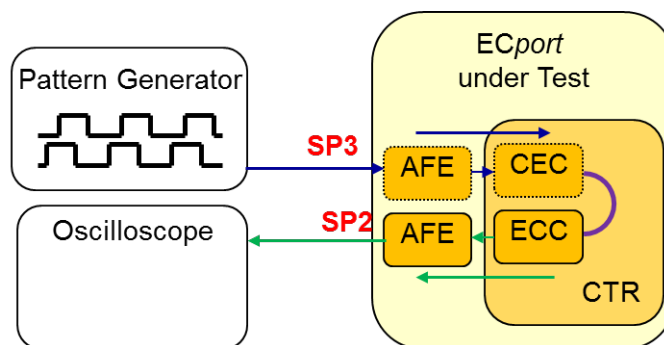


Figure 5-2: SP2 Signal Quality Measurement Setup for Simplex and integrated Transceiver

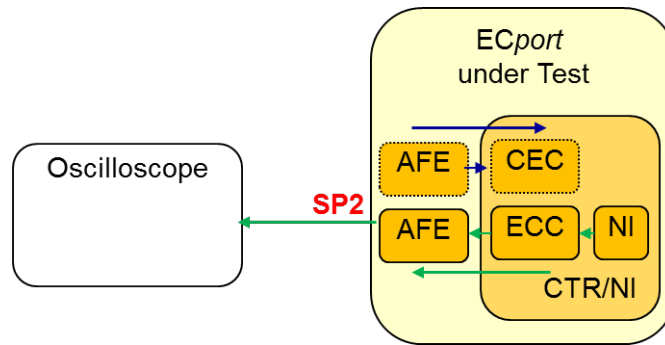


Figure 5-3: SP2 Jitter Measurement Setup for Simplex and integrated Transceiver, Reference with Data from internal NI

5.1.1.2 SP4 Jitter Measurement (A_j & T_j) for Simplex

As discussed in 3.9, there is various influences on a transmission channel that degrades signal quality of an input signal @ SP3. Such impacts as well as the operating conditions of a Coaxial Receiver determine the signal quality at SP4.

A CEC, realized as a standalone component exhibits an output interface in LVDS technology. Signal Quality as a response to SP3 input stimuli and operating conditions can be measured as Jitter (A_j and T_j). A Test setup in Simplex Operation is shown in Figure 5-4.

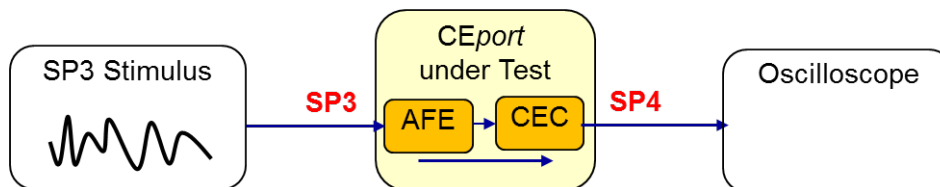


Figure 5-4: SP4 Jitter Measurement for Simplex and standalone Transceiver

For integrated Transceiver as described in chapter 4.4.2 of [3], the CEC output signal can be accessed making use of the internal bypass (Details see chapter 3.2.10.1 in[1]). The CEC output is re-transmitted on the ECC. This provides a re-shaping of the ECC output signal but no re-timing. The measured signal then includes Timing Distortion of the CEC plus the ECC. A reference of ECC performance shall be measured upfront and the result can be compensated for the ECC impact.

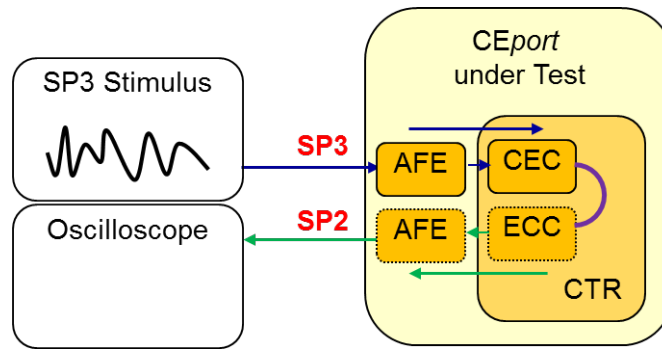


Figure 5-5: SP4 Jitter Measurement for Simplex and with integrated Transceiver

5.1.2 Setups for Duplex

In Duplex mode, Signals are transmitted in both directions over the same cable. Upstream and downstream signals are overlaying each other. For unification and simplification, the following test setups are showing the ECC under test to drive the downstream path, while incoming signals are always fed from upstream path.

5.1.2.1 Directional Couplers

Signal Quality Measurements in Duplex links may require usage of directional couplers. The directional coupler provides three terminals. Two of them offer a bidirectional transmit path, a third terminal provides an out-couple path from one of the other two terminals. The coupler itself is a non-ideal component and therefore has impact on the signals.

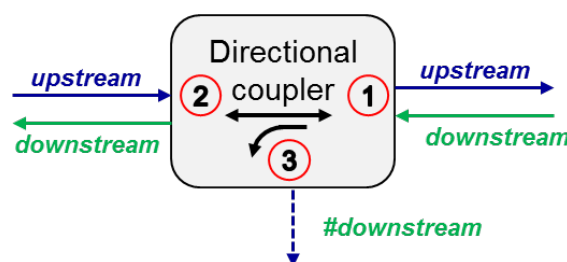


Figure 5-6: Directional Coupler

Example in Figure 5-6 shows a directional coupler with 3 terminals. Up-/Downstream signals are applied to terminals (1) and (2). An attenuated version of downstream is produced at (3), it is marked with a '#'. The following impairments need to be considered:

impairment	effect
Insertion Loss	The transmit path (1) \leftrightarrow (2) attenuates both signals of the Duplex link
Coupling Loss	The out-coupled signal (1) \rightarrow (3) provides an attenuated copy of the signal on (1)
Return Loss	The impedances on the terminals of the coupler may deviate from ideal 50 Ohms. This creates impedance mismatches with the connected components and therefore causes loss and reflections.
Directivity	A crosstalk path between the signal path (2) \rightarrow (1) and the out-couple path (1) \rightarrow (3) might exist

Table 5-2: signal impairments due to directional coupler

All the listed impairments are functions of frequency. The grade of attenuation and imperfection depends on the chosen product. Depending on chosen product, not all might end up in measureable distortion, de-embedding of known impairments is recommended.

A pragmatically method to evaluate crosstalk caused by a Directional Coupler is depicted in Figure 5-7. Assuming the Components of a setup are all connected by cables and the right most devices would normally be the DUT (ECC / CEC under test). Replacing the DUT with an idealized 50Ohm termination device will result in a measurement, showing the reflected energy. Main portion of

reflections in that setup are supposed to stem from the impedance mismatch between Terminal (1) and the 50Ohm termination. Direct crosstalk from transmit path (2)→(1) to out-couple path (1) → (3) would also be visible but empirically seems to be of less significance. The Oscilloscope shows the reflection with attenuation given by the out-couple path.

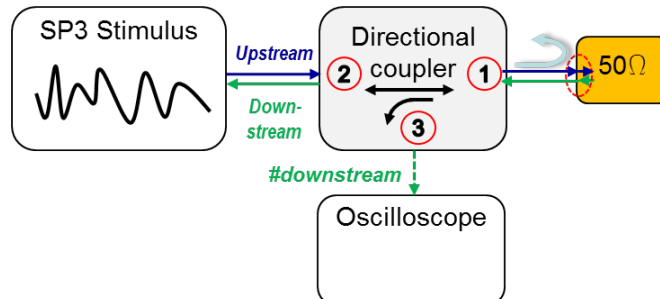


Figure 5-7: Crosstalk caused by directional coupler, measured with ideal 50Ohm

Note: In a real test setup, with a real DUT connected instead of the ideal 50Ohm termination, the Impedance of the DUT may deviate from 50Ohm (see [3] chapter 6.3.2). Therefore the total impedance mismatch may be larger or smaller as seen in the before mentioned setup.

Reflections are triggered by signal edges coming from both sides of the mismatch. In a Duplex link two potential issues need to be considered:

- This is the SP3-Stimulus in the Upstream path, creating reflections, which are overlaying with the Downstream Signal. This affects the out-coupled signal (#downstream). This may compromise parameter performance measured with the oscilloscope.
- But also the ECC output signal (Downstream), triggers reflections, which are overlaying with the Upstream Signal inside the DUT. This degrades the input signal into the CEC. This may compromise Signal Quality presented to the CEC input as well as it may affect the response of activity detection circuitry inside the Transceiver.

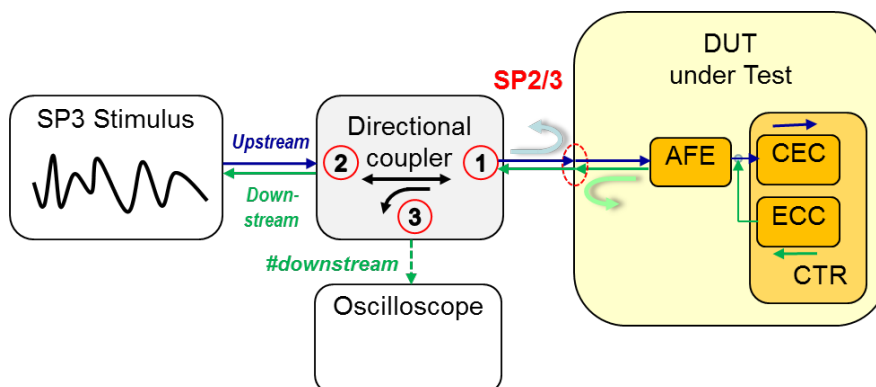


Figure 5-8: Crosstalk caused by directional coupler, in real setup

For selection of a suitable Directional Coupler all mentioned parameters need to be considered. As some parameters have interdependencies with each other, a chosen Coupler product may not be perfect. The impact of such imperfection in a setup needs to be considered!

5.1.2.2 SP2 Signal Quality Measurement for Duplex

In Duplex mode, Signals are transmitted in both directions over the same cable. Upstream and downstream signals are overlaying each other. The following test setups are showing the ECC under test to drive the downstream path, while incoming signals are fed from upstream path.

Duplex transceivers realized as standalone component, provide differential input interfaces in LVDS technology. Evaluation of the ECC's Signal Quality can be done without presence of an upstream signal. The setup is shown in Figure 5-9. From a function point of view, this setup is identical with the setup shown in Figure 5-1. The Test setup can be used for evaluation of Transition times, Steady State Amplitude and Jitter.

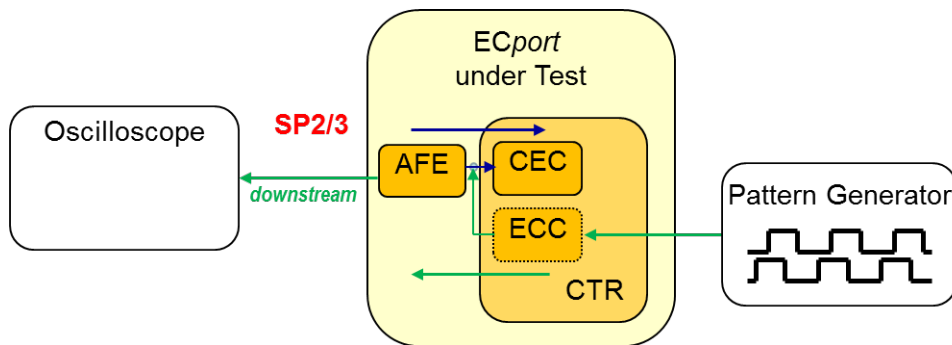


Figure 5-9: SP2 Jitter Measurement Setup for Duplex and standalone Transceiver

For integrated Transceivers the ECC input signal can be stimulated, using the internal bypass (Details see chapter 3.2.10.1 in [1]). As shown in Figure 5-10, the stimulus pattern being transmitted upstream, through the directional coupler, through the CEC (incl. AFE), bypassed to the ECC input and then re-transmitted by the ECC. The ECC output signal (again through the AFE) is transmitted downstream and certain portion of the signal energy is transferred to the out-coupled path of the directional coupler. The ECC provides a re-shaping of the output signal but no re-timing. Therefore the measured signal can be used for direct evaluation of Transition times and Steady State Amplitude. Timing Distortion however includes contribution from ECC and CEC.

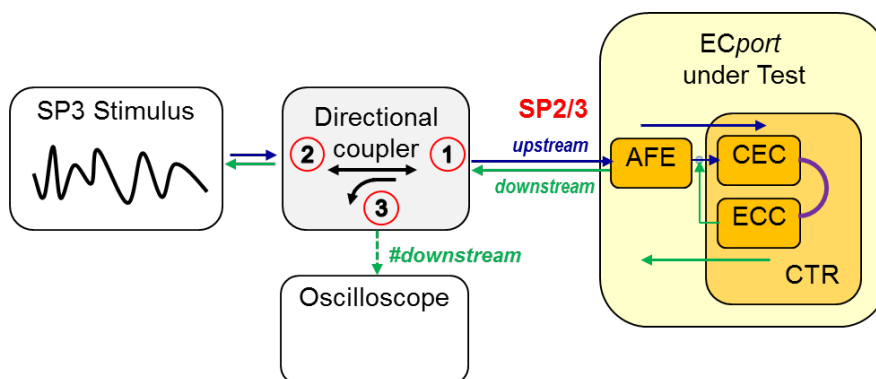


Figure 5-10: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver

A reference of ECC performance shall be measured upfront and the result can be compensated for the CEC impact on the Timing Distortion. An example for such reference measurement is shown in Figure 5-11, it uses pattern generated inside the NIC to get rid of impairments from CEC and the directional coupler.

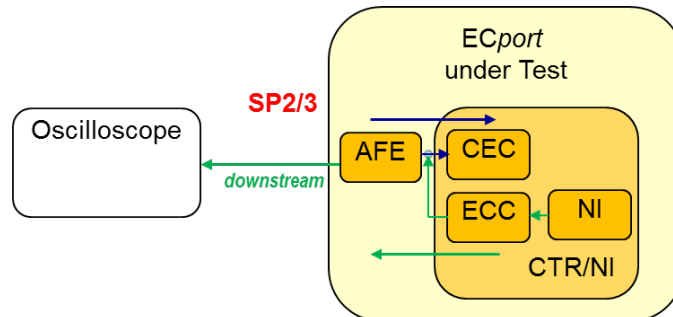


Figure 5-11: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver, Reference with Data from internal NI

5.1.2.3 SP4 Jitter Measurement (A_j & T_j) for Duplex

As discussed in 3.9, there are several options to emulate influences on a transmission channel that degrades signal quality of an input signal @ SP3. For Duplex links this is mainly Attenuation and Crosstalk. Such impacts as well as the operating conditions of a Coaxial Receiver determine the signal quality at SP4.

Compared to Simplex, the Duplex test setup is very similar. In Addition, the back channel is implemented as shown in Figure 5-12 to test the CEC under full load. Optionally, a directional coupler can be implemented to visualize the back channel signal, but this is not mandatory for this setup.

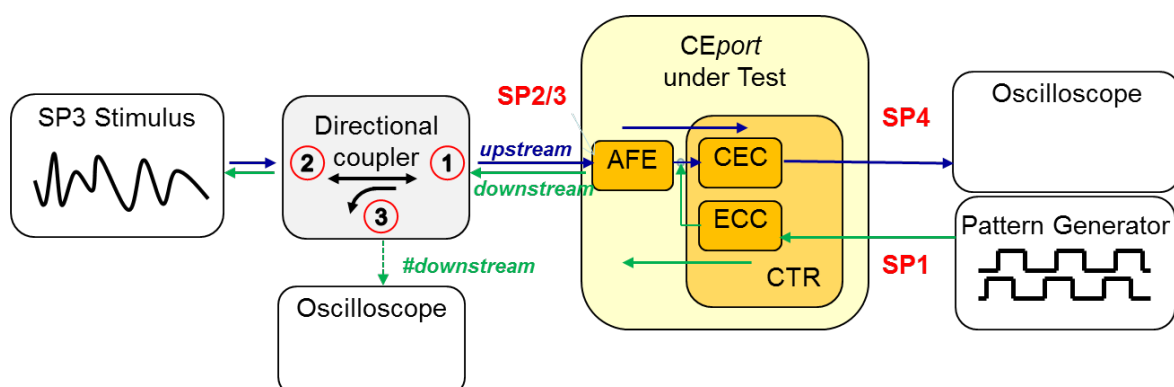


Figure 5-12: SP4 Jitter Measurement for Duplex and standalone Transceiver

For integrated Transceivers the CEC output signal can be accessed, using the internal bypass (Details see chapter 3.2.10.1 in [1]). As shown Figure 5-13, the stimulus pattern is being transmitted upstream, through the directional coupler, through the CEC (incl. AFE), bypassed to the ECC input and then re-transmitted by the ECC. The ECC output signal (again through the AFE) is transmitted downstream and certain portion of the signal energy is transferred to the out-coupled path of the directional coupler. The ECC provides a re-shaping of the output signal but no re-timing. Beside the CEC's

response on various stimuli and test conditions, the resulting Timing Distortion includes contribution from ECC.

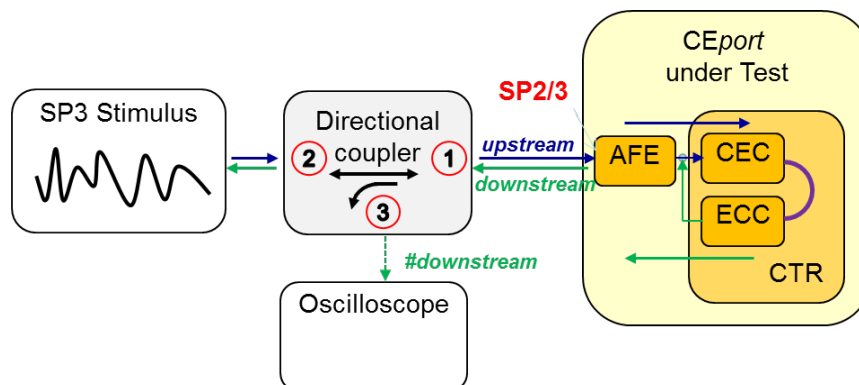


Figure 5-13: SP4 Jitter Measurement Setup for Duplex and integrated Transceiver

A reference of ECC performance can be measured upfront. The timing distortion result can be compensated for the ECC impact. An example for such reference measurement is shown in Figure 5-14, it uses pattern generated inside the NIC to eliminate impairments from CEC path.

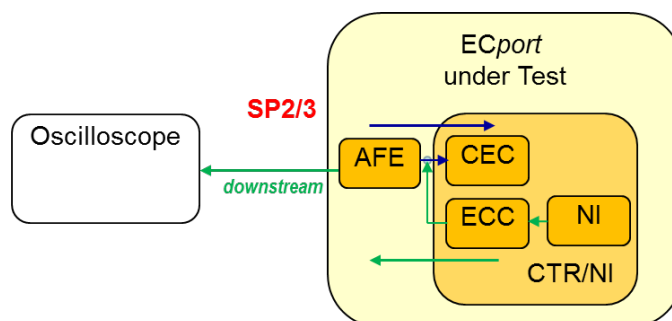


Figure 5-14: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver, Reference with Data from internal NI

6 Power Up / Power Down

6.1 General considerations

The chapter defines several possible test setups and sequences needed to exercise functional ECC and CEC requirements and also provides guidelines for the interpretation of the results.

All test sequences must be performed for the minimum, typical, and maximum of Operating Supply Voltage according to Operating Conditions given in section 1.2.

All test sequences must be performed for the minimum, typical, and maximum temperature specification.

When testing Modules (ECC and CEC in one case) crosstalk effects should be considered: when testing the one – the other must be active (where applicable)!

Some of the parameters defined by the Power Up / Power Down chapter of the Physical Layer Sub-specification could be measured directly (t_{STATF} , t_{LVDSV4} , etc.), others however (t_{ON2} , t_{OFF2} , t_{ON4} , etc.) define relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured directly this chapter defines test sequences including a timeout, which represents the maximal (resp. minimal) time interval allowed for the respective parameter. The end of this is marked in the signal charts (e.g., Figure 6-2) as Action Point (Δ) and appoints the time for a state validity evaluation.

E.g., $t_{ON2}(\text{max})$ time after the Reset signal goes HIGH start evaluating SP2 signal quality to check compliance to the requirements for “Valid Most Data”.

Measuring Electrical parameters such as LVTTTL or LVDS compliance is beyond the scope of this document and will not be discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

Testing of activity detection for ECC is described in chapter 6.2., followed by descriptions for CEC in chapter 6.3. Setups and Test cases are described based on standalone Transceivers, showing input stimuli and expected response. For a simplified presentation, all test cases are shown in Simplex mode. The requirements for activity detection in Duplex are identical with the Simplex ones. As an additional stress condition, a CEC in Duplex would be tested in presence of an actively driving ECC.

With integrated solutions as indicated in chapter 4.4.2 of [3], not all interfaces are accessible; therefore test case might not be applicable 1:1 (e.g. SP1-signals are inside the IC). In such case it is in solely responsibility of the ECC supplier to test the requested functionality in an appropriate way.

Testing of CEC's activity detection includes the full variety of scenarios being influenced by outer conditions, such as ac-conditions as specified in [3], SP2-signal performance of the preceding node, attenuation of coaxial interconnect, signal degradation due to return loss (especially for Duplex), etc. It is impossible depict all possible combinations of variations, nor is it possible to test them 100%. It is in the responsibility of the CEC supplier to perform tests that produce maximum stress for CEC under test and the selected mode of operation.

6.2 Measuring ECC Parameters

6.2.1 Measuring ECC Parameters – Test Setup

The diagram below outlines how a setup for measurement of the ECC performance could look like.

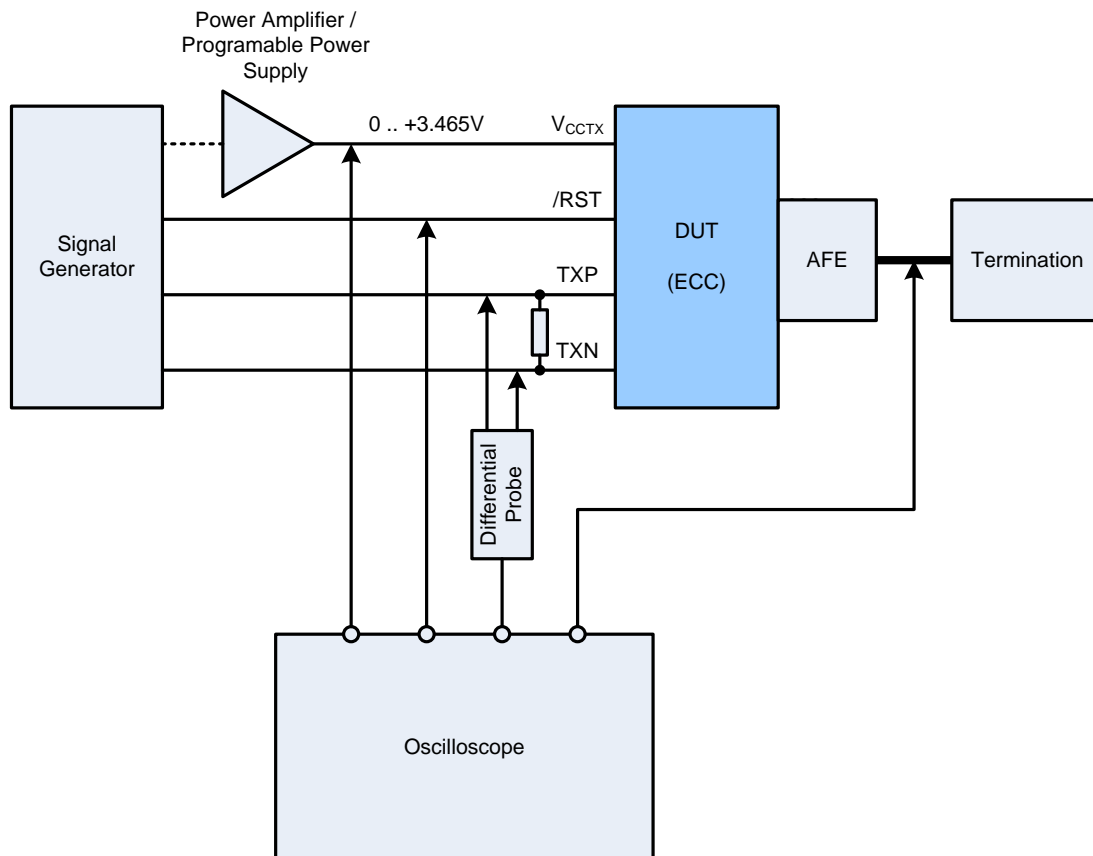


Figure 6-1: Setup for Measuring ECC ON/OFF Parameters

The main parts of the setup are:

- **DUT:** The DUT (Device Under Test), here the ECC or the ECC portion of a CTR, is fitted according to the manufacturer's recommended setup.
- **Signal Generator:** used to produce the stimuli (Test Patterns) and control the ECC Power Supply.
- **Termination:** 50 Ohm, preferably the Oscilloscope's internal 50 Ohm termination can be used
- **Oscilloscope:** to capture input and output signals data.
Note: SP1 signal is differential signal: the usage of active high-speed differential probe is recommended
- **Power Amplifier/ Programmable power supply:** to turn the ECC power supply on and off and to provide the desired supply voltage.

6.2.2 Measuring ECC Parameters – Signal Charts

The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the pre-requisites for the corresponding tests the ECC parameters.

The ECC parameter testing requires two different types of test sequences:

- In the first sequence ON/OFF behavior is controlled by signal content of SP1 while /RST is LVTTTL High (Figure 6-2).
- In the second sequence On/OFF behavior is controlled by /RST signal (Figure 6-3).

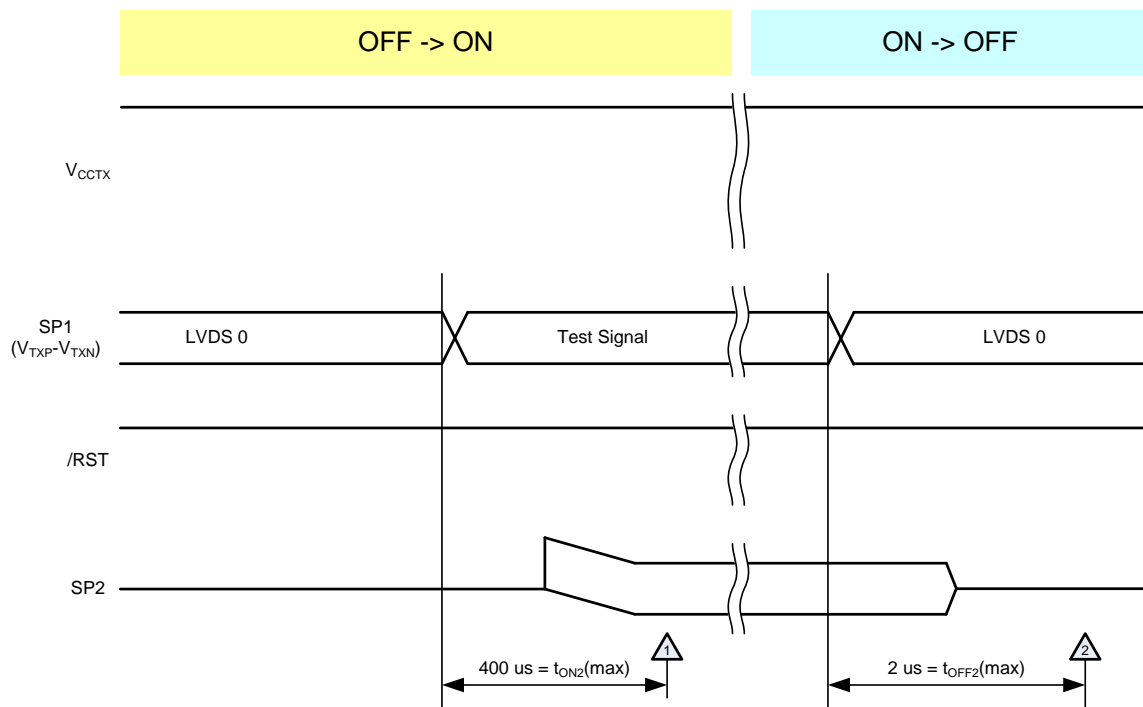


Figure 6-2: Measuring ECC Parameters: ECC Signal Chart No. 1

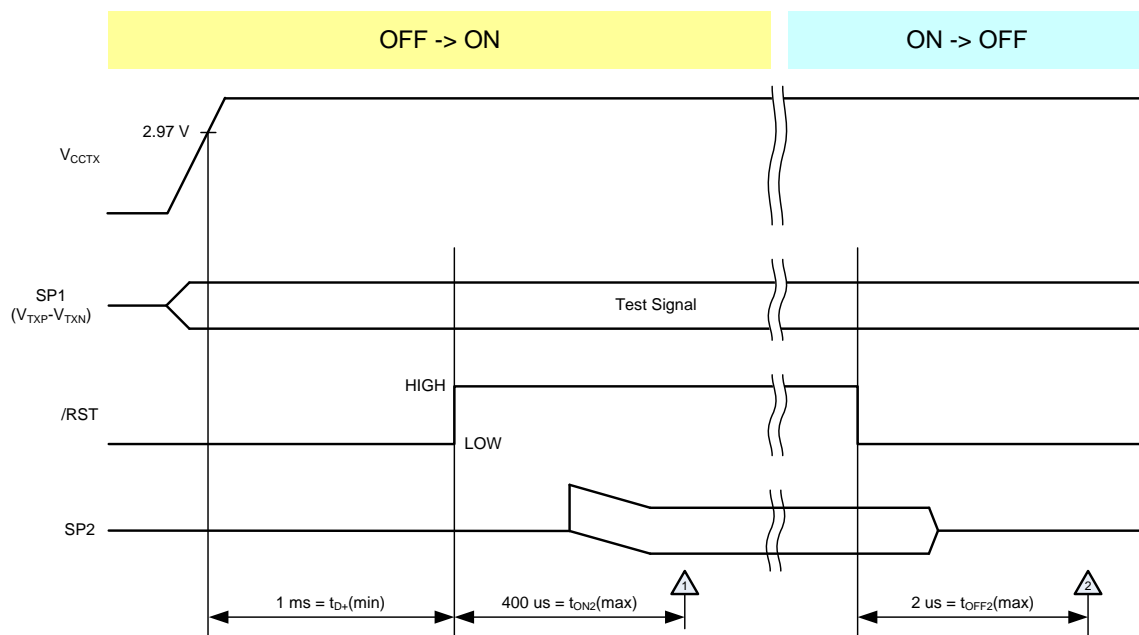


Figure 6-3: Measuring ECC Parameters: ECC Signal Chart No. 2

6.2.3 Measuring ECC Parameters – Test sequences

6.2.3.1 ECC Test Sequence #1 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS "0"
Initial State: Output	SP2	OFF state
Test Signal: Inputs	SP1 (V _{TXP} -V _{TXN})	10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	ECC shall remain in OFF state	

Table 6-1: ECC Test Sequence #1

This test sequence exercises the transition detection mechanism of the ECC. It is required that the ECC must remain in OFF state being supplied with input signal with frequency within F_{OFF1} requirements.

An oscilloscope must monitor the SP2 output before, during, and after the test to ensure the OFF state requirement is met.

6.2.3.2 ECC Test Sequence #2 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Initial State: Output	SP2	OFF state
Test Signal: Inputs	SP1 (V _{TXP} -V _{TXN})	12 MHz square wave pattern, LVDS compliant
Output / Expected behavior	ECC shall transition to ON state within time t_{ON2}(max)	

Table 6-2: ECC Test Sequence #2

This test sequence exercises the transition detection mechanism of the ECC. It is required that the ECC must perform transition detection at its input and remain in or transition to ON state being supplied with signal with frequency within F_{ON1} requirements. In this particular test the F_{ON1}(min) compliance is checked.

Another requirement being checked is the maximal allowed duration for the transition from OFF to ON state. The MOST150 cPhy Automotive Physical Layer Sub-Specification [3] states that the ECC must be in ON state not later than t_{ON2}(max) time after all ON conditions are met. In this case it is the time of the first rising edge of the Test Stimulus.

Since there is no directly measurable marker to notify the ECC entering ON state event, an indirect method is used: After the maximal allowed time has passed (end of t_{ON2}(max) – marked as Action Point 1 in the ECC Signal Chart Figure 6-2) a check of ON state requirements is started.

For this test, since the input is no MOST data, only the output voltage swing of the SP2 interface is checked.

6.2.3.3 ECC Test Sequence #3 - ON-to-OFF by SP1 Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 ($V_{TXP}-V_{TXN}$)	12 MHz LVDS compliant square wave
Initial State: Output	SP2	ON state
Test Signal: Inputs	SP1 ($V_{TXP}-V_{TXN}$)	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	ECC shall transition to OFF state within time $t_{OFF2}(\max)$	

Table 6-3: ECC Test Sequence #3

This test sequence exercises the transition detection mechanism of the ECC. It is required that the ECC must transition to OFF state being supplied with signal with frequency within F_{OFF1} requirements.

Another requirement being checked is the maximal allowed duration for the transition from ON to OFF state. The MOST150 cPhy Automotive Physical Layer Sub-Specification [3] states that the ECC must be in OFF state not later than $t_{OFF2}(\max)$ time after one or more OFF conditions are met. In this case, it is the time of the last falling edge of the 12 MHz square wave signal.

Since there is no directly measurable marker to notify the ECC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{OFF2}(\max)$ – marked as Action Point 2 in the ECC Signal Chart Figure 6-2), a check of OFF state requirements is started.

The oscilloscope must capture the SP2 output and evaluate the time after the point marked as Action Point 2 to ensure the OFF state requirement is met.

A signal marker could be produced from the signal generator after $t_{OFF2}(\max)$ time has elapsed since switching the SP1 signal to LVDS "0" (or 10 kHz square wave form) to allow triggering the oscilloscope.

Note: Long dataset capture is preferred, since the hold-off time that accompanies repetitive capture can lead to missed events.

6.2.3.4 ECC Test Sequence #4 - OFF-to-ON by SP1 Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Initial State: Output	SP2	OFF state
Test Signal: Inputs	SP1 (V _{TXP} -V _{TXN})	LVDS compliant Stress Pattern with nominal bit rate (BR)
Output / Expected behavior	ECC shall transition to ON state within time t _{ON2} (max)	

Table 6-4: ECC Test Sequence #4

This test sequence exercises the transition detection mechanism of the ECC. It is required that the ECC must perform transition detection at its input and remain in or transition to ON state being supplied with signal with frequency within F_{ON1} requirements. In this particular test, the F_{ON1}(min) compliance is checked.

Another requirement being checked is the maximal allowed duration for the transition from OFF to ON state. The MOST150 cPhy Automotive Physical Layer Sub-Specification [3] states that the ECC must be in ON state not later than t_{ON2}(max) time after all ON conditions are met. In this case, it is the time of the first rising edge of the Test Stimulus.

Since there is no directly measurable marker to notify the ECC entering ON state event, an indirect method is used: After the maximal allowed time has passed (end of t_{ON2}(max) – marked as Action Point 1 in the ECC Signal Chart Figure 6-2) a check of ON state requirements is started.

For this test the SP2 signal quality must be checked. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP2 signal quality. To assist the capture of the SP2 data in ON state, the signal generator could assert trigger signal to the oscilloscope t_{ON2}(max) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 100 μs.

6.2.3.5 ECC Test Sequence #5 - ON-to-OFF by SP1 Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2	ON state
Test Signal: Inputs	SP1 (V _{TXP} -V _{TXN})	LVDS "0", DC to 10 kHz square wave pattern, LVDS compliant
Output / Expected behavior	ECC shall transition to OFF state within time t _{OFF2} (max)	

Table 6-5: ECC Test Sequence #5

This test sequence exercises the transition detection mechanism of the ECC. It is required that the ECC must transition to OFF state being supplied with signal with frequency within F_{OFF1} requirements.

Another requirement being checked is the maximal allowed duration for the transition from ON to OFF state. The MOST150 cPhy Automotive Physical Layer Sub-Specification [3] states that the ECC must be in OFF state not later than t_{OFF2}(max) time after one or more OFF conditions are met. In this case it is the time of the last falling edge of the 12 MHz square wave signal.

Since there is no directly measurable marker to notify the ECC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of t_{OFF2}(max) – marked as Action Point 2 in the ECC Signal Chart Figure 6-2) a check of OFF state requirements is started.

The oscilloscope must capture the SP2 output and evaluate the time after the point marked as Action Point 2 to ensure the OFF state requirement is met.

A signal marker could be produced from the signal generator after t_{OFF2}(max) time has elapsed since switching the SP1 signal to LVDS "0" (or 10 kHz square wave form) to allow triggering the oscilloscope.

Note: Long dataset capture is preferred, since the hold-off time that accompanies repetitive capture can lead to missed events.

6.2.3.6 ECC Test Sequence #6 - OFF-to-ON by /RST Signal

Signal Chart	Figure 6-3	
Initial State: Inputs	V_{CCTX}	According to operating conditions
	/RST	LVTTL Low
	SP1 ($V_{TXP}-V_{TXN}$)	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2	OFF state
Test Signal: Inputs	/RST	LVTTL High
Output / Expected behavior	ECC shall transition to ON state within time $t_{ON2}(\max)$	

Table 6-6: ECC Test Sequence #6

This test sequence exercises the reset mechanism of the ECC. It is required that the ECC must transition to ON state within a time $t_{ON2}(\max)$ after the /RST signal has been driven low (and SP1 signal within F_{ON1}).

Another requirement being checked is the minimal allowed time for the /RST to be driven high after the power supply crosses the $V_T(\min)$ voltage. There are two aspects for treating this parameter:

The first is the power supply application aspect; the reset generator providing the signal must be designed to ensure the /RST signal does not transition to LVTTL High before $t_{D+}(\min)$ time has passed since the V_{CCTX} measured on the ECC power supply pins crossed V_T .

The second is the ECC parameter aspect; the MOST150 cPhy Automotive Physical Layer Sub-Specification [3] states that when being supplied with an operating voltage within V_{CCTXGR} , the internal circuitry of the ECC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+} . By driving the reset signal High at the $t_{D+}(\min)$ time it is checked if the ECC complies to that specification.

Since there is no directly measurable marker to notify the ECC entering ON state event, an indirect method is used for testing the $t_{ON2}(\max)$ compliance: After the maximal allowed time has passed (end of $t_{ON2}(\max)$ – marked as Action Point 1 in the ECC Signal Chart Figure 6-3) a check of ON state requirements is started.

For this test the SP2 signal quality must be checked. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP2 signal quality. To assist the capture of the SP2 data in ON state, the signal generator could assert trigger signal to the oscilloscope $t_{ON2}(\max)$ after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 100 μs .

6.2.3.7 ECC Test Sequence #7 - ON-to-OFF by /RST Signal

Signal Chart	Figure 6-3	
Initial State: Inputs	V _{CCTX}	According to operating conditions
	/RST	LVTTL High
	SP1 (V _{TXP} -V _{TXN})	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2	ON state
Test Signal: Inputs	/RST	LVTTL Low
Output / Expected behavior	ECC shall transition to OFF state within time t _{OFF2} (max)	

Table 6-7: ECC Test Sequence #7

This test sequence exercises the reset mechanism of the ECC. It is required that the ECC must transition to OFF state within a time t_{OFF2}(max) after the /RST signal has been driven low and it must stay in OFF state as long as /RST is driven low.

Since there is no directly measurable marker to notify the ECC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of t_{OFF2}(max) – marked as Action Point 2 in the ECC Signal Chart Figure 6-3) a check of OFF state requirements is started.

The oscilloscope must capture the SP2 output and evaluate the time after the point marked as Action Point 2 to ensure the OFF state requirement is met.

A signal marker could be produced from the signal generator after t_{OFF2}(max) time has elapsed since switching the switching /RST signal low to allow triggering the oscilloscope.

Note: Long dataset capture is preferred, since the hold-off time that accompanies repetitive capture can lead to missed events.

6.3 Measuring CEC Parameters

6.3.1 Measuring CEC Parameters – Test Setup

Physical Layer Specification defines a set of functional requirements and performance parameters that CEC has to meet. The diagram in Figure 6-4 outlines how a setup for measurement of the performance of CEC could be realized.

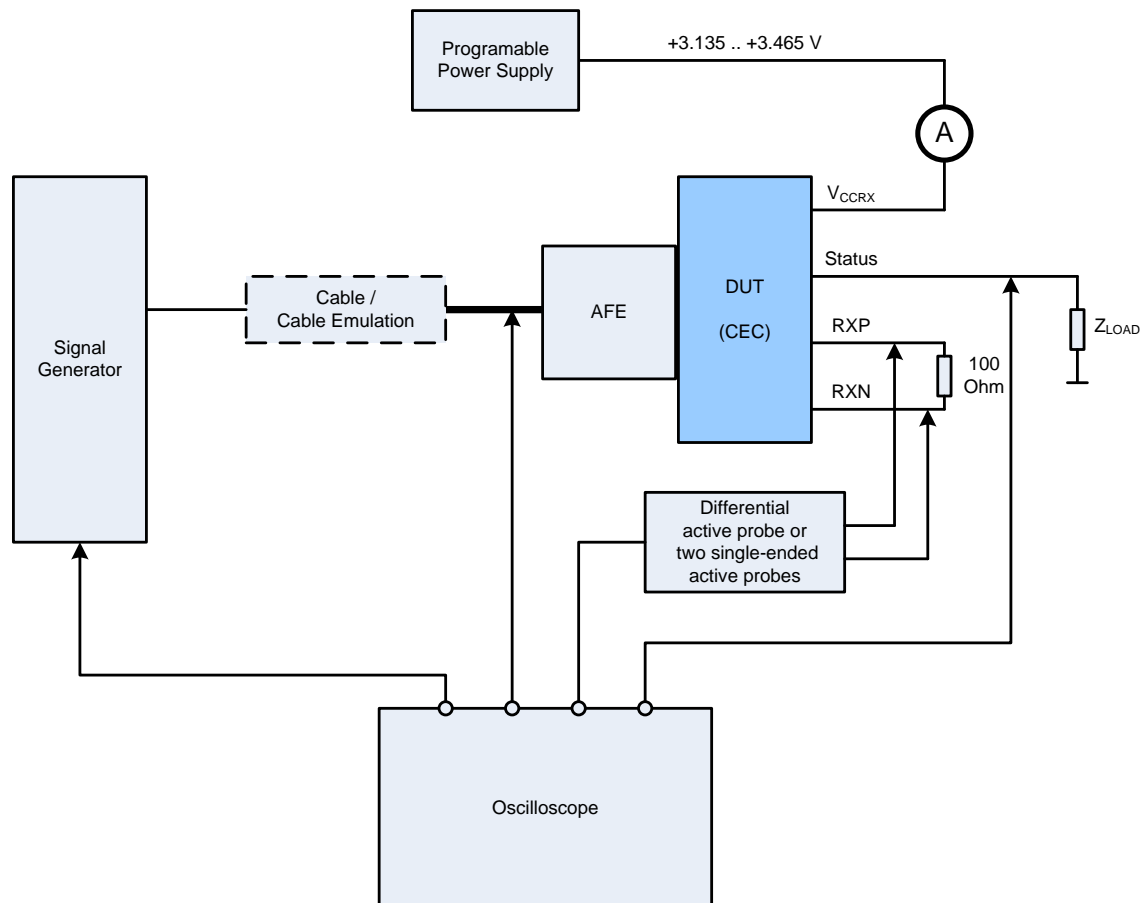


Figure 6-4: Setup for Measuring CEC ON/OFF Parameters

The main parts of the setup are:

- DUT: The DUT (Device Under Test), here the CEC or the CEC portion of a CTR, is fitted according to the manufacturer's recommended setup and is powered constantly during the tests.
- Cable or Cable Emulation to emulate degradation on data signals due to coaxial interconnects..
Note: Options to create a stimulus for SP3 interfaces as discussed in chapter 3.9 are also applicable here.
- Signal Generator: used to produce the test patterns and produce trigger signal for the oscilloscope.
Oscilloscope: to capture input and output signals data.
Note: SP4 signal is differential signal; the usage of an active high-speed differential probe is recommended.
- (Micro-)Ampere meter: to measure the current consumption of the CEC device in OFF state.

Signal Generator shown on Figure 6-4 emulates the SP2-interface in a real network. Therefore output signal amplitudes have to follow the specified values for SP2. In cases where cable emulation is already mathematically embedded in the Signal generators output patterns, amplitude settings have to follow SP2 amplitude values plus targeted cable degradation.

As a general rule, Signal amplitude at SP3 of the setup has to emulate SP2 amplitudes plus targeted the cable degradation. This is valid for MOST patterns as well as for Square wave pattern used for testing AC-conditions. Signal Generator and Cable/Cable emulation also shall provide an OFF-state as defined for the ECC (see chapter 7.3.2. in [3])

Note:

Conditions for CEC ON state and OFF state consist of AC-conditions (F_{on} , F_{off}) and Signal Amplitude. AC-conditions are directly specified in (see chapter 7.3.3. in [3]), while amplitude limits can be indirectly derived.

Based on specification of SP2 Steady State amplitudes, cable attenuation and return loss in [3], signals with minimal amplitude for SP3 can be calculated. It is to be noted that the frequency dependent attenuation of the coaxial interconnect, will lead to different steady state amplitudes for pulses with different pulse width (2UI, 3UI, 4UI, 5UI, 6UI). Due to this effect, for every stimulus with specific (different) frequency content its corresponding minimal amplitude must be calculated. In the context of this document this frequency (stimulus) dependent minimal amplitude will be referred to as "minAMP_ON".

As a general requirement, a CEC must be in ON state when AC-conditions are met and signal amplitudes equal or larger than the "minAMP_ON".

With valid AC-conditions for ON state, there is no amplitude limit specified in [3] to enforce CEC OFF state, nor can be directly derived. This is solely in the responsibility of the CEC-Supplier. Such test cases, listed below, are marked "for information only". The corresponding amplitude condition will be referred to as "maxAMP_OFF".

6.3.2 Measuring CEC Parameters – Signal Charts

The signal chart represents the graphical view of test sequence. It shows the location of the action points and provides the pre-requisites for the corresponding tests of the CEC parameters.

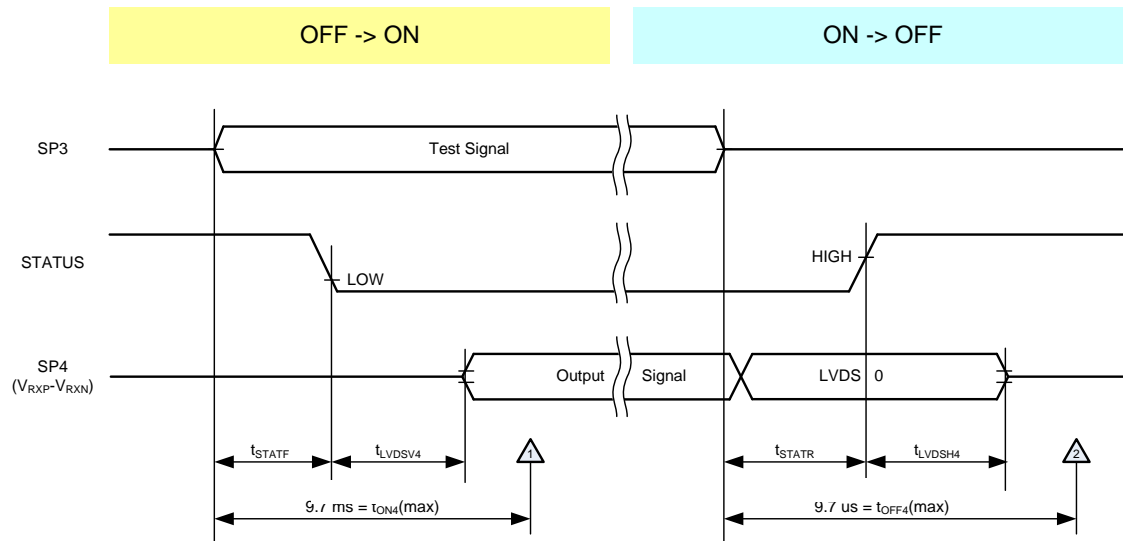


Figure 6-5: Measuring CEC Parameters: CEC Signal Chart No. 1

6.3.3 Measuring CEC Parameters – Test sequences

6.3.3.1 CEC Test Sequence #1 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V _{CCRX}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{RXN})	Disabled
Test Signal: Inputs	SP3	DC .. Continuous 10 kHz Square Wave
Output / Expected behavior	<p>CEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that I_{CCRX} > I_{CCSLEEP}(MAX)</p>	

Table 6-8: CEC Test Sequence #1

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the CEC. It is required that the CEC must remain in OFF state being supplied with input signal with frequency within F_{OFF3} requirements (assuming all other ON state requirements are met).

The CEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, I_{CCSLEEP}. During the Test Signal application the CEC is allowed to consume more than I_{CCSLEEP}.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values shall be tested.

6.3.3.2 CEC Test Sequence #2 - OFF-to-ON

“for information only”

Signal Chart	Figure 6-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{R_{XN}})	Disabled
Test Signal: Inputs	SP3	Continuous 12 MHz Square Wave Signal Amplitude < maxAMP_OFF (not spec.)
Output / Expected behavior	CEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that I _{CCR_X} > I _{CCSLEEP} (MAX)	

Table 6-9: CEC Test Sequence #2

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the CEC. It is required that the CEC must remain in OFF state being supplied with input signal with amplitude of less than maxAMP_OFF (assuming all other ON state requirements are met).

The CEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, I_{CCSLEEP}. During the Test Signal application the CEC is allowed to consume more than I_{CCSLEEP}.

6.3.3.3 CEC Test Sequence #3 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	$V_{CCR\bar{X}}$	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
	SP4 ($V_{RXP}-V_{RXN}$)	Disabled
Test Signal: Inputs	SP3	12 MHz Square Wave burst, Amplitude > minAMP_OFF, with duration $\leq t_{STATF(min)}$
Output / Expected behavior	CEC shall stay in OFF state with STATUS = LVTTL High and SP4 outputs disabled Note: With input stimulus present it is allowed that $I_{CCR\bar{X}} > I_{CCSLEEP(MAX)}$	

Table 6-10: CEC Test Sequence #3

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the CEC. It is required that, when all ON state requirements are met, the CEC must still remain in OFF state for at least $t_{STATF(min)}$ time.

The CEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, $I_{CCSLEEP}$. During the Test Signal application the CEC is allowed to consume more than $I_{CCSLEEP}$.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.4 CEC Test Sequence #4 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	$V_{CCR\bar{X}}$	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
	SP4 ($V_{RXP}-V_{RXN}$)	Disabled
Test Signal: Inputs	SP3	12 MHz Square Wave burst Amplitude > minAMP_OFF with duration > $t_{STATF(min)}$
Output / Expected behavior	CEC shall transition to ON state within time $t_{ON4(max)}$ with: STATUS = LVTTL Low within $t_{STATF(min)}$ to $t_{STATF(max)}$, and valid LVDS levels within $t_{LVDSV4(max)}$	

Table 6-11: CEC Test Sequence #4

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the CEC. It is required that, when all ON state requirements are met, the CEC must transition to ON state not earlier than $t_{STATF(min)}$ time, but also not later than $t_{ON4(max)}$.

Another requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.
- SP4 signal Timing: the SP4 signal must be LVDS compliant not later than $t_{LVDSV4(max)}$ after the STATUS is at LVTTL Low. This could be achieved with an oscilloscope, triggered off the STATUS signal falling edge, capturing the RXP and RXN signals. Only the data after $t_{LVDSV4(max)}$ needs to be evaluated, so a trigger delay needs to be used or removal of the corresponding amount of measurement data needs to be applied.

For this test, since the input signal is no MOST data, only the STATUS signal timing and SP4 LVDS compliance need to be checked.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.5 CEC Test Sequence #5 - ON-to-OFF

“for information only”

Signal Chart	Figure 6-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3	Continuous 12 MHz Square Wave Amplitude > minAMP_OFF
Initial State: Outputs	STATUS	LVTTL Low
	SP4 (V _{RXP} -V _{R_{XN}})	LVDS Compliant Signal
Test Signal: Inputs	SP3	Signal Amplitude < maxAMP_OFF (not spec.)
Output / Expected behavior	CEC shall transition to OFF state with STATUS = LVTTL High within t _{STATR} (max) and SP4 outputs disabled within t _{OFF4} (max), but not earlier than t _{LVDSH4} (min) after STATUS transitions High. After t _{OFF4} (max) time the current consumption shall be I _{CCCEC} < I _{CCSLEEP} (max)	

Table 6-12: CEC Test Sequence #5

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and shutdown mechanism of the CEC. It is required that the CEC must transition to OFF state being supplied with input signal with amplitude of less than maxAMP_OFF (assuming all other ON state requirements are met).

Another requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- SP4 signal Timing:
 - o The SP4 signal must transition to LVDS “0” within t_{STATR}(max) time after application of the Test Signal.
 - o The SP4 signal must maintain LVDS “0” for at least t_{LVDSH4}(min) after STATUS signal transitions to LVTTL High
 - o The SP4 outputs disabled within t_{OFF4}(max) time after application of the Test Signal.
- CEC power supply: t_{OFF4}(max) time after the application of the Test Signal, the CEC power consumption should be less than I_{CCSLEEP}(max).

To trigger the start of the electrical current measurement, the signal generator could assert trigger signal to the ampere meter t_{OFF4}(max) time after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

Multiple testing with different initial state signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.6 CEC Test Sequence #6 - OFF-to-ON

“for information only”

Signal Chart	Figure 6-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3	Stress Pattern with nominal bit rate (BR) Signal Amplitude < maxAMP_OFF (not spec.)
Initial State: Outputs	STATUS	LVTTL High
	SP4 (V _{RXP} -V _{R_{XN}})	Disabled
Test Signal: Inputs	SP3	Amplitude > minAMP_OFF
Output / Expected behavior	CEC shall transition to ON state within time t _{ON4} (max) with: STATUS = LVTTL Low within t _{STATF} (min) to t _{STATF} (max), and valid LVDS levels within t _{LVDSV4} (max)	

Table 6-13: CEC Test Sequence #6

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the CEC. It is required that the CEC must perform transition detection at its input and remain in or transition to ON state, being supplied with with input signal with amplitude of more than minAMP_OFF and frequency within F_{ON3} requirements.

Other requirements being checked are:

- STATUS signal timing – time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.
- SP4 signal Timing – The SP4 signal must be LVDS compliant not later than t_{LVDSV4}(max) after the STATUS is at LVTTL Low. This could be achieved with an oscilloscope, triggered off the STATUS signal falling edge, capturing the SP4 signals single-ended. Only the data after t_{LVDSV4}(max) needs to be evaluated for, so a trigger delay needs to be used or removal of the corresponding amount of measurement data needs to be applied.

Since there is no directly measurable marker to notify the CEC entering compliant ON state, an indirect method is used for the t_{ON4}(max) parameter evaluation: After the maximal allowed time has passed (end of t_{ON4}(max) – marked as Action Point 1 in the Signal Chart Figure 6-5) a check of ON state requirements is started.

For this test, along with STATUS at LVTTL Low requirement check, also the SP4 signal quality must be evaluated. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP4 signal quality. To assist the capture of the SP4 data, the signal generator could assert trigger signal to the oscilloscope t_{ON4}(max) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 10 ms.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.7 CEC Test Sequence #7 - ON-to-OFF

“for information only”

Signal Charts	Figure 6-5	
Initial State: Inputs	V _{CCR_X}	According to operating conditions
	SP3	Stress Pattern with nominal bit rate (BR) Amplitude > minAMP_OFF
Initial State: Outputs	STATUS	LVTTL Low
	SP4 (V _{RXP} -V _{R_{XN}})	LVDS Compliant Valid MOST Data
Test Signal: Inputs	SP3	Signal Amplitude < maxAMP_OFF (not spec.)
Output / Expected behavior	CEC shall transition to OFF state with STATUS = LVTTL High within t _{STATR} (max) and SP4 outputs disabled within t _{OFF4} (max), but not earlier than t _{LVDSH4} (min) after STATUS transitions High. After t _{OFF4} (max) time the current consumption shall be I _{CCR_X} < I _{CCSLEEP} (MAX)	

Table 6-14: CEC Test Sequence #7

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and shutdown mechanism of the CEC. It is required that the CEC must transition to OFF state being supplied with signal with amplitude below maxAMP_OFF (assuming all other ON state requirements are met).

Other requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- SP4 signal Timing:
 - o The SP4 signal must transition to LVDS “0” within t_{STATR}(max) time after application of the Test Signal.
 - o The SP4 signal must maintain LVDS “0” for at least t_{LVDSH4}(min) after STATUS signal transitions to LVTTL High
 - o The SP4 outputs disabled within t_{OFF4}(max) time after application of the Test Signal.
- CEC power supply: t_{OFF4}(max) time after the application of the Test Signal the CEC power consumption should be less than I_{CCSLEEP}(max).

To trigger the start of the electrical current measurement the signal generator could assert trigger signal to the ampere meter t_{OFF4}(max) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

Multiple testing with different initial state signal amplitudes is recommended. At least the minimal and maximal values must be tested.

7 Detecting Bit rate (Frequency Reference)

The bit rate is detected as follows:

Data-pulses range from 2 UI to 6 UI yielding 5 different pulse widths (2, 3, 4, 5, 6 UI). A clock at UI-rate represents a cycle time of 1 UI, which is twice the bit rate (i.e., for F_s 48 kHz, the bit rate is 147.45 Mbit/s, the UI-clock is 294.91 MHz).

A method of extracting the UI-clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. Then the bit rate is $\frac{1}{2}$ of the UI-rate.

The bit rate can be measured with MOST150 stress pattern or any other valid data pattern. Setup of the oscilloscope shall follow the general requirements using acquisition length of 10 MSamples and a sampling rate of 10 GSamples/s.

8 System Performance

The system-level specifications apply to an entire MOST network.

8.1 SP4 Receiver Tolerance

Unlike the link-level tests which use a pattern generator as the signal source, the system-level tests use live data from a fully formed MOST150 ring. Using the same eye diagram methodologies developed in chapter 4, a measurement is taken at SP4 of the Timing Master node. By taking the measurement in this way, one can quantify the total jitter accumulation around the ring. This measurement is applicable for every node in the network at SP4.

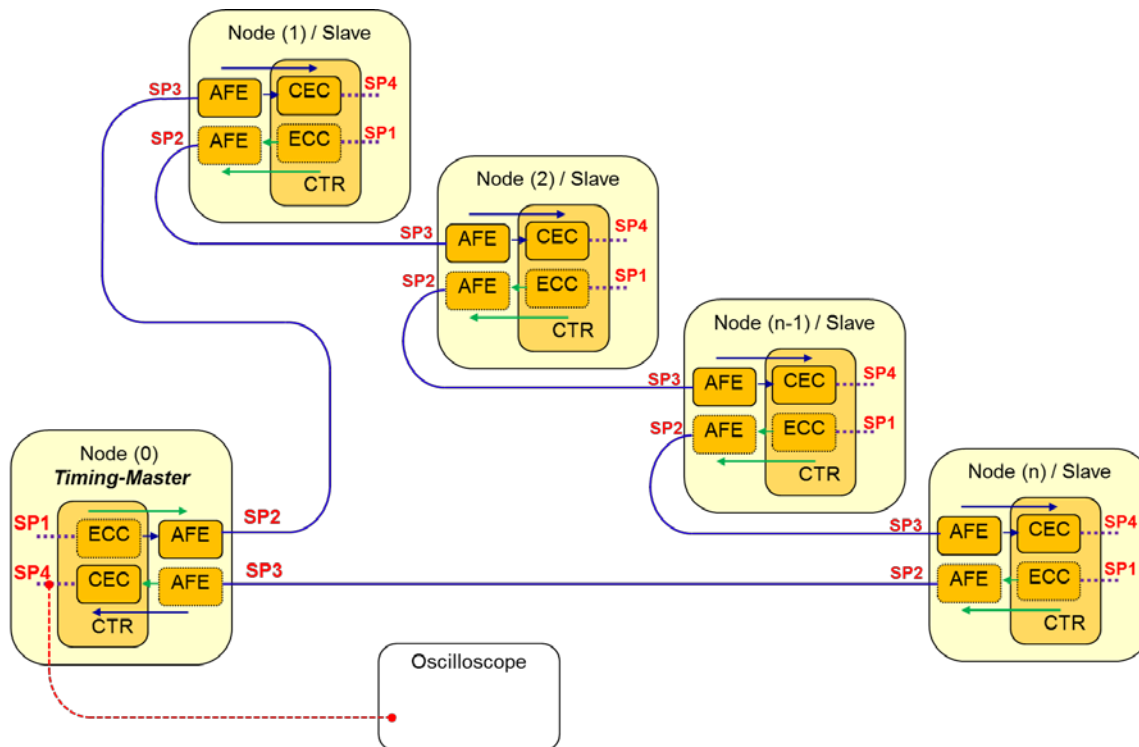


Figure 8-1: SP4 Receiver Tolerance Setup

8.2 Master Delay Tolerance

Master Delay Tolerance is a measure of end-to-end delay and phase variation between SP1 and SP4 of the Timing Master device. To ensure proper network operation, the total network delay must not exceed the specified maximum.

Following the setup diagram shown in Figure 8-2, the total delay can be measured on an oscilloscope.

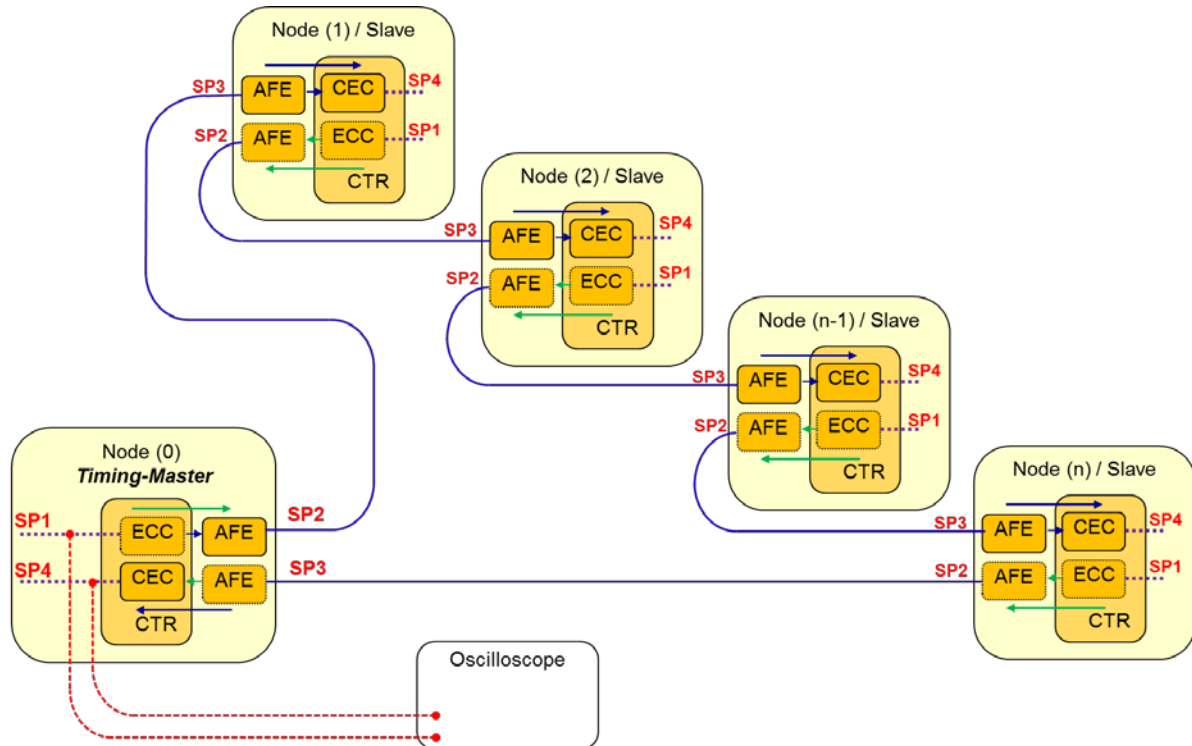
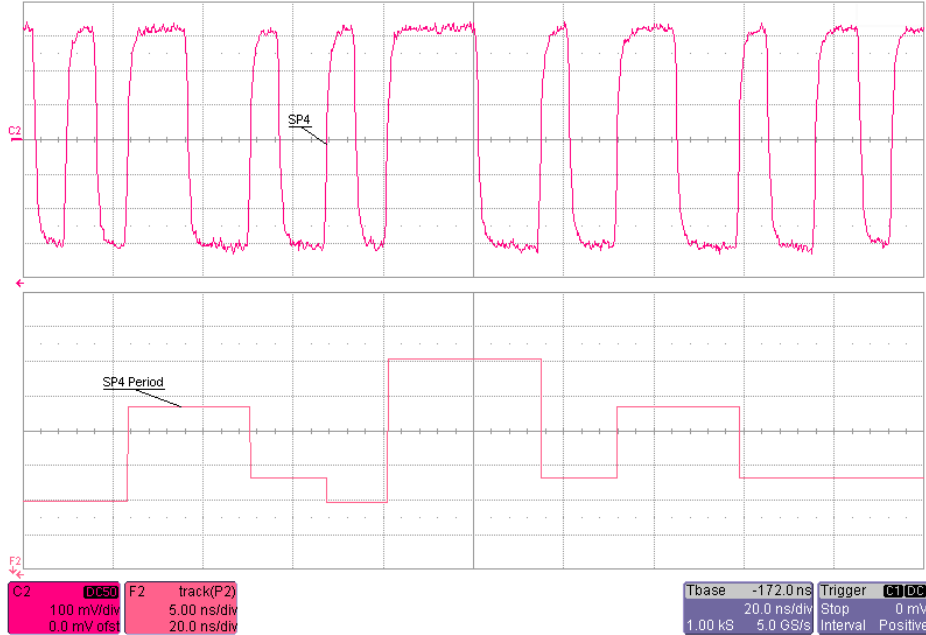
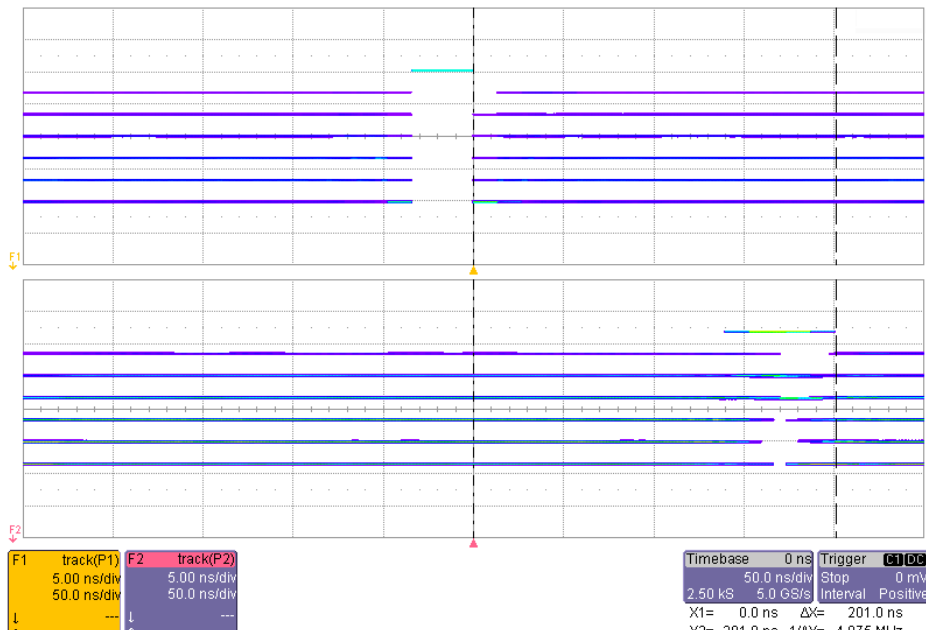


Figure 8-2: Master Delay Tolerance Setup

The following table describes the procedure used to measure the total delay. The oscilloscope used must be able to trigger on a specified period and have software functions for tracking periods. Two high-speed differential probes are required.

Step	Action
Acquiring a waveform	<p>For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP1 of the TimingMaster node. A second differential probe is connected to SP4 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels.</p> <p>The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP1. The interval should be set to $10 \text{ UI} \pm 0.5 \text{ UI}$. The <i>Trigger Mode</i> should be Normal.</p> <p>A sequence of the data stream ("waveform") is sampled into the scope's memory.</p>
Measure period	<p>The MOST150 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay</p>

Step	Action
	<p>between any two points in the network.</p> <p>Configure the oscilloscope to measure the period of both SP1 and SP4.</p>
Track the period	<p>Configure the oscilloscope to display a “Track” waveform for both SP1 and SP4 period measurements. This should result in two waveforms with time on the y-axis where the line indicates the length of the current period.</p> 
Measure the delay	<p>Configure the oscilloscope display to show only the SP1 and SP4 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP1 and SP4.</p> <p>Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP4 10 UI period. This is the Master Delay.</p> 

Appendix A: TBD

TBD

Appendix B: List of Figures

Figure 3-1: Detection of “high” and “low”	12
Figure 3-2: Example for detection of rise-time	13
Figure 3-3: Measurement Setup for evaluation Return Loss of coaxial interconnects.....	18
Figure 3-4: Measurement Setup for evaluation Return Loss of coaxial interconnects.....	19
Figure 3-5: Measurement Setup for evaluation Return Loss of PCB Interfaces	20
Figure 3-6: Measurement Setup for evaluation Return Loss of PCB Interface.....	21
Figure 4-1: Sub-categories of Phase Variation	27
Figure 5-1: SP2 Signal Quality Measurement Setup for Simplex and standalone Transceiver.....	36
Figure 5-2: SP2 Signal Quality Measurement Setup for Simplex and integrated Transceiver	36
Figure 5-3: SP2 Jitter Measurement Setup for Simplex and integrated Transceiver, Reference with Data from internal NI	37
Figure 5-4: SP4 Jitter Measurement for Simplex and standalone Transceiver.....	37
Figure 5-5: SP4 Jitter Measurement for Simplex and with integrated Transceiver	38
Figure 5-6: Directional Coupler	39
Figure 5-7: Crosstalk caused by directional coupler, measured with ideal 50Ohm	40
Figure 5-8: Crosstalk caused by directional coupler, in real setup.....	40
Figure 5-9: SP2 Jitter Measurement Setup for Duplex and standalone Transceiver.....	41
Figure 5-10: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver	41
Figure 5-11: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver, Reference with Data from internal NI	42
Figure 5-12: SP4 Jitter Measurement for Duplex and standalone Transceiver	42
Figure 5-13: SP4 Jitter Measurement Setup for Duplex and integrated Transceiver	43
Figure 5-14: SP2 Jitter Measurement Setup for Duplex and integrated Transceiver, Reference with Data from internal NI	43
Figure 6-1: Setup for Measuring ECC ON/OFF Parameters.....	45
Figure 6-2: Measuring ECC Parameters: ECC Signal Chart No. 1	46
Figure 6-3: Measuring ECC Parameters: ECC Signal Chart No. 2.....	46
Figure 6-4: Setup for Measuring CEC ON/OFF Parameters.....	54
Figure 6-5: Measuring CEC Parameters: CEC Signal Chart No. 1	56
Figure 8-1: SP4 Receiver Tolerance Setup.....	65
Figure 8-2: Master Delay Tolerance Setup	66

Appendix C: List of Tables

Table 3-1: Signal Level Measurement Interval	12
Table 4-1: Measuring Alignment Jitter	31
Table 4-2: Measuring Transferred Jitter	33
Table 5-1: component symbols	35
Table 5-2: signal impairments due to directional coupler	39
Table 6-1: ECC Test Sequence #1	47
Table 6-2: ECC Test Sequence #2	48
Table 6-3: ECC Test Sequence #3	49
Table 6-4: ECC Test Sequence #4	50
Table 6-5: ECC Test Sequence #5	51
Table 6-6: ECC Test Sequence #6	52
Table 6-7: ECC Test Sequence #7	53
Table 6-8: CEC Test Sequence #1	57
Table 6-9: CEC Test Sequence #2	58
Table 6-10: CEC Test Sequence #3	59
Table 6-11: CEC Test Sequence #4	60
Table 6-12: CEC Test Sequence #5	61
Table 6-13: CEC Test Sequence #6	62
Table 6-14: CEC Test Sequence #7	63

Notes: