

MOST

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST50 bPHY Compliance
Measurement Guideline**

**Rev 1.0
06/2019**

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Bibliography

All documents, which are referenced by this MOST document, are listed here along with their versions. For the current release status, please refer to the MOST Cooperation Document List.

Document		Revision
[1]	MOST Specification	3.1
[2]	MOST Basic Physical Specification	1.0
[3]	MOST50 bPhy Automotive Physical Layer Sub-Specification	1.0
[4]	MOST Compliance Requirements	2.3

MOST Document references

Document		Revision
[5]	JEDEC No. JESD8C.01 Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits	
[6]	DIN EN 50289-1-8 Communication cables - Specifications for test methods - Part 1-8: Electrical test methods - Attenuation	

Other Documents

Document History

Revision 1.0

Change Ref.	Chapter	Changes
1V0_001	All	Initial version.

Terminology and Abbreviations

Abbreviation	Explanation
AFE	Analog Frontend
A _J	Alignment Jitter
AWG	Arbitrary Waveform Generator
BALUN	Balanced-unbalanced
BEC	Balanced Media to Electrical Converter
BTR	Balanced Media Transceiver
BW	Bandwidth
EBC	Electrical to Balanced Media Converter
ISI	Inter-Symbol Interference
MNC	MOST Network Controller
PG	Pattern Generator
PLL	Phase Lock Loop
RBW	Resolution Bandwidth
SDA	Serial Data Analyzer
SMD	Surface Mount Device
SP	Specification Point
TDR	Time-Domain Reflectometer
T _J	Transferred Jitter
UI	Unit Interval
VNA	Vector Network Analyzer

1 General Remarks

1.1 Introduction

This document MOST50 bPHY Compliance Measurement Guideline specifies basic measurement methods, relevant for verifying compatibility of networks, nodes, modules, and components with the requirements specified in the documents MOST Basic Physical Specification [2] and MOST50 bPHY Automotive Physical Layer Sub-Specification [3].

This document shows basic measurement principles and setups for all specified parameters in [3]. There might be other options for determining parameters, which are more suitable for characterization and end-of-line testing in the supply chain. Selection and definition of an appropriate test strategy is in the responsibility of the supplier. However, all used measurement procedures shall provide measurement traceability to the basic principles shown in this document.

For the majority of parameters, the specification [3] is defined as an interface specification. Parameters and the requested performance ranges are stated for components sending into the interface. The same performance ranges need to be considered as input tolerances for components being connected to the interface as receiver. For verification of output performance of a component that sends into an interface, the input variations have to be considered – if they exist.

The process of compliance verification is defined in the MOST document MOST Compliance Requirements [4]. It describes how to achieve compliance certification for MOST subsystems (devices) and components.

For documentation clarity some values of MOST50 bPHY Automotive Physical Layer Sub-Specification [3] are used within this document. In case of discrepancies with the MOST50 bPHY Automotive Physical Layer Sub-Specification [3], the MOST50 bPHY Automotive Physical Layer Sub-Specification [3] shall be deemed the controlling document.

1.2 Operating Conditions

Temperature range for modules or components $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ according to [3].

Voltage range for modules or components $3.3\text{ V} \pm 5\%$ according to [3].

Note that there are functional requirements for the EBC within an extended voltage supply range according to [3].

1.3 Measurement Tools, Requested Accuracy

State-of-the-Art Tools:

- **Digital Oscilloscope**
 - DSO Type
 - ≥ 5 GS/s
 - BW ≥ 1.0 GHz
 - Sampling Memory ≥ 10 MSample
 - Active Probe (single-ended, differential)
- VNA (Vector Network Analyzer) or alternatively TDR (Time-Domain Reflectometer)
- **Ampere meter:**
 - Accuracy: better than 2 μ A
 - Optionally, Trigger input (for timing measurements)
- **Pattern generator for generating MOST50 stress pattern:**
 - BW 100 Mbit/s
 - Trigger output (for timing measurements)

Note: Depending on the chosen test-method and method to generate stimuli for the test, further equipment may be needed (e.g. electrical attenuator, discrete filter module to emulate cable transfer function, etc.). Performance requirements of such equipment need to be decided based on the particular use case. Performance variation of such equipment and impact on measurement results due to that, need to be considered.

2 Electrical characteristics

2.1 Test according to LVTTTL

Testing of devices, modules, or components has to be performed according to [5].

3 Specific characteristics for Balanced Media Interfaces and components

3.1 Threshold for detection of Alignment and Transferred Jitter

All jitter measurements are based on detection of edges in the data stream. Threshold for detecting edges is set to 0V of the differential signal (Zero-Crossing). DC-Offset in the measurements shall be minimized as it may indirectly compromise timing-parameter results, see section 5.1 and 5.2,

3.2 RMS Signal Amplitude

In MOST bPHY specification, output signal power boundaries for SP2 and minimum input signal power at SP3 is defined as RMS Voltage.

A waveform, signal voltage over time $v(t)$ is acquired on an oscilloscope. The RMS voltage of that waveform can be found by squaring that waveform, taking the mean (or average) of that squared waveform and then computing the square root.

$RMS = \sqrt{\frac{1}{N} \sum_{i=1}^N v(i)^2}$	<p>N: Observation length of the acquired waveform, N gives the number of samples with equidistant time interval</p> <p>$v(i)$: Amplitude at specific time steps</p>
--	--

RMS signal amplitude gives a representation of the average signal power $P_{av} = (Signal-Amplitude [VRMS])^2 / 100 \Omega [W]$. In order to get to a representative average value, it requires a longer term observation. Depending on chosen SP2 and applied channel losses, ISI impact will affect the signal to be measured. It may lead to locally distributed RMS minima and maxima when choosing only short snippets of the signal. In order to achieve sufficient statistical certainty, the acquired waveform shall have a minimum length of $>125\mu s$ ($125\mu s$ equals 6 frames with frame rate 48 kHz).

DC Offset in the measurements shall be minimized as it may indirectly compromise RMS signal amplitude results, see section 5.1 and 5.2,.

3.3 PSD of SP2 Output Signal

PSD as specified in [3] is used as a Link Quality criteria at SP2, which defines Signal Integrity requirements for the transmit Interface of a node. Main purpose is to limit pulse shape variations and inherently limit the transmitted signal bandwidth.

Several measurement options are available to perform spectral signal analysis. A method using time-domain data acquisition followed by FFT post-processing is given for reference. To ensure non-ambiguous measurements the method described below is recommended and will be applied as a reference procedure to resolve possible discrepancies.

PSD shall be measured with an RMS detector and using an effective RBW of 500 kHz. Beside directly measuring PSD with 500 kHz resolution bandwidth, this can be achieved by using lower RBW setting and averaging spectral results in n overlapping groups of the lower RBW bands to produce the effect of 500 kHz RBW sliding window (linear scale), (i.e., measurement with RBW 10 kHz, averaged in overlapping groups of 50 bands, therefore $n = 50$). To achieve statistical representation, the spectral density results of multiple trace segments are averaged to form the final result. The number of trace segments contributing to the averaged spectrum equals the sweep time.

Example Procedure:

- DUT Transmitter is configured to repetitively sending the MOST50 PSD Test Pattern
- Differential signal at terminated SP2 is measured with a differential probe. Other methods to measure a single ended representation of the differential signal are acceptable. (e.g. use BALUN or use test fixture with matched length 50 Ω coaxial cables, measured with 2 channels and mathematical combination)
- SP2 signal is being acquired with an oscilloscope. To reduce noise in measurement channel, use of averaging technique for time domain data acquisition is recommended. Selecting oscilloscope sampling rate and acquisition length leads to the inherent RBW for the acquisition, which is the reciprocal of the acquired duration time. Appropriate duration time can be achieved by adjusting horizontal oscilloscope settings accordingly or by acquiring longer traces and slice the trace into appropriate trace segments for the further processing.

Measurement Example: Acquisition length of 1 MSamples with sampling rate 10 GHz results in a duration of 100 μ s or inherent RBW of 10 kHz.

- For further post-processing, FFT algorithm can be applied on the oscilloscope or via processing per external script on a PC. In frequency domain, PSD is then formed as a moving average (linear scale) of n consecutive samples of the inherent RBW bands.

Measurement Example: This would need an overlapping of $n = 50$ inherent RBW bands to form effective RBW of 500 kHz.

- To achieve statistical representation, the spectral density results of multiple trace segments are averaged to form the final result. The number of trace segments contributing to the averaged spectrum equals the sweep time.

Measurement Example: 100 runs of above mentioned processing lead to a sweep time of 10ms

- Described procedure provides spectral density for consecutive 500 kHz bands in the relevant frequency range and can be directly compared with the limit lines.

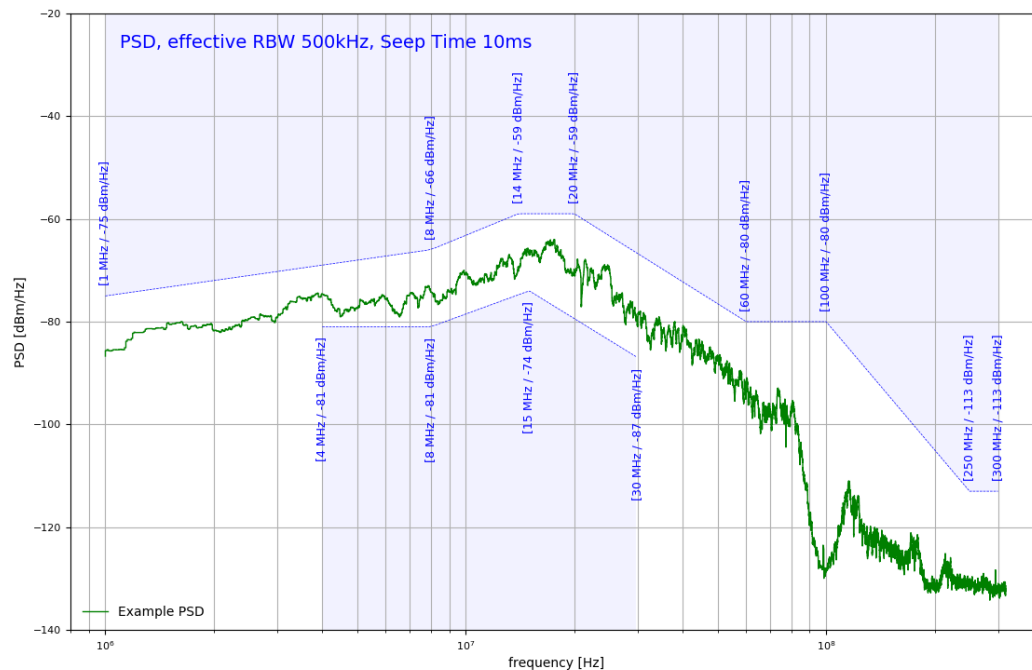


Figure 3-1: Example measurement for PSD

Performing PSD analysis can also be done with a spectral analyzer. The number of data points might be lower and not produce gapless data in the specified frequency range. Settings are applied that fit the above described processing.

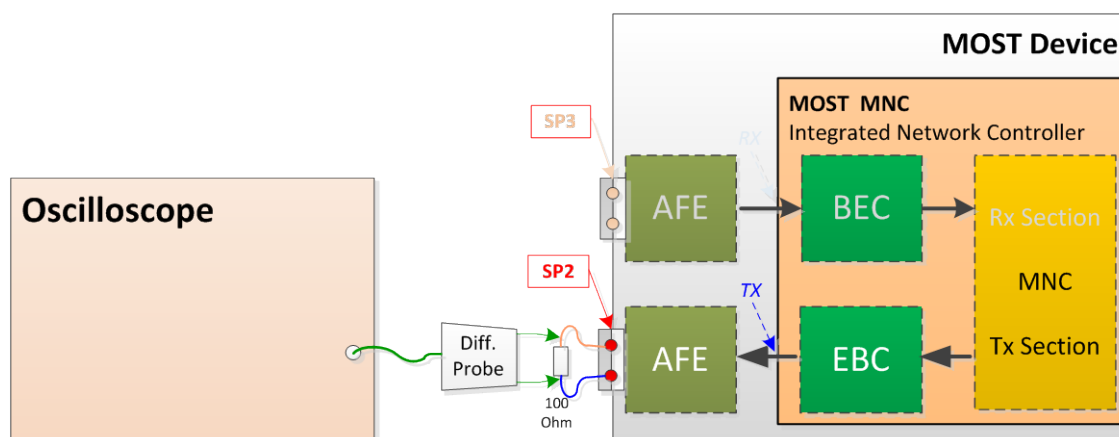


Figure 3-2: Test setup for measuring PSD with an oscilloscope

3.4 Attenuation of Electrical Interconnect

MOST bPHY limits the maximum attenuation for an Electrical Interconnect, formed of one or more cable pieces and the associated couplers and harness connectors. The total length of the Interconnect is limited to a maximum of 15m. The attenuation of such an Interconnect is frequency dependent. The MOST50 bPHY Automotive Physical Layer Sub-Specification [3] document specifies the maximum tolerable attenuation with a Limit line in the frequency range of 1 MHz to 66 MHz.

Attenuation requirement must be guaranteed for the full temperature range, automotive environmental conditions and over lifetime.

Test Setup:

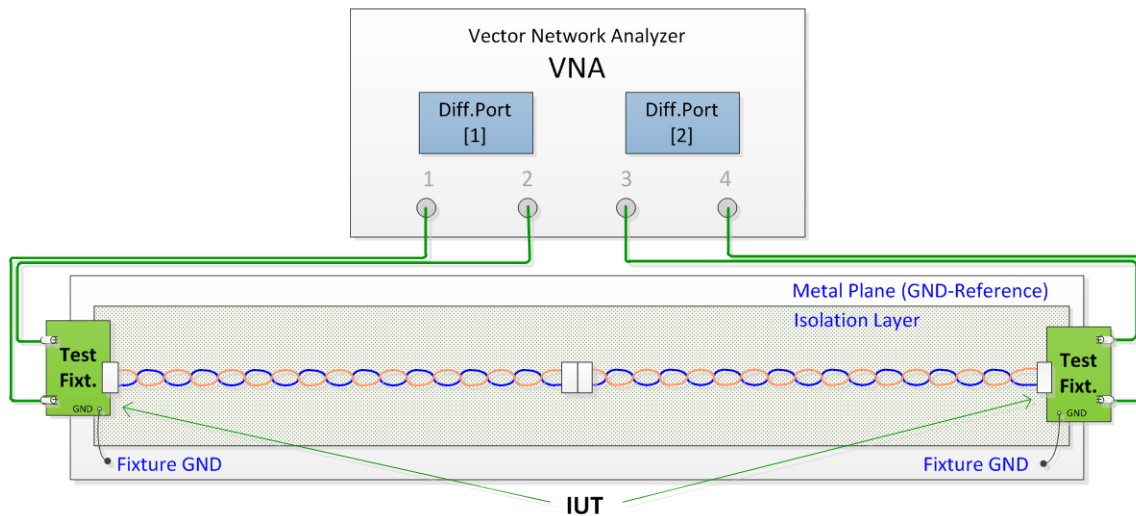


Figure 3-3: Test setup for measuring attenuation of an electrical interconnect

Test Procedure:

The evaluation of cable attenuation follows the principle as described in DIN EN 50289-1-8[6]. This is usually done with a Network Analyzer, using a 4-Port arrangement. Example setup is shown in Figure 3-3.

A Test fixture is being used to connect the differential cable system to the single ended Measurement Equipment. For details see Appendix A.

When acquiring a full set of the mixed mode S-Parameters for an Interconnect Under Test (IUT), extract the magnitude of the transfer characteristic from Differential Port 1 to 2 and vice versa (SDD21 and SDD12) in dB-Scale.

The cable attenuation varies with environmental conditions (e.g. temperature) and also depends on production process, properties of used materials and stability of geometric properties. It also depends on the way the cable under test is being arranged for the test.

The cable under test shall be placed on an arrangement with metal plane (GND-reference) at the bottom and an Isolation layer (thickness 10 mm, $\epsilon_r \leq 1.4$) on top. Cable shall be placed on top of the Isolation layer, cable shall be laid out with a minimum distance of 30mm between the cable portions (either meander shaped on a flat plane or cable assembled on a conductive drum with a minimum distance to each winding). GND of test fixture shall be connected to the metal plane.

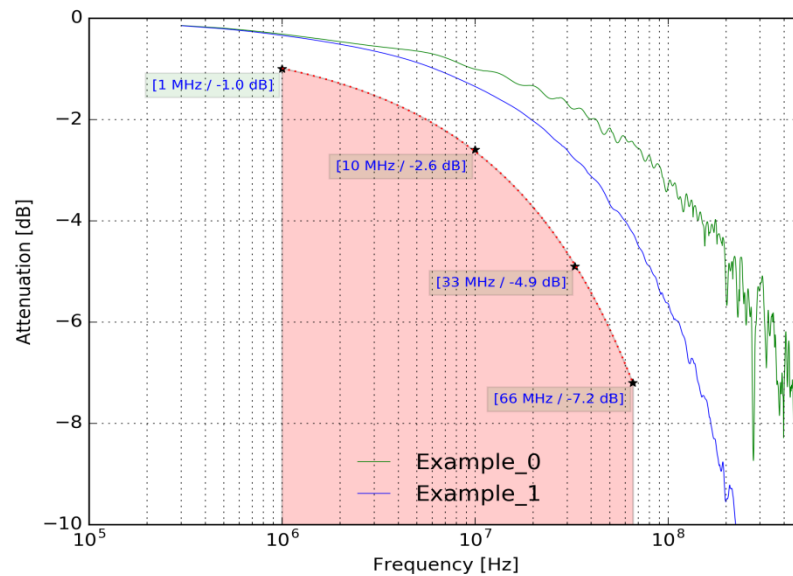


Figure 3-4: Example measurement of attenuation of an electrical interconnect

3.4.1 Impact of Attenuation on Data Signal

As specified in section 6.2.1 of [3], the attenuation characteristic of Electrical Interconnect follows a function of frequency. Therefore, the spectrum of a Data Signal being fed into such channel will be attenuated in a non-uniform manner. Attenuation on higher frequencies will stronger than on lower frequencies. In consequence, transition times will slow down (as they are controlled by the higher components of the relevant spectrum of the data signal). Shorter pulses of the signal may not achieve full amplitude swing anymore. The effect is usually described as Inter-Symbol Interference (ISI).

The graph in Figure 3-5 gives an example: The SP2-signal (blue) starts with a nearly uniform amplitude on all pulses. A small ISI effect is already visible, which is caused by AFE band-filtering. The SP3-Signal (green) shows the resulting signal shape after having past a typical electrical interconnect, more ISI is being added.

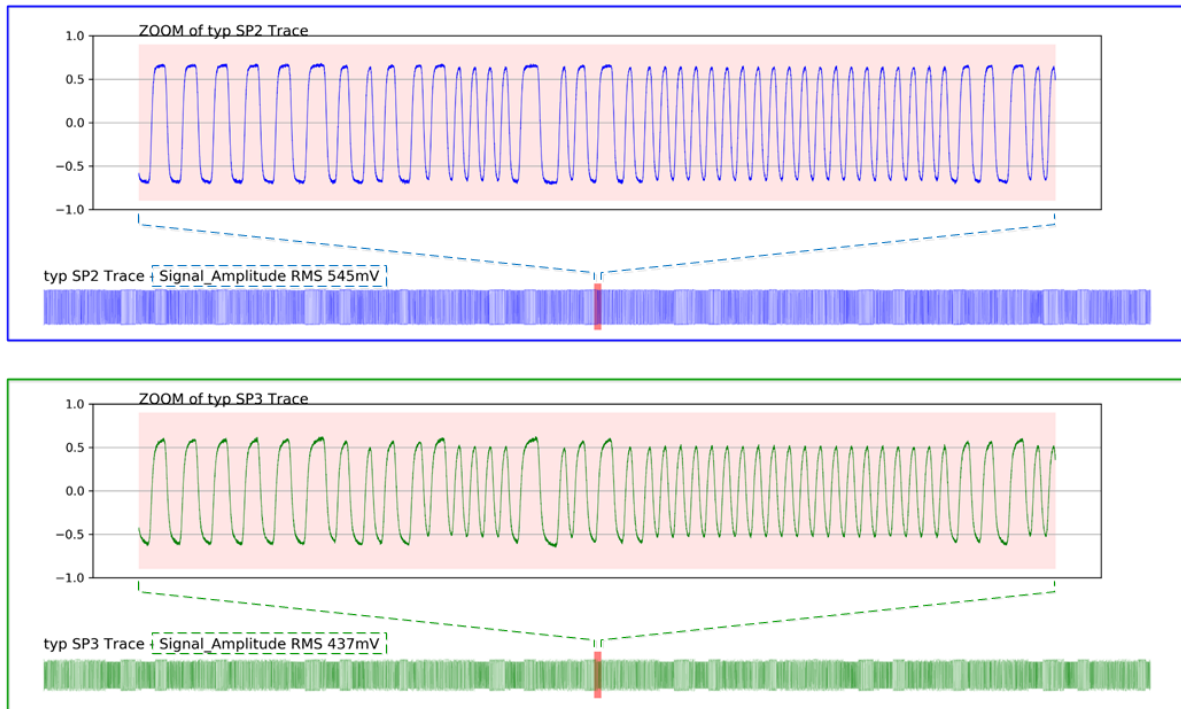


Figure 3-5: Example measurement of impact of attenuation on data signal

3.5 Characteristic impedance of balanced media

Characteristic impedance of balanced media shall be determined using time domain reflectometer and analyzing the space-resolved wave resistance. Alternatively, frequency domain measurement results can be taken and adequately transferred into time domain.

The minimum requirement to adequately evaluate the cable impedance in the context of the specified application is given by the rise time of the TDR signal; it shall be $< 1\text{ns}$. This considers $T_{r,TDR_min} = 0.35 / \text{maximum signal frequency}$, while maximum signal frequency is assumed with 3 times the UI-Rate (3rd harmonic). A recommended setup is to use a tester with at least 3.5 GHz (which corresponds to a rise time of max. 100 ps.) and use post-filtering to adjust for bPHY BW requirement.

A TDR instrument with two channels (CH1, CH2) is to be used. The two channels are to be adjusted differentially. The near end of the electrical interconnect under test is connected to the TDR measuring instrument in a suitable manner. The two wires of the pair are to be connected to the differential input of the measuring instrument. The two connection cables shall have the same HF characteristics and should match with respect to length, phase velocity and attenuation. At the connection level, the ground potentials of the two lines are to be connected to one another. The far end of the interconnect under test can remain open.

The TDR instrument may present the result as a readily processed differential Impedance profile. However, the result can also be displayed as two single ended impedance profiles. In this case, the differential impedance of the pair is the sum of the two individual impedances in the case of differential excitation: $Z_{0_cable} = Z_{TDR_CH1} + Z_{TDR_CH2}$

MOST50 bPHY Automotive Physical Layer Sub-Specification [3] does not define explicit requirements for impedance matching of connector and coupler components. Therefore, it is permitted to gate out area around the connector components. The interconnect under test must be evaluated from both ends.

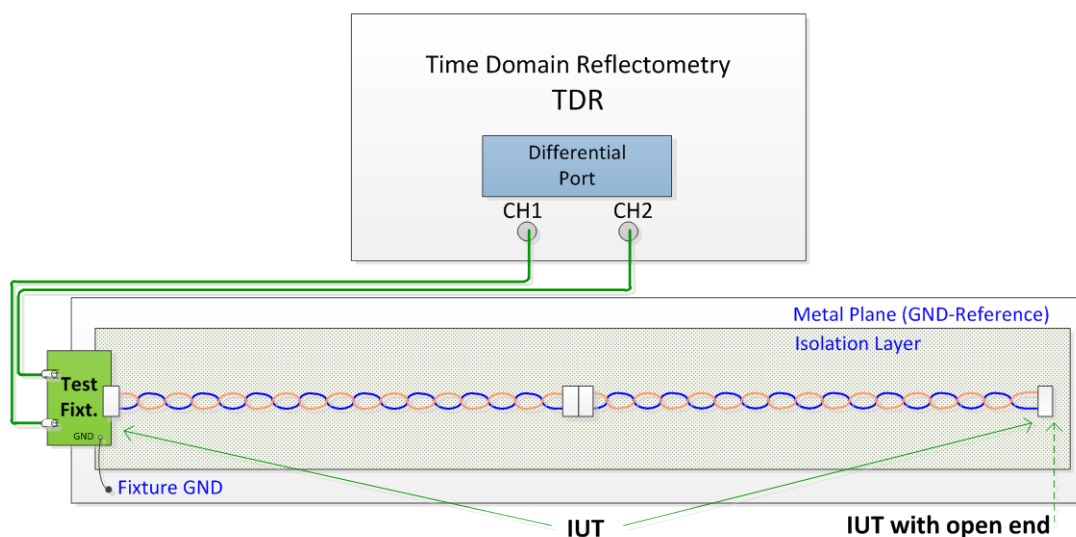


Figure 3-6: Test setup for measuring characteristic impedance of balanced media, stimulating left end of IUT

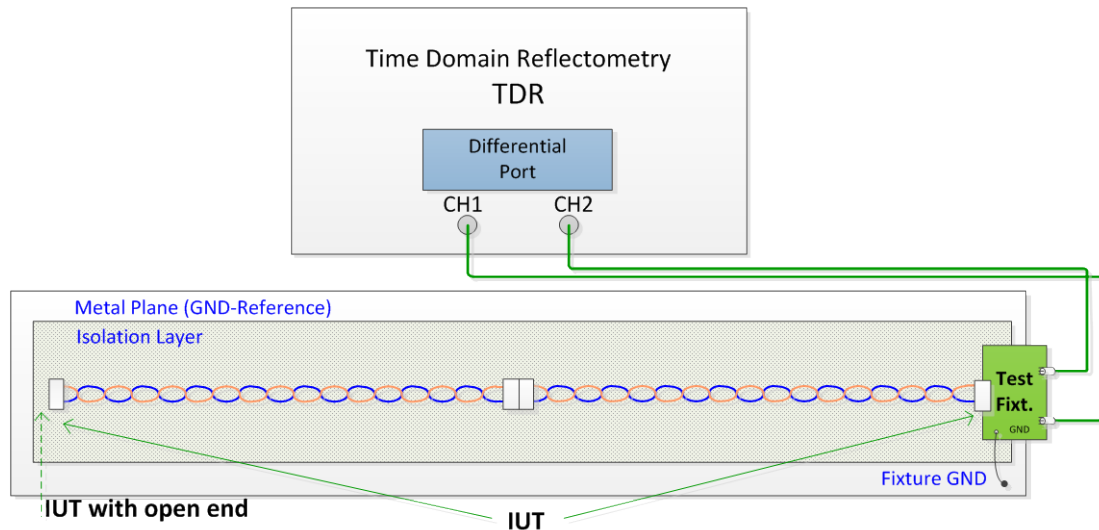


Figure 3-7: Test setup for measuring characteristic impedance of balanced media, stimulating right end of IUT

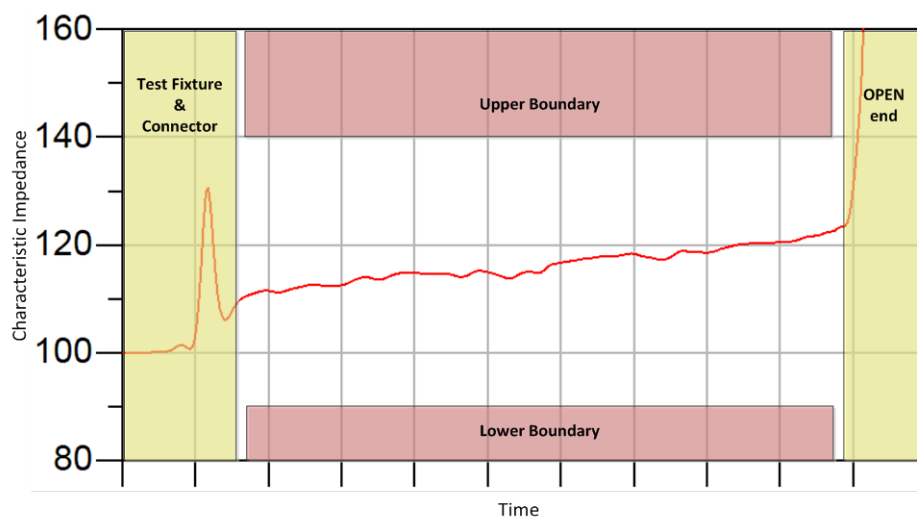


Figure 3-8: Example measurement for characteristic impedance of balanced media

3.6 Return Loss of PCB Interfaces

Signals going to or coming from balanced media interconnect are electrically connected on the PCB and finally end at the transceivers. The combination of board traces, passive components and board connector is summarized under the term analog front-end (AFE). This portion of the link should closely match the characteristic line impedance. Deviations in impedance matching will cause reflections; Return Loss is the ratio between transmitted and the reflected signal energy.

MOST50 bPHY Automotive Physical Layer Sub-Specification [3] defines a limit line in the frequency domain; the measurement however can be done in time – or frequency domain. The measurement setup is a differential single port configuration, emitting a signal into the PCB-Interface under test (SP2 and SP3) and measuring the reflected energy.

The result must be transferred to magnitude in dB scale and compared with the Limit Line.

A Test fixture is being used to connect the differential cable system to the single ended Measurement Equipment. For details see Appendix A.

Note: For Return Loss measurement of PCB interfaces, the ECU must be set into appropriate test mode. Supplier of MNC must enable appropriate test modes for SP2 and SP3 RL evaluation.

Test Mode	Test Case	Condition
SP2 Silent mode	Return Loss at SP2, RL_SP2	Test mode must ensure: <ul style="list-style-type: none"> EBC Impedance with AFE impairment detectable EBC does not emit data transitions
SP3 Silent mode	Return Loss at SP3, RL_SP3	Test mode must ensure: <ul style="list-style-type: none"> BEC Impedance with AFE impairment detectable No valid data signal present, while stimuli from TDR or VNA may occur
Note: Based on implementation of EBC and BEC functionality, the termination may be detectable in un-powered state of the MNC or may need MNC to be powered or may need the MNC to be powered and configured specifically. MNC vendors need to provide required information		

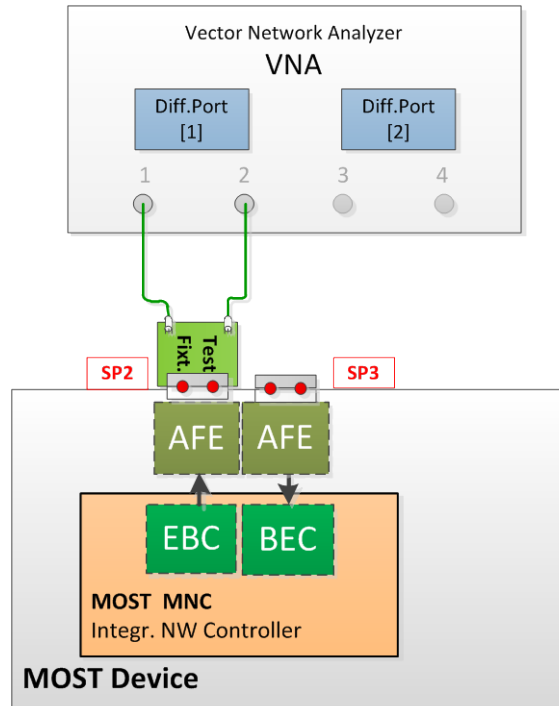


Figure 3-9: Measurement Setup for evaluation Return Loss of PCB Interfaces

MOST50 bPhy does not define specific requirements in resolution or scale of the frequency axis for RL. It is solely in the responsibility of the supplier to apply appropriate settings. Figure 3-10 shows valid example plot of Return Loss measurements for various PCB Interfaces.

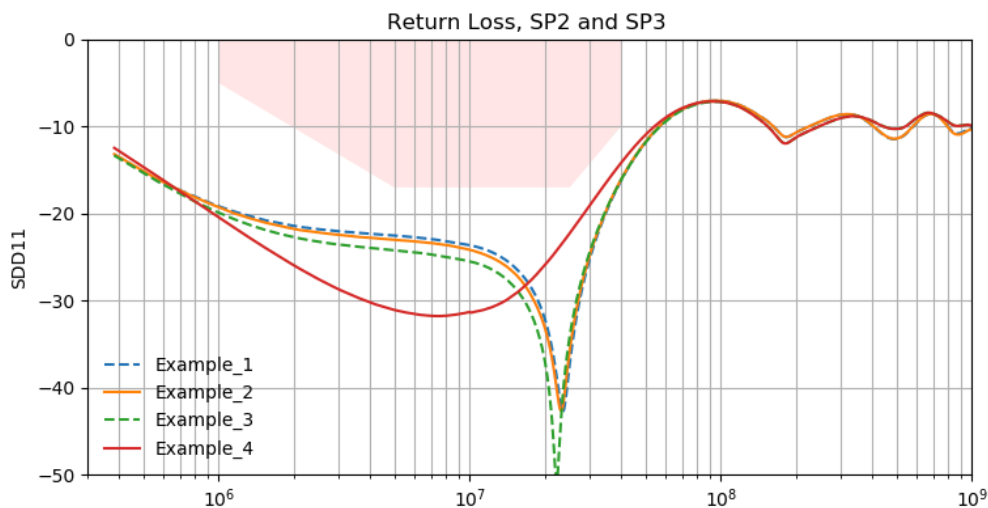


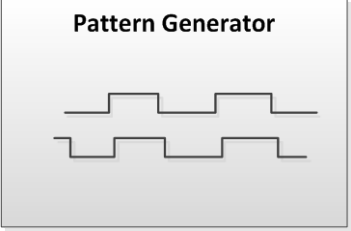
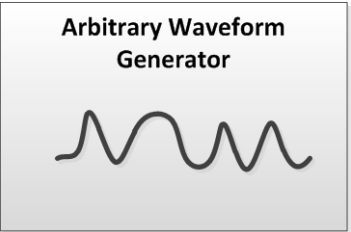
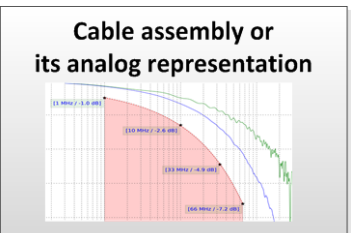
Figure 3-10: Example Return Loss measurement of PCB Interface

Time-Domain Reflection (TDR) is another valuable method to evaluate impedance characteristic of such PCB-interfaces. TDR sends a pulse into the DUT and measures response in magnitude and delay. The result usually is a plot of impedance over propagation time. In order to compare with the specified Limit Line in [3], TDR result need to be transferred to frequency domain.

3.7 Receive Tolerance

Evaluation of a Receive Tolerance means to apply *worst case* signals to SP3 and check the ability of the receiver to correctly recover clock and data. Challenge here is to find out what *worst case* means for a receiver, which conditions are relevant, and how to create such scenarios.

For better visibility, the block-diagrams in this section are showing simplified setups. Some general comments are listed below:

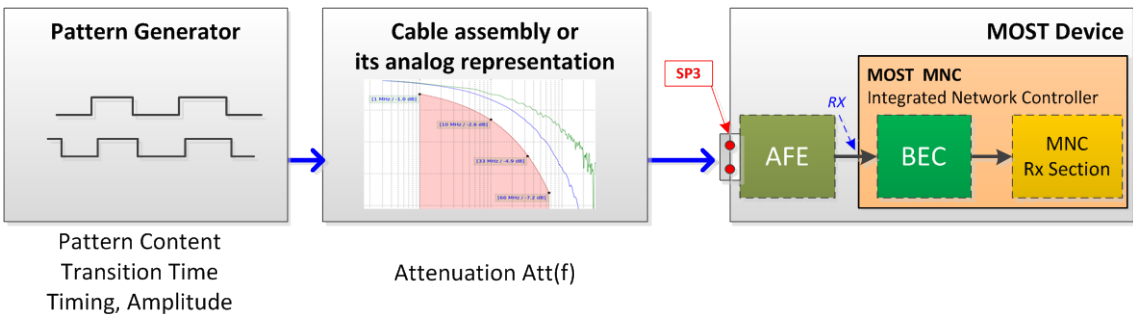
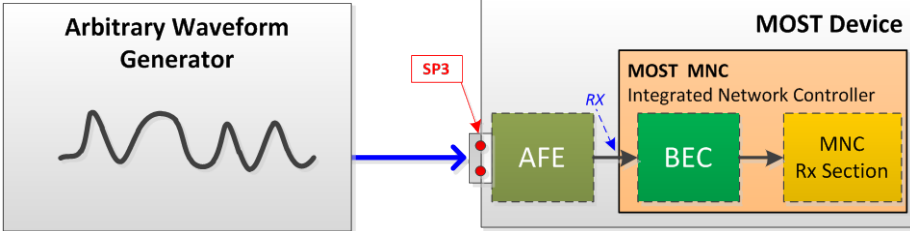
<i>graphical symbol</i>	<i>Description</i>
 <p>Pattern Generator</p>	<p>used to create MOST patterns, here mainly for SP2.</p> <p>Pattern Generator must be able to create Signals following SP2 Signal Quality requirements (e.g. differential output signal, variation within extremes of Timing Distortion, adjustable output voltage)</p>
 <p>Arbitrary Waveform Generator</p>	<p>used to create MOST patterns, for SP2 and SP3.</p> <p>used to emulate Pulse Shape and timing, which includes signal variations as produced by a differential driver in combination with variations added by AFE or/and electrical interconnects.</p>
 <p>Cable assembly or its analog representation</p>	<p>used to emulate Attenuation as produced by an electrical Interconnect. This can be either real cables with known transfer characteristics, analog modules emulating such cable transfer characteristic or combinations of both.</p>

3.7.1 Creating a Stimulus for SP3

Based on bPHY specification, the following impairments on Signal Quality at SP3 need to be considered:

- Valid MOST signal starts from SP2, all variations permitted by bPHY need to be taken into account (e.g. min/max RMS Amplitude, PSD, Jitter, etc.)
- Signal is attenuated when travelling through the interconnect (Attenuation(f))
- Some additional but minor losses will happen at the interface between cable and PCB due to Return Losses (SP3)
- For activity detection, other patterns (e.g. with lower frequency content) than valid MOST patterns have to be used. Signal with lower amplitude or additional attenuation may be used for evaluating on/off thresholds

There are 3 basic test setups which can be used to emulate above listed influences and stress an BEC under test. The following table explains the 3 configurations (A, B, C)

	Emulating EBC	Emulating Wire Harness	BEC under Test
	Pattern Generation / Signal Conditioning	Frequency dependent Attenuation	
	 <p>Pattern Content Transition Time Timing, Amplitude</p> <p>Attenuation Att(f)</p> <p>MOST Device</p> <p>MOST MNC Integrated Network Controller</p> <p>BEC</p> <p>MNC Rx Section</p> <p>SP3</p> <p>RX</p>		
[A]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10 kHz and up to 75 MHz MOST Stress Pattern	Use real cables in various combinations, requires pre-selected cables and components	
[B]	Pattern Generator, Signal Conditioner, Attenuator square wave, with frequency < 10 kHz and up to 75 MHz MOST Stress Pattern	Use specific circuitry, emulating cable characteristic with analog filters. A few characteristics may be combined on one PCB	
	 <p>Arbitrary Waveform Generator</p> <p>MOST Device</p> <p>MOST MNC Integrated Network Controller</p> <p>BEC</p> <p>MNC Rx Section</p> <p>SP3</p> <p>RX</p>		
[C]	Using an arbitrary waveform generator – combining signal generation with cable emulation: processing various patterns, incl. various signal conditions, adding frequency dependent attenuation Additional Attenuation may be needed!		

Note:

In case attenuator is needed, use either:

- Differential signal from generator and very symmetrical attenuation on both signal lines (P and N)
- Single ended signal from generator, attenuator followed by BALUN (conversion into Differential signal)

Pro / Cons of suggested setups:

Setup	PRO	CON
[A], [B]	wire harness / cable emulation can be re-used in real network-links, multi node networks, qualification testing, EOL testing, etc.	fixed structure, not adaptable, practically low number of test scenarios applicable
[C]	gives best flexibility in generating multiple stress- scenarios, easy adaptation in case new challenging configurations	not usable in real links, no re-use in other test areas.

4 Measurement of Phase Variation

4.1 Basics

Measurement of Phase Variation

Phase Variation describes data stream noise and distortion in the time domain. Based on spectral content of the variation, Sub-categories of Phase Variation are defined.

Phase Variation	Spectral limits
Wander	DC up to 10 Hz
Transferred Jitter (T_j)	Jitter with 10 Hz up the limit given by the Jitter Filter
Alignment Jitter (A_j)	Jitter with spectral content above the limit given by the Golden PLL

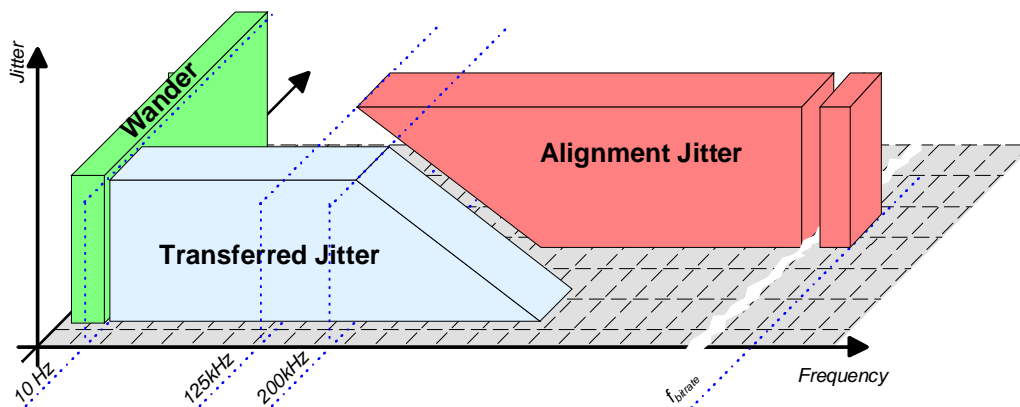


Figure 4-1: Sub-categories of Phase Variation

The need for separating T_j and A_j is founded in the synchronous approach of the MOST network. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node will recover the clock for sampling the input data out of the received data stream. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain correlation in phase between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). The PLL enables the capability of tracking of Phase variations. Phase variation in a lower spectral range on an incoming data stream will be compensated by aligning the clock's phase accordingly. Therefore, low frequency jitter will not impact the data recovery. However, the clock for generating the output data, which is derived from the recovered input clock, will be affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter cannot be tracked by the PLL and will lead to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum Alignment Jitter A_j) to be tolerated is defined with the eye masks for each specification point.

The dynamic characteristics of a PLL for a MOST node are covered by the physical layer specification with two definitions:

“Golden PLL”:

The “Golden PLL” is a model, given in the form of a transfer function representing a low pass filter. The “Golden PLL” serves two purposes.

1. It is used as a measurement tool for generating a time base which is required for forming eye diagrams and determining A_j at each SP along a link. The golden PLL must take data in from the measured SPs and generate a UI-clock. Based on the recovered UI-clock an eye diagram is drawn. Eye masks, defined for each SP give the limits for A_j respectively.
2. The “Golden PLL” describes the behavior of a MNC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass (or higher) will be tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass may lead to misalignment. The “Golden PLL” in combination with the eye mask for SP4 receiver tolerance describes the minimum A_j tolerance of a MNC’s receive section.

“Jitter Filter”:

The Jitter Filter is a model, given in the form of a transfer function representing a low pass filter. It serves two purposes.

1. It is used as a measurement tool for extracting Transferred Jitter (T_j) out of the total jitter.
2. Additionally, it describes the worst case jitter transfer characteristic over a MNC. Jitter below the spectral range described by the low-pass may be tracked by a PLL. The data stream being generated by this MNC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

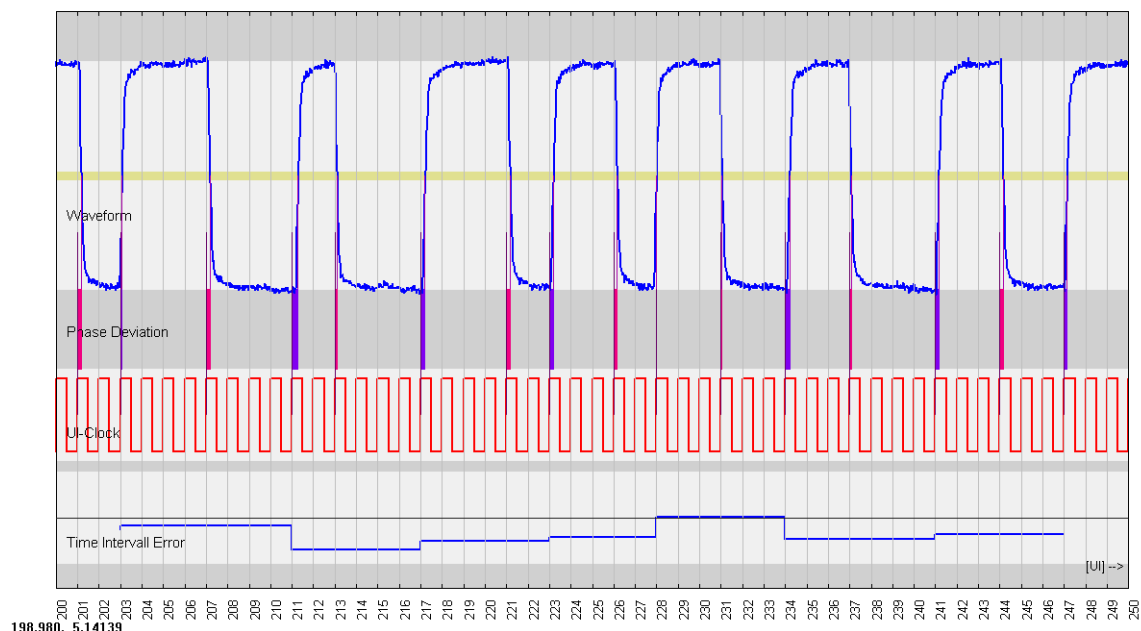
4.2 Measuring Alignment Jitter

The following table describes a procedure for detecting A_j out of a measured data stream. Oscilloscopes appropriate for the jitter measurements are Digital Sampling Oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	A probe (active differential or single-ended probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data stream ("waveform") is sampled into the scope's memory.
Clock recovery	<p>The DCA-coded MOST50 data stream contains clock and data. In a first step the clock must be extracted.</p> <p>Data-pulses range from 2 UI to 6 UI yielding 5 different pulse widths (2, 3, 4, 5, 6 UI). The required clock has a cycle-time of 1 UI, which is twice the bit rate (i.e., for F_s 48 kHz, the bit rate is 49.152 Mbit/s, the UI-clock is 98.304 MHz).</p> <p>A method of extracting the UI-clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST bPHY specifies that the "Golden PLL" is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p>

Example:

- UI-clock is fitted in frequency and phase to the waveform
- remaining phase deviations are marked in the diagram
- phase deviations for rising edges are shown in the "Timing-Interval Error" graph



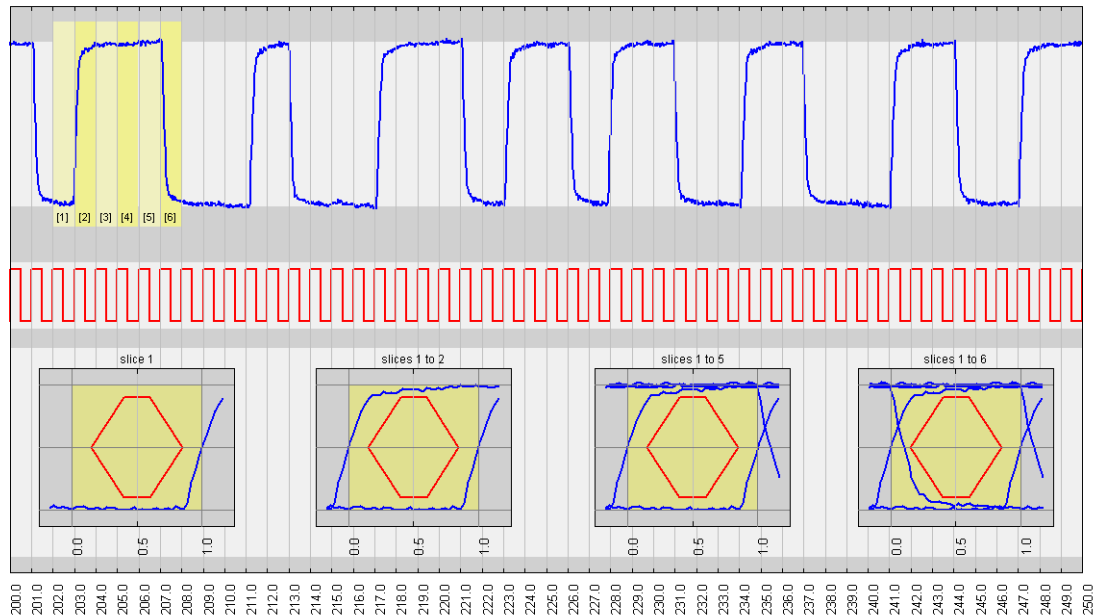
Note: In many oscilloscopes, visualization of the recovered UI-clock is not possible.

Applying Low Pass filter given by "Golden PLL"	Once a first derivate of the UI-clock is approximated, there may still be phase differences between rising data-edges and the recovered UI-clock, called "Time Interval Errors". Applying the low-pass filter (given by the "Golden PLL" model) to the sequence of consecutive "Time Interval Errors" results in a filtered phase-deviation sequence. This sequence represents the minimum
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	<p>capability of the MNC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI-clock need to be compensated by the sequence of filtered Phase-deviations.</p> <p>The resulting new UI-clock, which is used for further calculations, now represents the base UI-clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. However, modulation capability is limited in spectrum given by the “golden PLL” model.</p>
Calculating Alignment Jitter	<p>Alignment Jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI-clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over run-time in a graph result in an “A_J-Track” which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an “A_J-Jitter-Histogram”.</p>
Forming the Eye	<p>For drawing the eye diagram, the waveform is sliced in intervals of 1 UI length aligned with the UI-clock. The sliced waveform segments plus some overhead (i.e., 0.25 UI on both sides) are overlaid in one graph.</p> <p>Notes:</p> <ul style="list-style-type: none"> • <i>As shown in the diagram below, each transition is drawn twice, one time on the left side and secondly on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram.</i> • <i>Duty cycle distortion DCD, if it exists, will shift the eye towards the mask. In the shown example, LOW pulses are shorter than HIGH pulses. The UI-clock is referenced to rising edges which causes the rising edges to be adjusted to the UI-borders, while the falling edges are shifted by the amount of the DCD.</i>

Example:

- slice-sections are marked in the waveform graph
- sliced waveform segments are overlaid in a single diagram
- temporary results are shown



Pass/Fail-Test using Eye masks	<p>Signal integrity is checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error.</p> <p>The masks are defined by hexagons with points A, B, C, D, E and F. Points A and D are limiting A_V while B, C, E, F build constraints for amplitude and pulse-shape.</p>
Bit Error Rate	<p>The requested BER of 10^{-9} requires an eye diagram showing at least 10^9 bits without violation of the mask!</p> <p>1 Bit = 2 UI → at least $2 \cdot 10^9$ hits are required</p> <p>Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is in the responsibility of the user.</p>

Table 4-1: Measuring Alignment Jitter

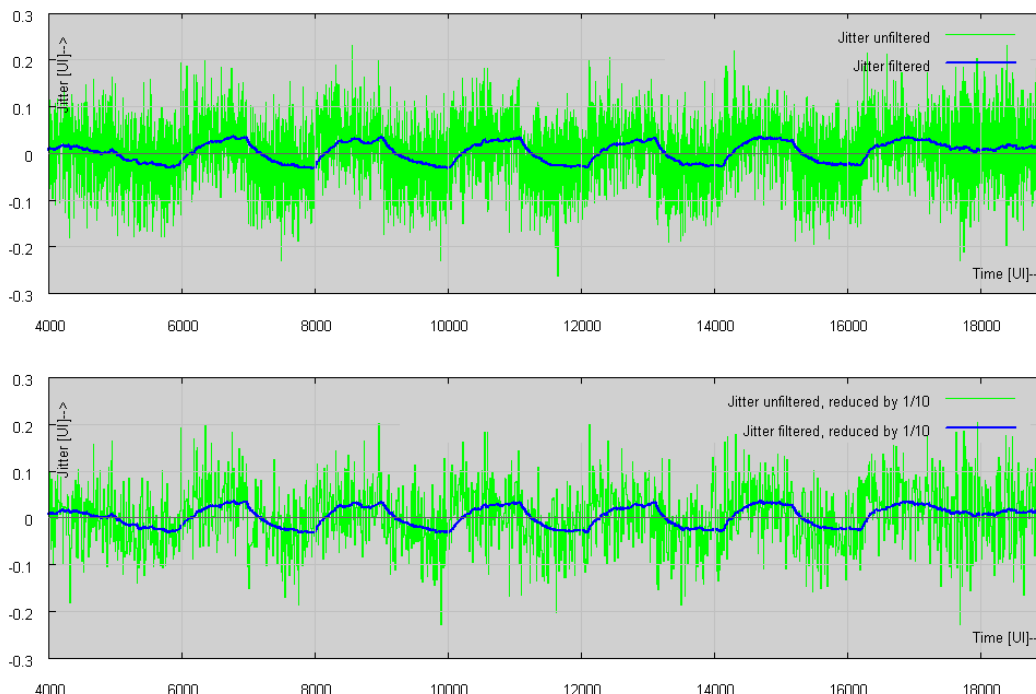
4.3 Measuring Transferred Jitter

The following table describes a procedure how to detect T_j out of a measured data stream. The following description will give a rough overview and will highlight some MOST specific features.

Step	Action
Acquiring a waveform	<p>For this measurement, the maximum available sampling memory of the oscilloscope has to be used. A probe (active differential or single-ended probe according to the SP under test) is connected to the DUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution (see b1/b0 detection, scaling channel/mask). A sequence of the data stream ("waveform") is sampled into the scope's memory.</p> <p>T_j is defined in the spectrum from 10 Hz (beyond Wander) and 100 kHz. The resolution of an oscilloscope low frequency jitter is limited by the size of memory.</p> <p>Note: <i>Even Oscilloscopes with very deep memory will hardly achieve 10 Hz resolution.</i></p>
Clock recovery	<p>Similar to the A_j Measurement procedure, the clock must be extracted. Clock separation is provided by an oscilloscope internal function.</p> <p>Similar to the A_j Measurement procedure, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency, the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.</p> <p>In contrast to the A_j Measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. However, smallest deviations in the detected bit-rate may grow up to a significant phase mismatch over the length of the acquired waveform and therefore affect further results. To enable a robust measurement procedure it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz).</p>
Extracting Transferred Jitter	<p>Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI-clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant, because only these deviations are tracked by the PLL and impact the recovered clock's phase.</p> <p>Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over run-time in a graph result in a "Jitter-Track".</p> <p>Successive phase deviations appear in pulse time intervals (2, 3, 4, 5, 6 UI), which correspond to the theoretical maximum jitter frequencies up to 50 MHz. With respect to the focused spectral range 10 Hz to 100 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process.</p> <p>In the next step, this "Jitter Track" (optionally reduced) needs to be low-passed, using the transfer function given with the "Jitter Filter" definition, which results in the "Filtered Jitter".</p>

Example:

- First graph: successive phase deviations are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")
- Second graph: successive phase deviations but reduced by factor 10 are shown over run-time ("jitter unfiltered"), weighting with the Jitter Filter leads to the low passed version ("jitter filtered")



Calculating Transferred Jitter

Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using root-mean-square method RMS.

$$RMS = \sqrt{\frac{1}{N} \sum_{i=1}^N v_i^2}$$

In case filtered jitter contains a DC-component or Wander (i.e., caused by a constant phase mismatch between clock and data), it is tolerable to calculate the Standard Deviation instead of RMS.

Note: This option is only applicable if the spectral content of eliminated jitter component, expressed by the mean-value, is below 10 Hz.

$$StdDev = \sqrt{\frac{1}{N} \sum_{i=1}^N (v_i - mean)^2}$$

Table 4-2: Measuring Transferred Jitter

5 Test Setups

5.1 Setups for SP2 Link Quality

This section discusses SP2 measurement setups, suggested to determine parameters as specified in [3]. Suggested setups are targeting evaluation of signal amplitude, PSD and timing distortion at the output of an ECU.

Note: For evaluating SP2 Link Quality, the ECU must be setup to an appropriate test mode. This is in order to deliver the appropriate test pattern for the respective parameter being tested. Supplier of MNC must enable such test modes for SP2 Link Quality evaluation.

Test Mode	Test Case	Condition
MOST50 Stress Test Pattern	SP2 Link Quality, <ul style="list-style-type: none"> Signal Amplitude RMS, V_{rms2} Alignment Jitter, acc. to Eye Mask A₂... D₂ Transferred Jitter, J_{tr2} 	Data signal at SP2 provides data content as specified for MOST50 Stress Test Pattern
MOST50 PSD Test Pattern	SP2 Link Quality, <ul style="list-style-type: none"> PSD, acc. to PSD Mask U1 ... U7, L1 ... L4 	Data signal at SP2 provides data content as specified for MOST50 PSD Test Pattern
SP2 Silent mode	DC-offset compensation for Sp2 Link Quality	Test mode must ensure: <ul style="list-style-type: none"> EBC Impedance with AFE impairment detectable EBC does not emit data transitions

Two possible options are shown:

Connect SP2 directly to two 50 Ω terminated oscilloscope channels and use MATH functions inside the oscilloscope to create the differential signal. A test fixture is being used to connect the differential port to the single ended measurement equipment. Matched single ended cable shall be used. For details see Appendix A.

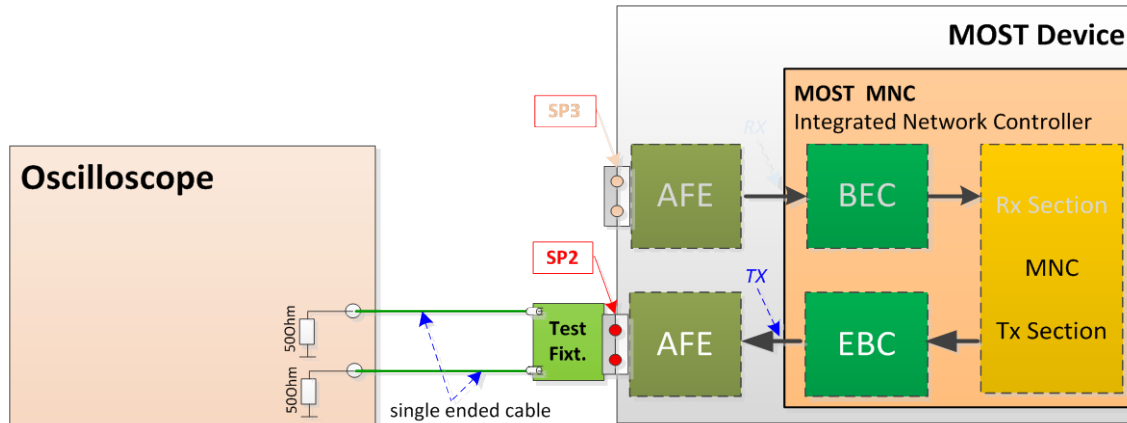


Figure 5-1: Measurement setup for SP2 – option 1

Alternatively, add a 100 Ω termination to the differential signal at SP2 and use a differential probe, connected to an oscilloscope channel.

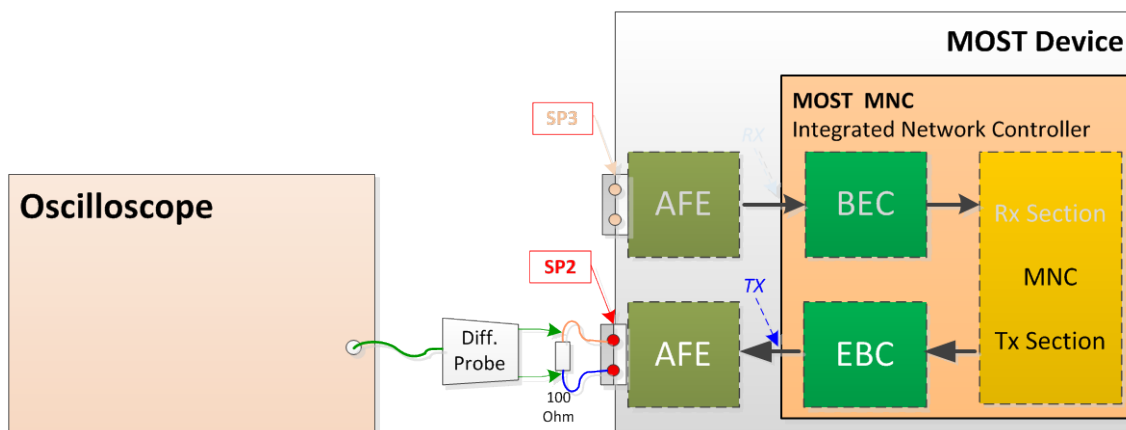


Figure 5-2: Measurement setup for SP2 – option2

Example, SP2 eye diagram:

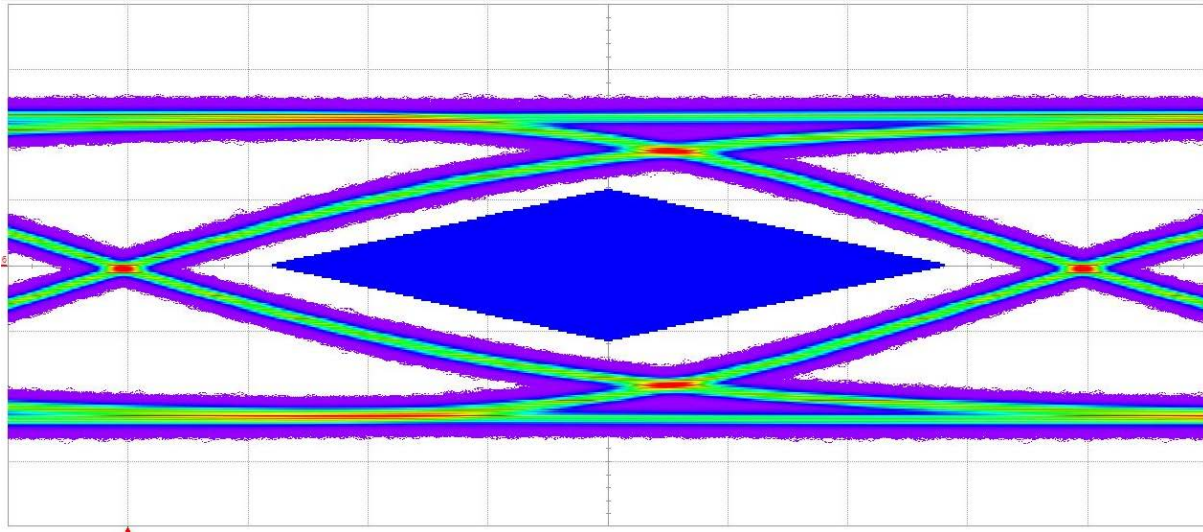


Figure 5-3: Example SP2 eye diagram

Compensation of DC-Offset:

DC-Offset in the measurements shall be minimized as it may indirectly compromise timing-parameter and RMS Signal Amplitude results. With Shown setups options, put the EBC into test modes "SP2 Silent Mode". The differential signal swing is zero and the common mode, due to AC-coupling in the signal path is expected to be zero. Any deviation of the common mode from zero is DC offset and need to be compensated.

5.2 Setups for SP3 Link Quality

This section discusses SP3 Measurement setups, suggested to determine parameters as specified in [3]. These setups are targeting evaluation of Signal Amplitude and Timing Distortion at the output of an ECU.

Signal Generation can start from a regular ECU, having MNC and AFE with SP2-compliant Signal Quality. Also a Signal Generator can be used instead.

Note: When evaluating SP3 Link Quality, for majority of tested parameters the MOST Test Pattern must be provided

Test Mode	Test Case	Condition
MOST50 Stress Test Pattern	SP2 Link Quality, <ul style="list-style-type: none"> Signal Amplitude RMS, V_{rms3} Alignment Jitter, acc. to Eye Mask A₃... D3 Transferred Jitter, J_{tr3} 	Data signal at SP2 provides data content as specified for MOST50 Stress Test Pattern
SP2 Silent mode	DC-offset compensation for SP3 Link Quality	Test mode must ensure: <ul style="list-style-type: none"> Signal Generator or EBC Impedance with AFE impairment detectable Signal Generator or EBC does not emit data transitions

Two options to connect to the oscilloscope are shown:

Connect SP3 directly to two 50 Ω terminated oscilloscope channels and use the oscilloscope's MATH functions to create the Differential signal. A test fixture is being used to connect the differential cable system to the single ended measurement equipment. For details see Appendix A.

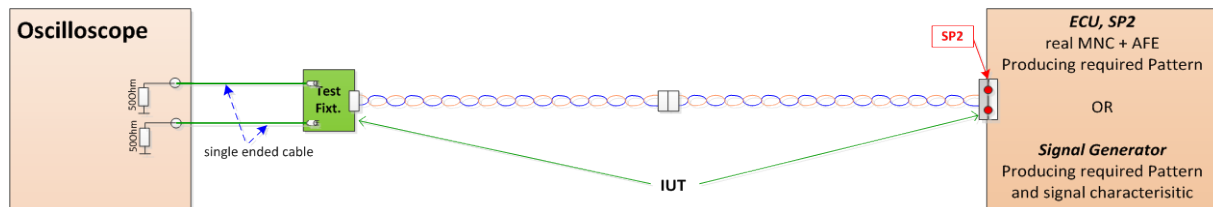


Figure 5-4: Test Setup for SP3 Link Quality – option 1

Alternatively, add a 100 Ω termination to the differential signal at SP3 and use a differential probe, connected to an oscilloscope channel.

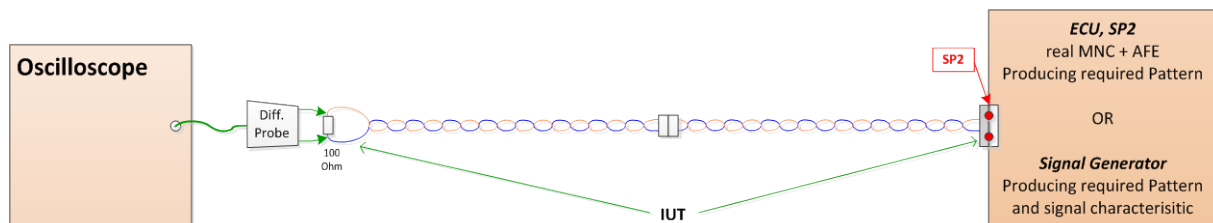


Figure 5-5: Test Setup for SP3 Link Quality- option 2

Example, SP3 eye diagram

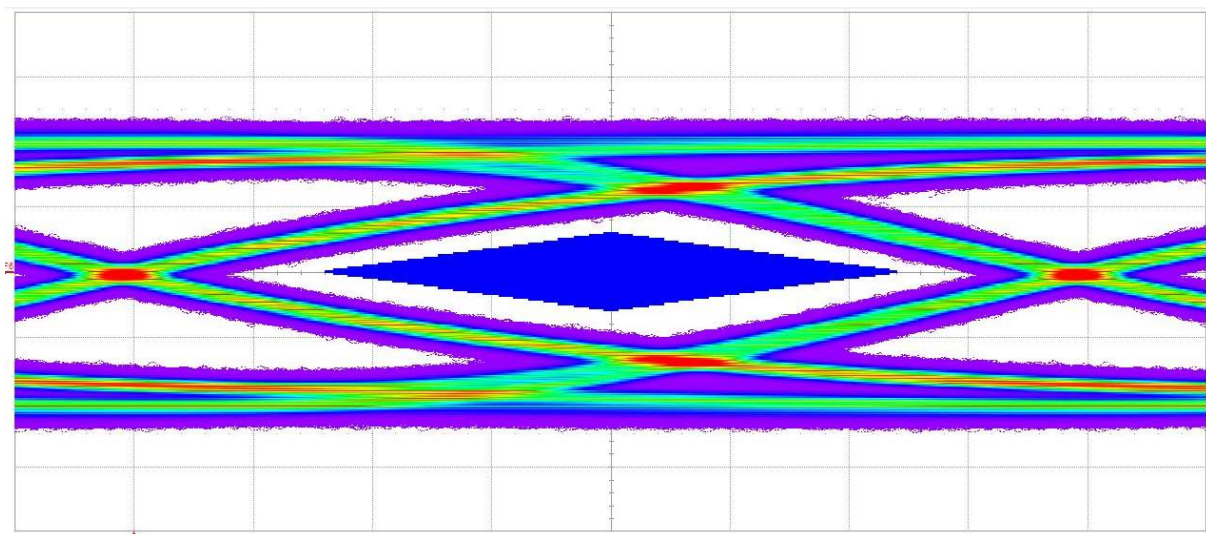


Figure 5-6: Example SP2 eye diagram

Compensation of DC-Offset:

DC-Offset in the measurements shall be minimized as it may indirectly compromise timing-parameter and RMS Signal Amplitude results. With Shown setups options, put the EBC or Signal Generator into test mode “SP2 Silent Mode”. The differential signal swing at SP2 is zero and the common mode, due to AC-coupling in the signal path, is supposed to be zero. Any deviation of the common mode from zero is dc-offset and need to be compensated.

5.3 Setups for SP3 Receive Tolerance

This section discusses SP3 Receive Tolerance setups. These setups are targeting the ability of an ECU Receive section to recover clock and data from a stressed input signal. General options to generate stressed signals is discussed in section 3.7.1 .

Option [A], [B] as described in in section 3.7.1:

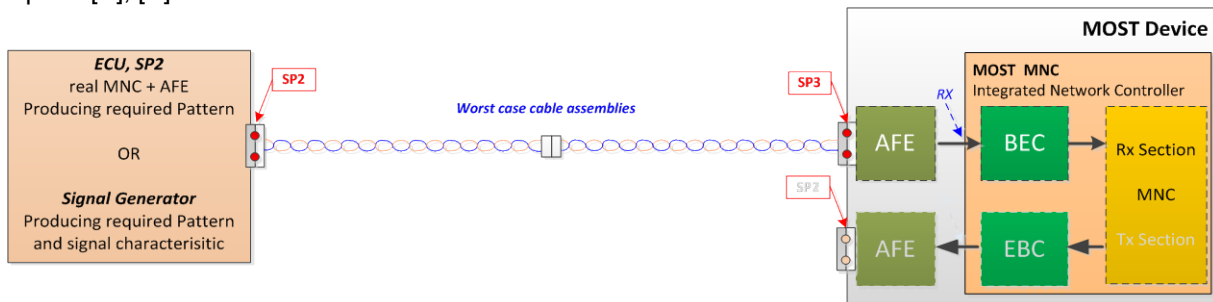


Figure 5-7: Test Setup for SP3 Receive Tolerance – option [A],[B]

Option [C] as described in in section 3.7.1:

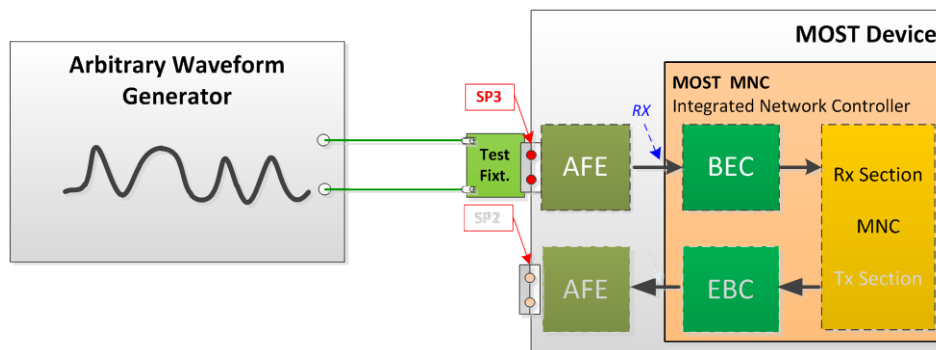


Figure 5-8: Test Setup for SP3 Receive Tolerance – option [C]

6 Power Up / Power Down

6.1 General considerations

The section defines several possible test setups and sequences needed to exercise functional EBC and BEC requirements and also provides guidelines for the interpretation of the results.

All test sequences must be performed for the minimum, typical, and maximum of Operating Supply Voltage according to Operating Conditions given in section 1.2.

All test sequences must be performed for the minimum, typical, and maximum temperature specification.

Some of the parameters defined by the Power Up / Power Down section of the Physical Layer Sub-specification could be measured directly (t_{STATF} , t_{STATR} , etc.), others however (t_{ON2} , t_{OFF2} , etc.) define relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured directly this chapter defines test sequences including a timeout, which represents the maximal (resp. minimal) time interval allowed for the respective parameter. The end of this is marked in the signal charts (e.g., Figure 6-2 as Action Point (Δ)) and appoints the time for a state validity evaluation.

E.g., $t_{ON2}(\max)$ time after the Reset signal goes HIGH start evaluating SP2 signal quality to check compliance to the requirements for "Valid Most Data".

Measuring Electrical parameters such as LVTTTL compliance is beyond the scope of this document and will not be discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

Testing of activity detection for EBC is described in section 6.2., followed by descriptions for BEC in section 6.3.

6.2 Measuring EBC Parameters

6.2.1 Measuring EBC Parameters – Test Setup

The diagram below outlines how a setup for measurement of the EBC performance could look like.

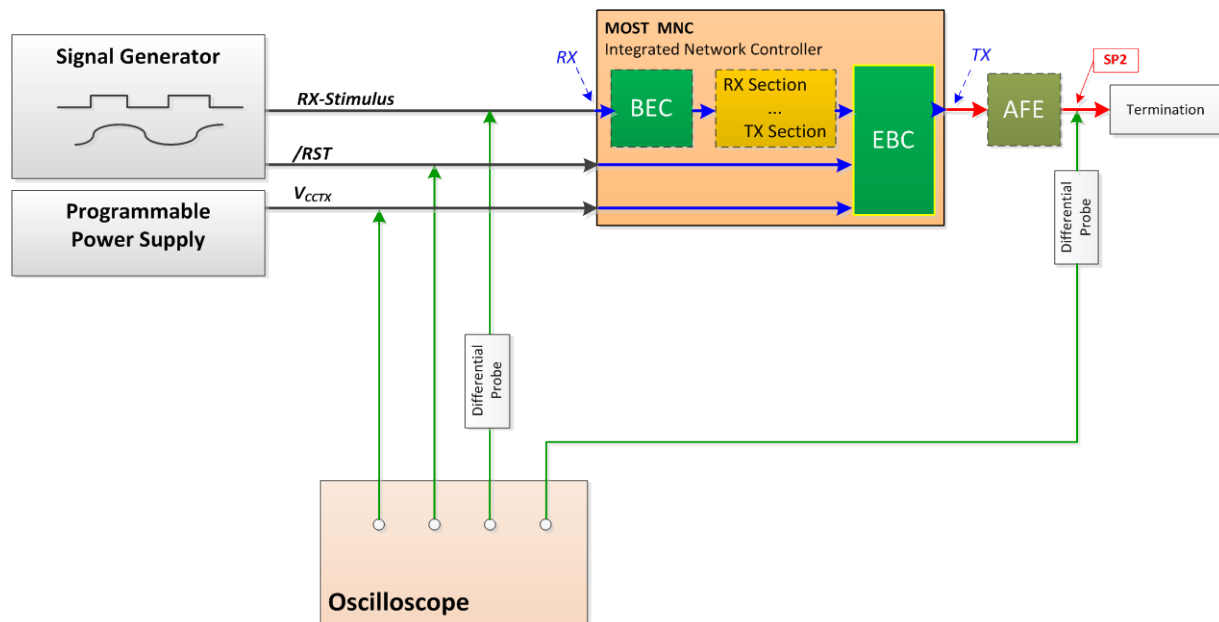


Figure 6-1: Setup for Measuring EBC ON/OFF Parameters

The main parts of the setup are:

- DUT: The DUT (Device Under Test)
 - o The EBC portion of a MNC is highlighted, relevant input signals for the test are shown.
 - o Stimuli Signals are shown directly connected to MNC, while Test Result is measured at SP2. The result can also be gathered directly at the MNC TX pins, excluding AFE impact.
- Signal Generator: Generator or Test Node used to produce the stimuli (Test Patterns) and control the EBC Power Supply.
- Termination: differential 100 Ω
- Oscilloscope: to capture input and output signals data.

Programmable power supply: to turn the EBC power supply on and off and to provide the desired supply voltage within given range for V_{EBC_OR}

6.2.2 Measuring EBC Parameters – Signal Charts

The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the pre-requisites for the corresponding tests the EBC parameters.

The EBC parameter testing requires a test sequence, while On/OFF behavior is controlled by /RST signal (*Figure 6-2*).

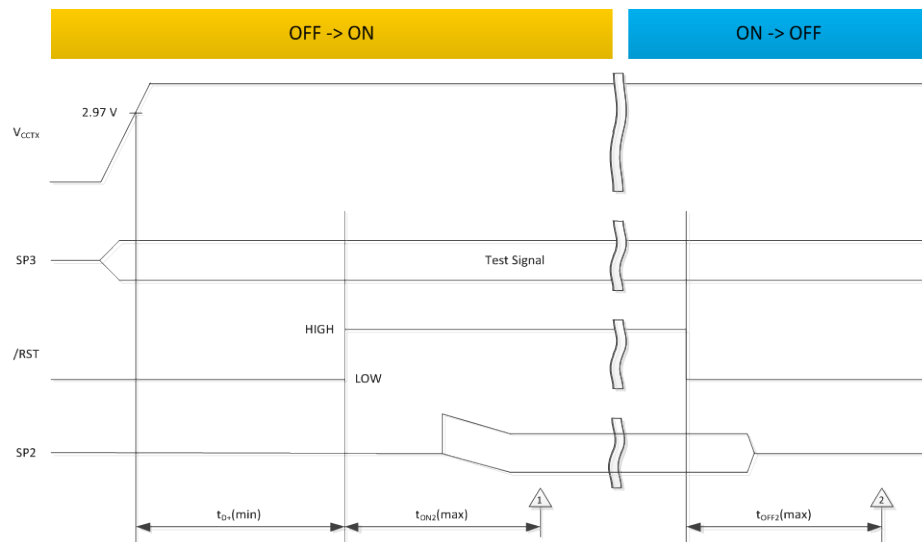


Figure 6-2: Measuring EBC Parameters: EBC Signal chart

6.2.3 Measuring EBC Parameters – Test sequences

6.2.3.1 EBC Test Sequence #1 - OFF-to-ON by /RST Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V_{EBC}	According to operating conditions
	/RST	LVTTL Low
	SP3	Valid Most Pattern with nominal bit rate (BR)
Initial State: Output	SP2	OFF state
Test Signal: Inputs	/RST	LVTTL High
Output / Expected behavior	EBC shall transition to ON state within time $t_{ON2(max)}$	

Table 6-1: EBC Test Sequence #1

This test sequence exercises the reset mechanism of the EBC. As a pre-requisite, valid MOST data must be present at the RX-input of the DUT (shown as “Test Signal” in Figure 6-2) or MNC must be configured in a way to produce TX data to the input of the EBC. It is required that the EBC must transition to ON state within a time $t_{ON2(max)}$ after the /RST signal has been driven low.

Another requirement being checked is the minimal allowed time for the /RST to be driven high after the power supply crosses the $V_T(min)$ voltage. There are two aspects for treating this parameter:

The first is the power supply application aspect; the reset generator providing the signal must be designed to ensure the /RST signal does not transition to LVTTL High before $t_{D+}(min)$ time has passed since the VCCTX measured on the EBC power supply pins crossed V_T .

The second is the EBC parameter aspect; the MOST50 bPHY Automotive Physical Layer Sub-Specification [3] states that when being supplied with an operating voltage within V_{CCTXGR} , the internal circuitry of the EBC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+} . By driving the reset signal High at the $t_{D+}(min)$ time it is checked if the EBC complies to that specification.

Since there is no directly measurable marker to notify the EBC entering ON state event, an indirect method is used for testing the $t_{ON2(max)}$ compliance: After the maximal allowed time has passed (end of $t_{ON2(max)}$ – marked as Action Point 1 in the EBC Signal Chart *Figure 6-2*) a check of ON state requirements is started.

For this test the SP2 signal quality must be checked. For this the oscilloscope starts capturing data sequence at Action Point 1, which will be used for testing the SP2 signal quality. To assist the capture of the SP2 data in ON state, the signal generator could assert trigger signal to the oscilloscope $t_{ON2(max)}$ after activation of the test signal. Alternatively (if the signal generator does not have enough outputs) scope can be triggered off the SP1 signal with a post delay of 100 μs .

6.2.3.2 EBC Test Sequence #2 - ON-to-OFF by /RST Signal

Signal Chart	Figure 6-2	
Initial State: Inputs	V_{EBC}	According to operating conditions
	/RST	LVTTL High
	SP3	LVDS compliant Stress Pattern with nominal bit rate (BR)
Initial State: Output	SP2	ON state
Test Signal: Inputs	/RST	LVTTL Low
Output / Expected behavior	EBC shall transition to OFF state within time $t_{OFF2}(\max)$	

Table 6-2: EBC Test Sequence #2

This test sequence exercises the reset mechanism of the EBC. It is required that the EBC must transition to OFF state within a time $t_{OFF2}(\max)$ after the /RST signal has been driven low and it must stay in OFF state as long as /RST is driven low.

Since there is no directly measurable marker to notify the EBC entering the OFF state event, an indirect method is used: After the maximal allowed time has passed (end of $t_{OFF2}(\max)$) – marked as Action Point 2 in the EBC Signal Chart Figure 6-2) a check of OFF state requirements is started.

The oscilloscope must capture the SP2 output and evaluate the time after the point marked as Action Point 2 to ensure the OFF state requirement is met.

A signal marker could be produced from the signal generator after $t_{OFF2}(\max)$ time has elapsed since switching the switching /RST signal low to allow triggering the oscilloscope.

Note: Long dataset capture is preferred, since the hold-off time that accompanies repetitive capture can lead to missed events.

6.3 Measuring BEC Parameters

6.3.1 Measuring BEC Parameters – Test Setup

Testing of BEC's activity detection includes the full variety of scenarios being influenced by outer conditions, such as ac-conditions as specified in [3], SP2 signal performance of the preceding node, attenuation of electrical interconnect, etc. It is impossible depict all possible combinations of variations, nor is it possible to test them 100%. It is in the responsibility of the BEC supplier to perform tests that produce maximum stress for BEC under test and the selected mode of operation.

Physical Layer Specification defines a set of functional requirements and performance parameters that BEC has to meet. The diagram in Figure 6-3 outlines how a setup for measurement of the performance of BEC could be realized.

Among many setup options two examples are shown below:

This setup can be used to check BEC response on an ECU. With stimulated events, response of STATUS signal can be measured. Further, for a functional verification, the resulting TX-Signal can be further used and connected via AFE to further nodes.

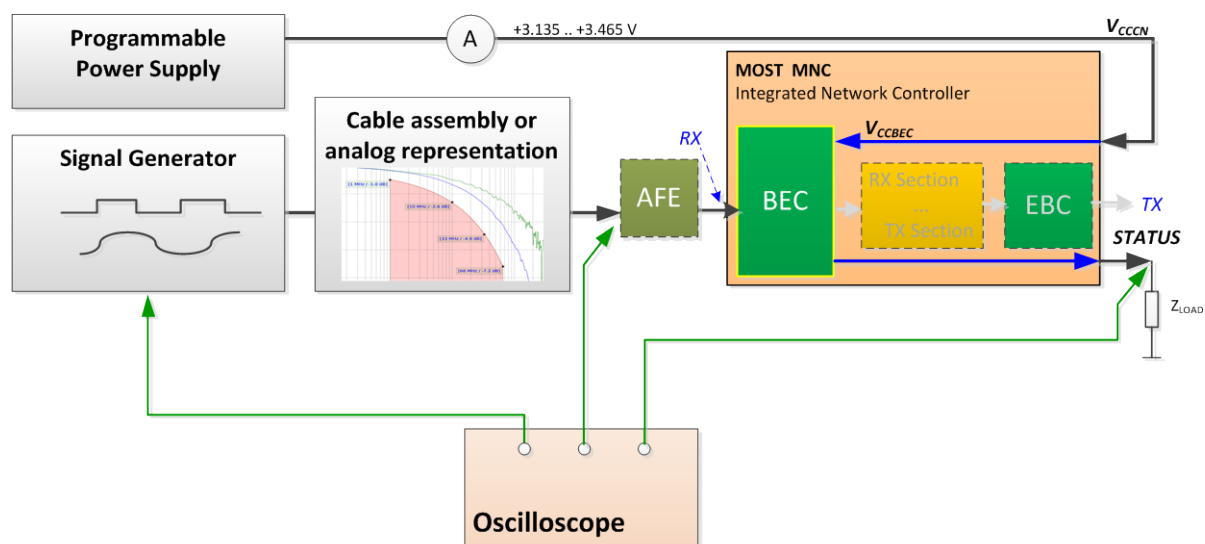


Figure 6-3: Setup 1 for Measuring BEC ON/OFF Parameters

The setup shown in Figure 6-4 can be used to check BEC response on Chip Level (MNC). Stimulation with Arbitrary Waveforms include all relevant impairments.

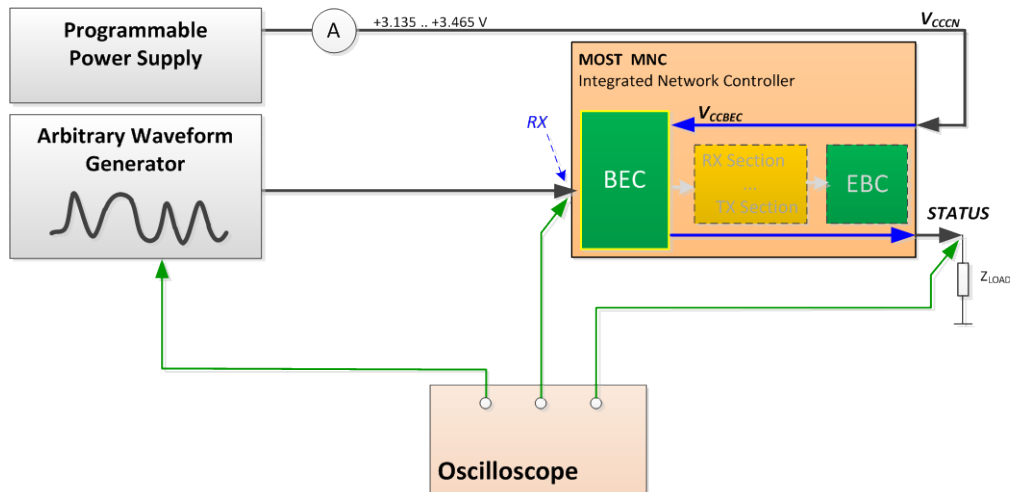


Figure 6-4: Setup 2 for Measuring BEC ON/OFF Parameters

The main parts of the setup are:

- DUT: (Device Under Test)
 - o The BEC portion of a MNC is highlighted, relevant output signals for the test are shown.
 - o Stimuli Signals are shown directly connected to MNC's RX-pins or introduced via SP3.
 - o Response and timing are directly measured at the STATUS Pin.
 - o Functional verification can be realized by detecting activity on the DUT's TX signal or SP2 signal.
- Programmable Power Supply: to vary supply in given Range for V_{BEC_OR}
- Signal Generator: Generator or Test Node used to produce the stimuli (Test Patterns) followed by Cable Assembly or analog cable representation
 OR
 Arbitrary Waveform Generator
- Oscilloscope: to capture input and output signals data.
- (Micro-)Ampere meter: to measure the current consumption of the BEC device in OFF state.

Signal Generator shown in Figure 6-4 emulates the SP2-interface in a real network. Therefore, output signal amplitudes have to follow the specified characteristics for SP2. In cases where cable emulation is already mathematically embedded in the Signal generators output patterns, amplitude settings have to follow SP2 amplitude values plus targeted cable degradation.

As a general rule, Signal amplitude at SP3 of the setup has to emulate SP2 amplitudes plus targeted the cable degradation. This is valid for MOST patterns as well as for Sine wave pattern used for testing AC conditions. Signal Generator and Cable/Cable emulation also shall provide an OFF-state as defined for the EBC in [3].

Note:

Conditions for BEC ON-state and OFF-state consist of AC conditions (F_{on} , F_{off}) and signal amplitude. which are specified in [3].

As described in section 3.4.1 the attenuation characteristic of Electrical Interconnect follows a function of frequency and results in Inter-Symbol Interference ISI. In consequence, shorter pulses of an incoming data signal may not achieve full amplitude swing anymore. Therefore, BEC response on data patterns with strong attenuation is dominated by the shorter pulses. In order to stress this effect, the MOST Stress Pattern contains sub-pattern structures that address such corner cases sufficiently. AC conditions are recommended to be tested with using pure sine wave signals.

As a general requirement,

- a BEC must be in ON state when AC-conditions F_{ON3} are met and signal amplitudes equal or larger than the V_{ON3_RMS}
- a BEC must be in OFF state when AC-conditions F_{OFF3} are met and signal amplitudes equal or lower than the V_{OFF3_RMS}

Note: Certain restriction with respect to STATUS signal may apply. In such case follow MNC supplier's instruction for testability. For details see [3], section 7.3.

6.3.2 Measuring BEC Parameters – Signal Charts

The signal chart represents the graphical view of test sequence. It shows the location of the action points and provides the pre-requisites for the corresponding tests of the BEC parameters.

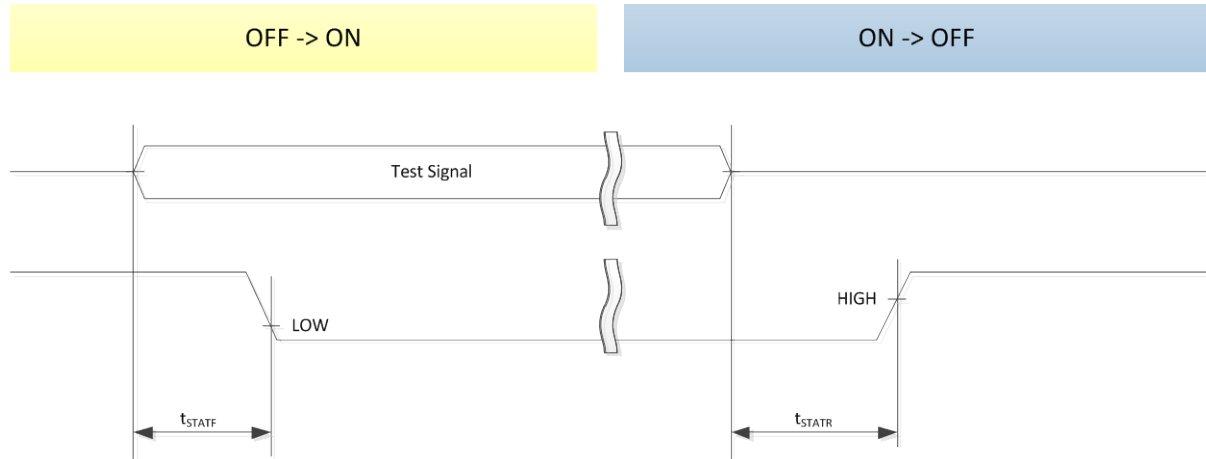


Figure 6-5: Measuring BEC Parameters: BEC Signal Chart

6.3.3 Measuring BEC Parameters – Test sequences

6.3.3.1 BEC Test Sequence #1 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
Test Signal: Inputs	SP3	Continuous Sine Wave within range of F_{OFF3}
Output / Expected behavior	<p>BEC shall stay in OFF state with STATUS = LVTTL High</p> <p>Note: With input stimulus present it is allowed that $I_{CCRX} > I_{CCSLEEP}(MAX)$</p>	

Table 6-3: BEC Test Sequence #1

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the wakeup mechanism of the BEC. It is required that the BEC must remain in OFF state being supplied with input signal with frequency within F_{OFF3} requirements (assuming all other ON state requirements are met).

The BEC must keep its STATUS signal LVTTL High at any time and before and after the Test Signal is applied consume no more than the sleep current, $I_{CCSLEEP}$. During the Test Signal application the BEC is allowed to consume more than $I_{CCSLEEP}$.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values shall be tested.

6.3.3.2 BEC Test Sequence #2 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
Test Signal: Inputs	SP3	Continuous Sine Wave > $F_{ON3_}(min)$ Signal Amplitude < V_{OFF3}
Output / Expected behavior	<p>BEC shall stay in OFF state with STATUS = LVTTL High</p> <p>Note: With input stimulus present it is allowed that $I_{CCR_} > I_{CCSLEEP}(MAX)$</p>	

Table 6-4: BEC Test Sequence #2

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the wakeup mechanism of the BEC. It is required that the BEC must remain in OFF state being supplied with input signal with amplitude of less than V_{OFF3} (assuming all other ON state requirements are met).

The BEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, $I_{CCSLEEP}$. During the Test Signal application the BEC is allowed to consume more than $I_{CCSLEEP}$.

6.3.3.3 BEC Test Sequence #3 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
Test Signal: Inputs	SP3	Burst, Sine Wave $> F_{ON3_}(min)$ Amplitude $> V_{ON3_RMS}$, with duration $\leq t_{STATF}(min)$
Output / Expected behavior	<p>BEC shall stay in OFF state with STATUS = LVTTL High</p> <p>Note: With input stimulus present it is allowed that $I_{CCRX} > I_{CCSLEEP}(MAX)$</p>	

Table 6-5: BEC Test Sequence #3

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the BEC. It is required that, when all ON state requirements are met, the BEC must still remain in OFF state for at least $t_{STATF}(min)$ time.

The BEC must keep its STATUS signal LVTTL High, the SP4 bus disabled at any time and before and after the Test Signal is applied consume no more than the sleep current, $I_{CCSLEEP}$. During the Test Signal application the BEC is allowed to consume more than $I_{CCSLEEP}$.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.4 BEC Test Sequence #4 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Equivalent SP2 OFF state
Initial State: Outputs	STATUS	LVTTL High
Test Signal: Inputs	SP3	Burst, Sine Wave > $F_{ON3_}(min)$ Amplitude > V_{ON3_RMS} , with duration > $t_{STATF}(min)$
Output / Expected behavior	BEC shall transition to ON state within time $t_{ON4}(max)$ with: STATUS = LVTTL Low within $t_{STATF}(min)$ to $t_{STATF}(max)$,	

Table 6-6: BEC Test Sequence #4

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the transition detection and wakeup mechanism of the BEC. It is required that, when all ON state requirements are met, the BEC must transition to ON state not earlier than $t_{STATF}(min)$ time, but also not later than $t_{ON4}(max)$.

Another requirements being checked are: STATUS signal timing: time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.5 BEC Test Sequence #5 - ON-to-OFF

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Sine Wave > $F_{ON3(min)}$ Amplitude > V_{ON3_RMS}
Initial State: Outputs	STATUS	LVTTL Low
Test Signal: Inputs	SP3	Signal Amplitude < V_{OFF3}
Output / Expected behavior	<p>BEC shall transition to OFF state with STATUS = LVTTL High within $t_{STATR(max)}$</p> <p>Afterwards (no specified time) current consumption shall be $I_{CCBEC} < I_{CCSLEEP(max)}$</p>	

Table 6-7: BEC Test Sequence #5

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the shutdown mechanism of the BEC. It is required that the BEC must transition to OFF state being supplied with input signal with amplitude of less than V_{OFF3} (assuming all other ON state requirements are met).

Another requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- BEC power supply: after transition to OFF state, the BEC power consumption should be less than $I_{CCSLEEP(max)}$.

Multiple testing with different initial state signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.6 BEC Test Sequence #6 - OFF-to-ON

Signal Chart	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	MOST Stress Pattern with nominal bit rate (BR) Signal Amplitude $< V_{OFF3}$
Initial State: Outputs	STATUS	LVTTL High
Test Signal: Inputs	SP3	Amplitude $> V_{ON3_RMS}$
Output / Expected behavior	BEC shall transition to ON state	
	STATUS = LVTTL Low within $t_{STATF(min)}$ to $t_{STATF(max)}$,	

Table 6-8: BEC Test Sequence #6

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the wakeup mechanism of the BEC. It is required that the BEC must remain in or transition to ON state, being supplied with input signal with amplitude of more than V_{ON3_RMS} and frequency within F_{ON3} requirements.

Other requirements being checked are:

- STATUS signal timing – time from Test Signal application to STATUS at LVTTL Low should be within t_{STATF} requirements.

Multiple testing with different test signal amplitudes is recommended. At least the minimal and maximal values must be tested.

6.3.3.7 BEC Test Sequence #7 - ON-to-OFF

Signal Charts	Figure 6-5	
Initial State: Inputs	V_{BEC}	According to operating conditions
	SP3	Stress Pattern with nominal bit rate (BR) Amplitude > V_{ON3_RMS}
Initial State: Outputs	STATUS	LVTTL Low
Test Signal: Inputs	SP3	Signal Amplitude < V_{OFF3}
Output / Expected behavior	<p>BEC shall transition to OFF state with STATUS = LVTTL High within $t_{STATR(max)}$</p> <p>Afterwards (no specified time) current consumption shall be $I_{CCBEC} < I_{CCSLEEP(max)}$</p>	

Table 6-9: BEC Test Sequence #7

The test is performed according to the setup given in 6.3.1.

This test sequence exercises the shutdown mechanism of the BEC. It is required that the BEC must transition to OFF state being supplied with signal with amplitude below V_{ON3_RMS} (assuming all other ON state requirements are met).

Other requirements being checked are:

- STATUS signal timing: time from Test Signal application to STATUS at LVTTL High should be within t_{STATR} requirements.
- BEC power supply: after transition to OFF state, the BEC power consumption should be less than $I_{CCSLEEP(max)}$.

Multiple testing with different initial state signal amplitudes is recommended. At least the minimal and maximal values must be tested.

7 Detecting Bit rate (Frequency Reference)

The bit rate is detected as follows:

Data-pulses range from 2 UI to 6 UI yielding 5 different pulse widths (2, 3, 4, 5, 6 UI). A clock at UI-rate represents a cycle time of 1 UI, which is twice the bit rate (i.e., for F_s 48 kHz, the bit rate is 49.152 Mbit/s, the UI-clock is 98.304 MHz).

A method of extracting the UI-clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI-clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. Then the bit rate is $\frac{1}{2}$ of the UI-rate.

The bit rate can be measured with MOST50 test stress pattern or any other valid data pattern. Setup of the oscilloscope shall follow the general requirements using acquisition length of at least 10 MSamples and a sampling rate of 5 GSamples/s.

8 System Performance

The system-level specifications apply to an entire MOST network.

8.1 SP3 Receiver Tolerance

Unlike the link-level tests which use a pattern generator as the signal source, the system-level tests use live data from a fully formed MOST50 ring. Using the same eye diagram methodologies developed in section 3.7 a measurement is taken at SP3 of the Timing Master node. By taking the measurement in this way, one can quantify the total jitter accumulation around the ring. This measurement is applicable for every node in the network at SP3.

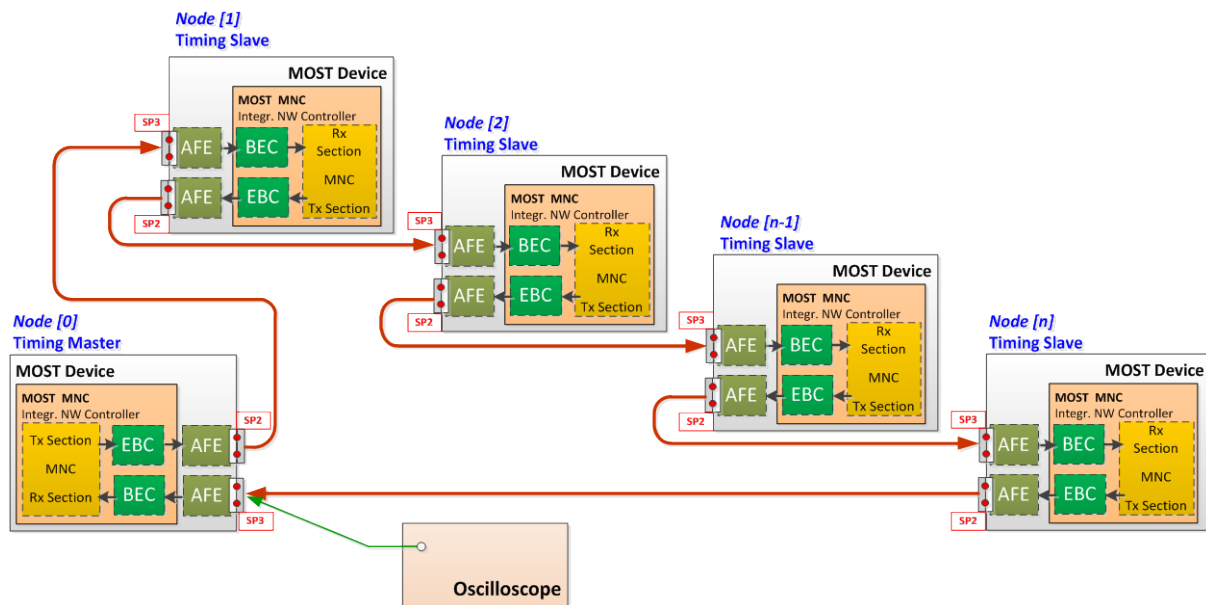


Figure 8-1: SP3 Receiver Tolerance Setup

8.2 Master Delay Tolerance

Master Delay Tolerance is a measure of end-to-end delay and phase variation between SP2 and SP3 of the Timing Master device. To ensure proper network operation, the total network delay must not exceed the specified maximum.

Following the setup diagram shown in Figure 8-2, the total delay can be measured on an oscilloscope.

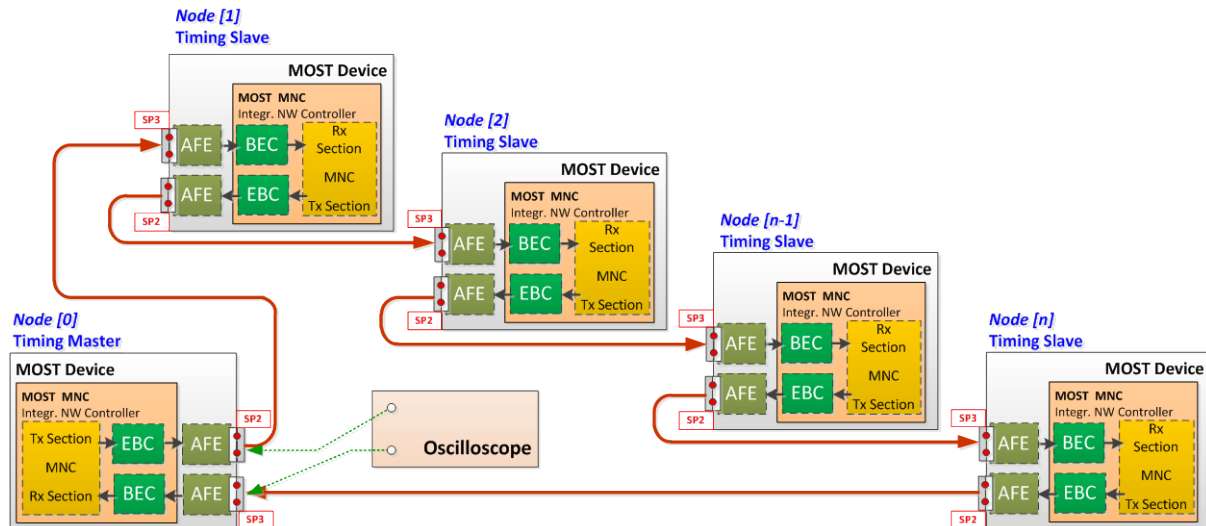

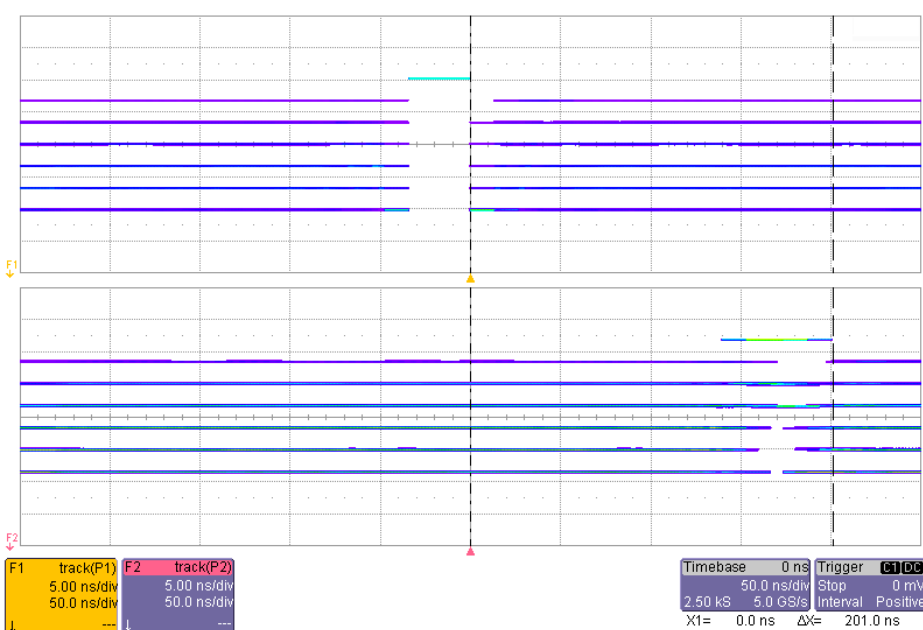


Figure 8-2: Master Delay Tolerance Setup

The following table describes the procedure used to measure the total delay. The oscilloscope used must be able to trigger on a specified period and have software functions for tracking periods. Two differential probes are required.

Step	Action
Acquiring a waveform	<p>For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP2 of the TimingMaster node. A second differential probe is connected to SP3 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels.</p> <p>The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP2. The interval should be set to $10 \text{ UI} \pm 0.5 \text{ UI}$. The <i>Trigger Mode</i> should be Normal.</p> <p>A sequence of the data stream ("waveform") is sampled into the scope's memory.</p>
Measure period	<p>The MOST50 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay between any two points in the network.</p> <p>Configure the oscilloscope to measure the period of both SP2 and SP3.</p>
Track the period	<p>Configure the oscilloscope to display a "Track" waveform for both SP2 and SP3 period measurements. This should result in two waveforms with time on the y-axis where the line indicates the length of the current period.</p>

Step	Action
	
Measure the delay	<p>Configure the oscilloscope display to show only the SP2 and SP3 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP2 and SP3.</p> <p>Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP3 10 UI period. This is the Master Delay.</p> 

9 Appendix A: Test Fixture

Test Fixtures for interfacing Measurement equipment with a Unit under Test

Test Fixtures are required when connecting differential signal terminals of components or modules under test to the respective Measurement Equipment.

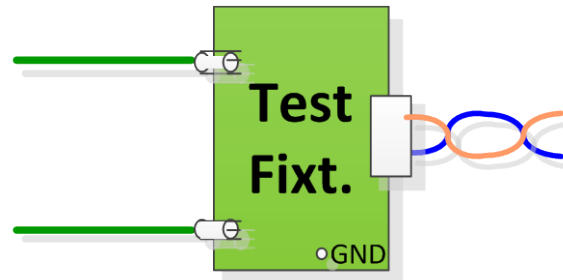


Figure 9-1: Test Fixture

Examples are:

- Signal Quality evaluation with an oscilloscope using two single ended channels and oscilloscope's internal 50 Ω termination
- Measurement of Attenuation using a VNA
- Measurement of Return Loss using a VNA

Modules under Test (e.g. ECU-SP2, electrical interconnect) are providing an interface with differential signal structure and a pair of customer defined contact geometries. Measurement equipment is being attached using single ended interfaces with SMA-connectors (or similar RF laboratory connectors).

As the MOST bPHY does not specify at particular connector system a unique test fixture can't be defined. However, recommendations and applications hints shall be given:

- The fixture shall have a low insertion loss
- It shall be highly symmetrical between the two wires of the pair
- It shall be very well adapted to the single-ended impedance of the measuring instrument (50 Ω).

Two versions of the fixture are needed for:

- Fixture with connector jacks to interface with an ECU. Here, the jacks must be extended to allow making contact with the ECU side pin header.

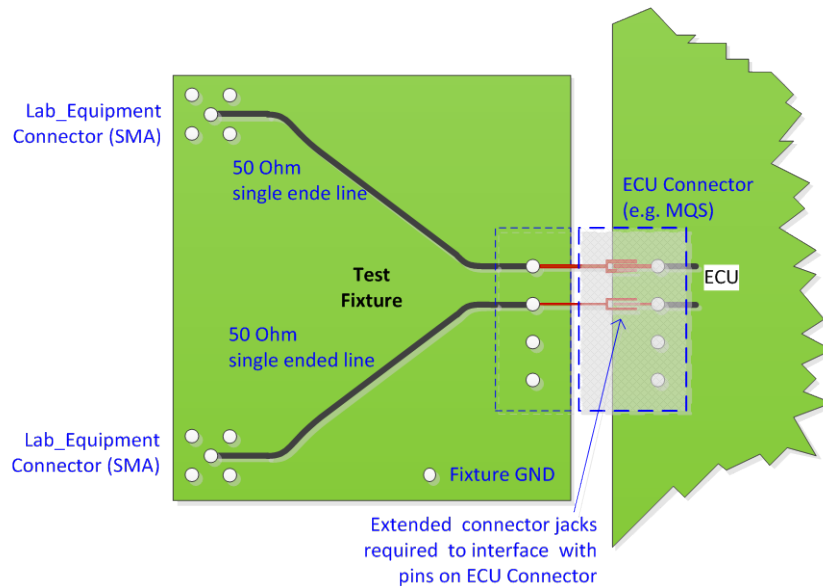


Figure 9-2: Test Fixture for connecting ECU

- Fixture with male contacts to interface with harness side female connectors. The pins at the fixture must be extended to allow making contact with a female header.

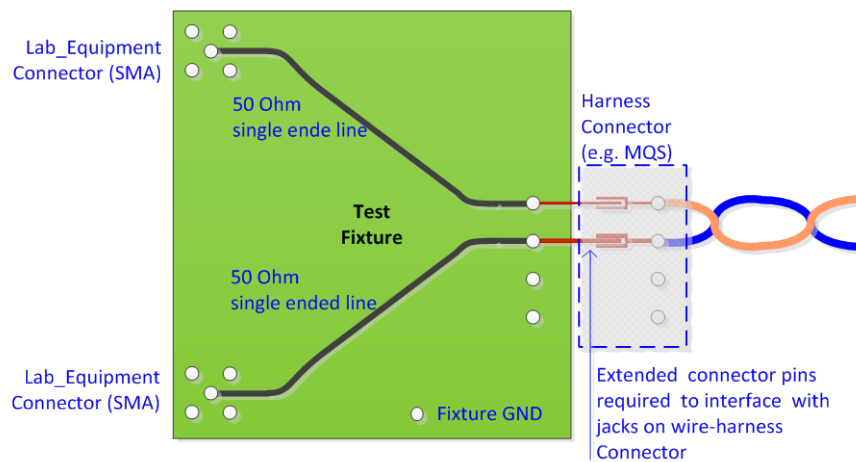


Figure 9-3: Test Fixture for connecting wire harness

10 Appendix B: Overview on Test Modes

This table lists test modes required to measure parameters as specified in [3]

Test Mode	Test Case	Condition
MOST50 Stress Test Pattern	SP2 Link Quality, <ul style="list-style-type: none"> Signal Amplitude RMS, V_{rms2} Alignment Jitter, acc. to Eye Mask A₂... D₂ Transferred Jitter, J_{tr2} 	Data signal at SP2 provides data content as specified for MOST50 Stress Test Pattern
MOST50 PSD Test Pattern	SP2 Link Quality, <ul style="list-style-type: none"> PSD, acc. to PSD Mask U1 ... U7, L1 ... L4 	Data signal at SP2 provides data content as specified for MOST50 PSD Test Pattern
SP2 Silent mode	Return Loss at SP2, RL_SP2 DC-offset compensation for SP2 Link Quality	Test mode must ensure: <ul style="list-style-type: none"> EBC Impedance with AFE impairment detectable EBC does not emit data transitions
SP3 Silent mode	Return Loss at SP3, RL_SP3	Test mode must ensure: <ul style="list-style-type: none"> BEC Impedance with AFE impairment detectable No valid data signal present, while stimuli from TDR or VNA may occur

Table 10-1: Overview test modes

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