

# MOST

Media Oriented Systems Transport

Multimedia and Control  
Networking Technology

**MOST150 cPHY Automotive Physical Layer  
Sub-Specification Rev. 1.1**

**Errata 2**

**Rev. 1.1E2**

**05/2016**

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For more information on the MOST technology, please contact:

**MOST Cooperation**  
Administration  
Emmy-Noether-Str. 14  
D-76131 Karlsruhe  
Germany

Tel: (+49) (0) 721 966 50 00

E-mail: [contact@mostcooperation.com](mailto:contact@mostcooperation.com)  
Web: [www.mostcooperation.com](http://www.mostcooperation.com)



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## Contents

1	INTRODUCTION .....	6
2	ERRATA .....	6

## Bibliography

Number	Document	Revision
[1]	MOST150 cPhy Automotive Sub-Specification [MOST150 cPhy]	Rev. 1.1
[2]	MOST Specification	Rev. 3.0
[3]	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits (TIA/EIA-644-A-2001)	

Table 1-1 Bibliography

## Document History

### Changes 1V1E2

Change Ref.	Section	Changes
1V1E2-00	2	Added 3.) - modify section 7.3.3: Delay to STATUS rising $t_{STATR}$

### Changes 1V1E1

Change Ref.	Section	Changes
1V1E1-00	2	First Issue
1V1E1-01	2	Modify section 9.12 LVDS
1V1E1-02	2	Modify section 7.3.3 CEC Requirements d), e)

## 1 Introduction

This document is a supplement to the MOST150 cPhy Automotive Sub-Specification Rev. 1.1 [1].

## 2 Errata

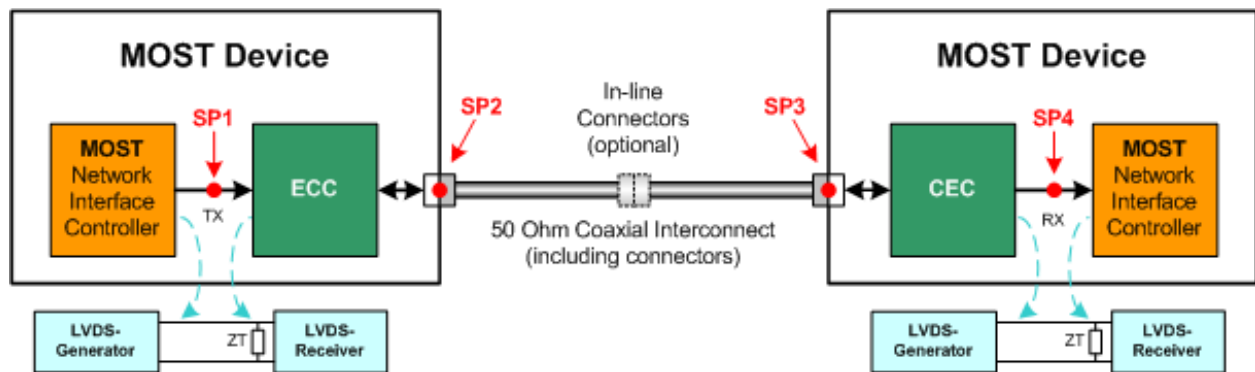
Legend: → means “will be substituted by”

### 1.)

*Specification of a further exception for the requested compliance to the referenced LVDS-standard in section 9.1.*

#### **Reason for Errata**

*MOST application with standalone Transceiver incorporates 2 LVDS links. This is at the SP1-Interface, connecting NIC with ECC and at the SP4-Interface, connecting CEC with the NIC.*



*LVDS System enables far more challenging channel configurations as being used in MOST applications. The Specification changes transfer performance margin from LVDS-Link to the transceivers to enable lean and robust transceiver designs for harsh automotive environment.*

## 9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. Exceptions are listed in Table 2-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for wiring harness. All electrical signals must maintain the correct polarity from CEC to NIC and from NIC to ECC.

Exception regarding LVDS [3]	Symbol	Condition	Min.	Max.	Unit
Common-mode Input Voltage range	$V_{CM}$		0.05	$V_{cctx} - 1.2V$	V
Steady-state Input Amplitude	$V_{ISS}$	1), 2)	0.30		V
Combined impedance of receiver loads connected to the bus	$R_{CRL}$	3), 4)		30	kOhm
Transition Times	$t_r ; t_f$	5)	200		ps
Notes: 1) Refers to chapter 4.2.4 “Receiver input sensitivity measurements” in [3]. 2) Difference between high-state and low-state of bimodal waveform. 3) The 30kOhm resistors represent the combined impedance of 4 receiver loads connected to the bus. 4) Refers to chapter 4.1.1 “Full Load Measurements” in [3]. 5) $t_r$ : 20% -80% , $t_f$ : 80% -20%.					

Table 2-1: Exception regarding LVDS [3]



## 9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. Exceptions are listed in Table 2-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for wiring harness. All electrical signals must maintain the correct polarity from CEC to NIC and from NIC to ECC.

Exception regarding LVDS [3]	Symbol	Condition	Min.	Max.	Unit
Common-mode Input Voltage range	$V_{CM}$		0.05	$V_{cctx} - 1.2V$	V
Steady-state Input Amplitude	$V_{ISS}$	1), 2), 8)	0.30		V
Combined impedance of receiver loads connected to the bus	$R_{CRL}$	3), 4)		30	kOhm
Transition Times	$t_r ; t_f$	5)	200		ps
Minimum Generator Output Amplitude	$ V_T $	6), 7)	0.185		V
Notes: 1) Refers to chapter 4.2.4 “Receiver input sensitivity measurements” in [3]. 2) Difference between high-state and low-state of bimodal waveform. 3) The 30kOhm resistors represent the combined impedance of 4 receiver loads connected to the bus. 4) Refers to chapter 4.1.1 “Full Load Measurements” in [3]. 5) $t_r$ : 20% -80% , $t_f$ : 80% -20%. 6) With lower $ V_T $ , ringing is limited to not exceed absolute limits given in [3] 7) Exception valid, for CEC RX-outputs only 8) Exception valid, for ECC TX-inputs only					

Table 2-1: Exception regarding LVDS [3]

**2.)** Correction of 7.3.3 CEC Requirements d) and e)

**7.3.3 CEC Requirements**

...

d) A CEC must transition from the *Off-State* to the *On-State* upon detecting valid wakeup conditions, defined as a signal with valid SP3 amplitude (see Section 6.3.2.1) and a frequency within  $F_{ON3}$  as specified in Table 7-3. The wakeup procedure has the following requirements:

- The CEC must transition the **STATUS** signal low within time  $t_{STATF}$  after valid wakeup conditions have been detected at SP3.
- The CEC must enable the SP4 LVDS bus and produce a valid LVDS signal within time  $t_{LVDSV4}$  from when **STATUS** was set low.
- The CEC must enter the *On-State* within time  $t_{ON4}$  from when the valid wakeup MOST data was detected.

e) A CEC in the *On-State* must constantly monitor the input signal frequency and must transition to the *Off-State* upon detecting valid shutdown conditions. When the signal at SP3 has a frequency within  $F_{OFF3}$  as specified, the CEC must be in *Off-State*. The transition procedure to the *Off-State* has the following requirements:

- The CEC must force the signal at SP4 to LVDS 0 and set **STATUS** high within a time  $t_{STATR}$  upon detecting valid shutdown conditions on SP3. The CEC must maintain a valid LVDS signal during the detection phase.
- The CEC must maintain its LVDS output at a logical 0 for a hold time of  $t_{LVDSH4}$  after **STATUS** transitions high.
- The CEC must enter the *Off-State* within time  $t_{OFF4}$  from when the valid shutdown conditions occurred.



**7.3.3 CEC Requirements**

...

d) A CEC must transition from the *Off-State* to the *On-State* upon detecting valid wakeup conditions, defined as a signal with valid SP3 amplitude (see Section 6.2 and 6.3.1) and a frequency within  $F_{ON3}$  as specified in Table 7-3. The wakeup procedure has the following requirements:

- The CEC must transition the **STATUS** signal low within time  $t_{STATF}$  after valid wakeup conditions have been detected at SP3.
- The CEC must enable the SP4 LVDS bus and produce a valid LVDS signal within time  $t_{LVDSV4}$  from when **STATUS** was set low.
- The CEC must enter the *On-State* within time  $t_{ON4}$  from when the valid wakeup MOST data was detected.

e) A CEC in the *On-State* must constantly monitor the input signal frequency and input amplitude. A CEC must transition to the *Off-State* upon detecting valid shutdown conditions. When the signal at SP3 has a frequency within  $F_{OFF3}$  as specified in Table 7-3 or a too low SP3 amplitude (see Section 6.2 and 6.3.1) the CEC must transition to *Off-State*. The transition procedure to the *Off-State* has the following requirements:

- The CEC must force the signal at SP4 to LVDS 0 and set **STATUS** high within a time  $t_{STATR}$  upon detecting valid shutdown conditions on SP3. The CEC must maintain a valid LVDS signal during the detection phase.
- The CEC must maintain its LVDS output at a logical 0 for a hold time of  $t_{LVDSH4}$  after **STATUS** transitions high.
- The CEC must enter the *Off-State* within time  $t_{OFF4}$  from when the valid shutdown conditions occurred.



### 3.)

Specification of an exception for  $t_{STATR}$  timing in case of using integrated Coaxial Transceivers (Details on integrated Coaxial Transceivers see reference in section 4.2.2.)

#### Reason for Errata

CEC Power State requirements in Table 7-3 define the response of a CEC on activity or on loss of activity at its input. This definition includes the requested behavior on the CEC's data output (SP4) and the STATUS line, to ensure interoperability of a CEC with its application environment. The STATUS signal is externally used to start Power Supply (falling edge,  $t_{STATF}$ ), Shut Down process however is fully under software control. For integrated Transceivers, the SP4 interface is not accessible and therefore interoperability with the NIC-part is in full responsibility of the supplier. The timely response on inactivity is processed fully internally, rising edge of STATUS being processed to outside (rising edge,  $t_{STATR}$ ) is for information only. Therefore, a less stringent timing for  $t_{STATR}$  can be tolerated.

CEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Powering On</b>						
Frequency range of input at SP3 for On-State operation	F <sub>ON3</sub>	1)	12	-	73.743	MHz
CEC power-on delay	t <sub>ON4</sub>	2)	-	-	9.7	ms
Delay to <b>STATUS</b> falling	t <sub>STATF</sub>	3)	200	-	700	μs
<b>STATUS</b> falling to LVDS valid	t <sub>LVDSV4</sub>		-	-	100	μs
CEC Operating Voltage Range	V <sub>CECOR</sub>		3.135	3.300	3.465	V
<b>Powering Off</b>						
Frequency range of input at SP3 for Off-State operation	F <sub>OFF3</sub>		0	-	10	kHz
CEC power-off delay	t <sub>OFF4</sub>	4)	-	-	1	ms
CEC LVDS hold time	t <sub>LVDSH4</sub>		1	-	-	μs
Delay to <b>STATUS</b> rising	t <sub>STATR</sub>	5)	-	-	2	μs
Current consumption in the Off-State	I <sub>CCSLEEP</sub>		-	-	30	μA
Notes: 1) The CEC can still be in the On-State above this frequency. 2) t <sub>ON4</sub> is the sum of t <sub>STATF</sub> , t <sub>LVDSV4</sub> and an additional time required for SP4 to be valid MOST traffic. 3) Time from valid wakeup condition to status low, see Section 7.3.3 d). 4) t <sub>OFF4</sub> is the sum of t <sub>STATR</sub> and t <sub>LVDSH4</sub> . 5) Time from signal off to status high, see Section 7.3.3 e).						

Table 2-1: CEC Power State Requirements



CEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Powering On</b>						
Frequency range of input at SP3 for On-State operation	F <sub>ON3</sub>	1)	12	-	73.743	MHz
CEC power-on delay	t <sub>ON4</sub>	2)	-	-	9.7	ms
Delay to <b>STATUS</b> falling	t <sub>STATF</sub>	3)	200	-	700	μs
<b>STATUS</b> falling to LVDS valid	t <sub>LVDSV4</sub>		-	-	100	μs
CEC Operating Voltage Range	V <sub>CECOR</sub>		3.135	3.300	3.465	V
<b>Powering Off</b>						
Frequency range of input at SP3 for Off-State operation	F <sub>OFF3</sub>		0	-	10	kHz
CEC power-off delay	t <sub>OFF4</sub>	4)	-	-	1	ms

CEC LVDS hold time	tLVDSH4		1	-	-	μs
Delay to <b>STATUS</b> rising	tSTATR	5), 6)	-	-	2	μs
		5), 7)	-	-	7	μs
Current consumption in the <i>Off-State</i>	ICCSLEEP		-	-	30	μA
Notes: 1) The CEC can still be in the On-State above this frequency. 2) t <sub>ON4</sub> is the sum of t <sub>STATF</sub> , t <sub>LVDSV4</sub> and an additional time required for SP4 to be valid MOST traffic. 3) Time from valid wakeup condition to status low, see Section 7.3.3 d). 4) t <sub>OFF4</sub> is the sum of t <sub>STATR</sub> and t <sub>LVDSH4</sub> . 5) Time from signal off to status high, see Section 7.3.3 e). 6) for stand-alone Transceivers 7) for integrated Transceivers						
Table 2-2: CEC Power State Requirements						

Notes: