

MOST[®]

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

MOST Physical Layer Basic Specification

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MOSTCO CONFIDENTIAL

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SUPPORT AND FURTHER INFORMATION

For more information on the MOST technology, please contact:

MOST Cooperation
Administration
P. O. Box 4327
D-76028 Karlsruhe
Germany
Phone: (+49) (0) 721 966 50 00
Fax: (+49) (0) 721 966 50 01
E-mail: contact@mostcooperation.com
Web: www.mostcooperation.com



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1 Introduction

The MOST® network physical layer supports the transmission of the bit stream between MOST Devices. This document describes and defines the “*MOST Physical Layer Specification*”.

The MOST network supports various transportation media as well as multiple speed grades. Some examples of possible physical layers include POF, PCS, UTP, and STP while some examples of speed grades include MOST50 and MOST150. All MOST networks operate as synchronous rings regardless of physical layer media or speed grade. Therefore, all MOST networks require the same basic types of timing measurements. These actual timing requirements are specific for the combination of physical layer and speed grade, however the measurement methods can be generalized into a strategy used to specify any MOST network and guarantee operation. This document is a master specification that outlines the basic measurement techniques and parameters. While the values of the measurements, methods, and actual parameter values are contained in sub-specifications that are physical layer and speed grade dependant. Each sub-specification adapts the basic system requirements into constraints that govern and define interfaces and parameters, which are the base for development of real products. The specification hierarchy is outlined in Figure 1-1.

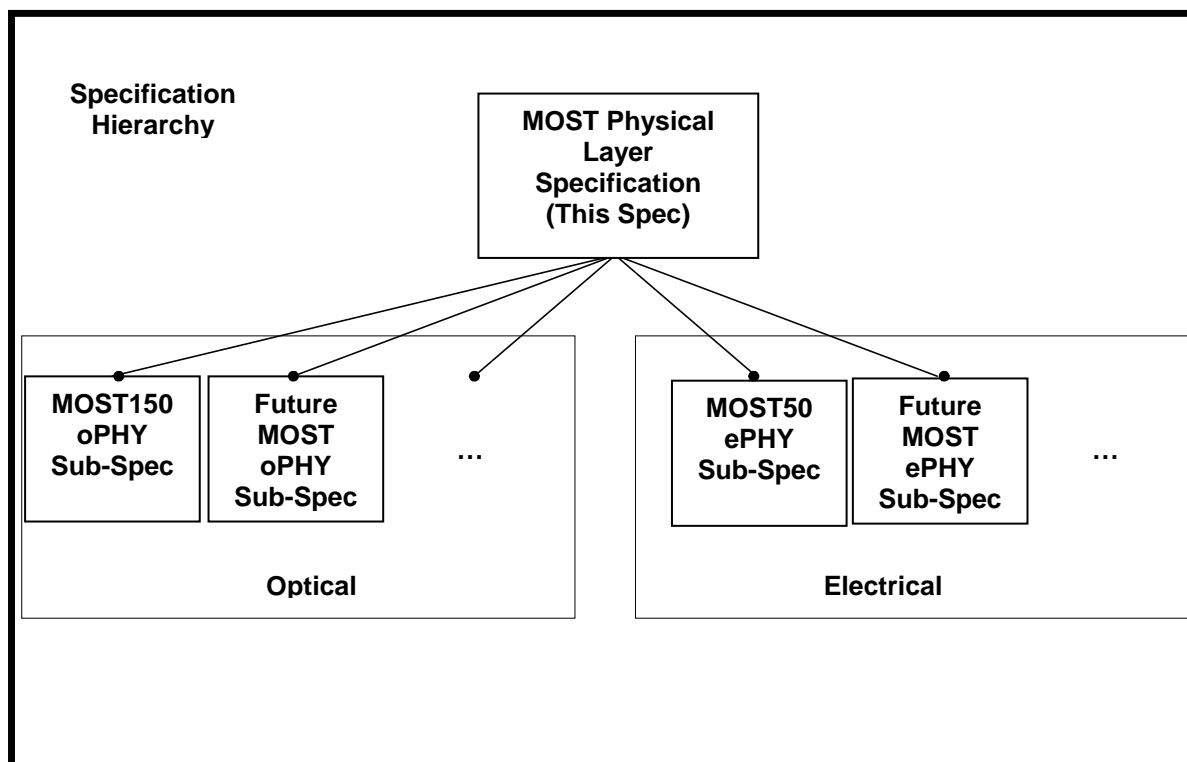


Figure 1-1 Specification Hierarchy

The physical connection of two MOST devices is called a link. The “*MOST Physical Layer Specification*” describes measurements taken at specific locations along a MOST link. These locations are called specification points. The location of the specification points is shown in Figure 1-2.

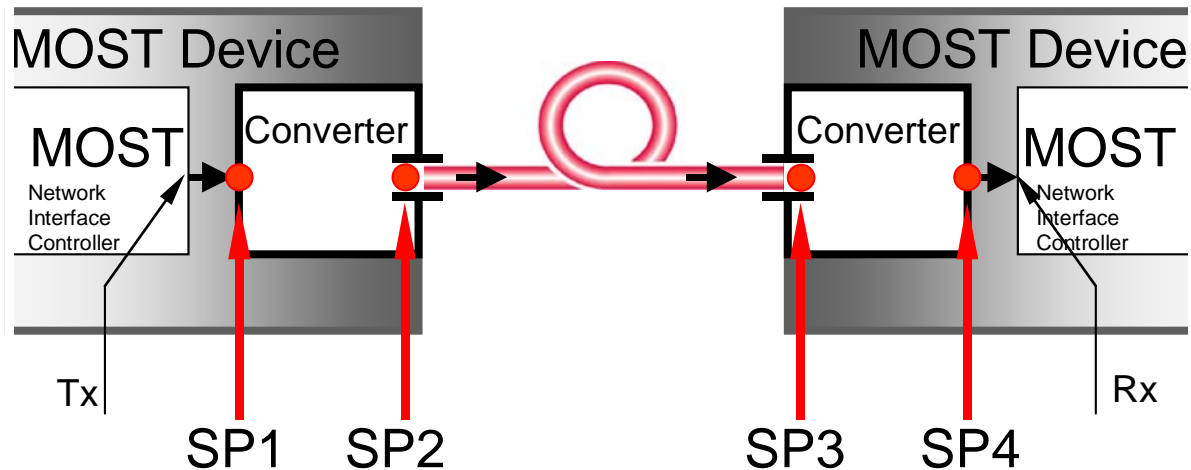


Figure 1-2: Location of specification points along a MOST link.

Specification point No.1 and specification point No.4 define the electrical signal requirements between a MOST NIC (with its input Rx and output Tx) and a converter. Specification point No.1 and No.2 define the transmit converter while No.3 and No.4 define the receive converter. Specification point No.2 and specification point No.3 define the properties of the interface between a MOST Device and a wiring harness (e.g. signal timing, signal amplitude, connector interface drawings).

Beside the link there are also definitions covering the system stability of the whole network. This system view describes mechanisms such as jitter transfer through MOST Devices and jitter accumulation around the network.

All parameters and definitions required for individual specification points and system requirements are summarized in the sub-specifications. Systems must meet all sub-specification requirements in order to guarantee proper operation.

The given parameters within the sub-specifications are minimum values to ensure functionality of the network in a wide range of environment conditions. Real hardware may have better performance than requested by the specifications to provide operating margin for the system.

Different physical layers or integration of components may require that certain specification points be omitted or shifted to a different location in the link. Sub-specifications will control the number and placement of specification points.

1.1 Terminology and Abbreviations

Accumulated Phase-Variation: the portion of phase-variation at any point in a network that is made up entirely of the transferred jitter and transferred wander from all previous nodes

Accumulated Jitter: the portion of jitter at any point in a network that is made up entirely of the transferred jitter from all previous nodes

Alignment Jitter: any jitter that degrades the receiver eye with horizontal closure

Average Pulse Width Distortion (APWD): the average deviation of the signal pulses from their ideal width

BER: Bit error rate

Bit Rate (BR): the number of bits including overhead transmitted through any point on the system per second, hence $BR = BPF * Fs$

Bits Per Frame (BPF): The number of bits including overhead contained in a MOST frame

$BPF_{MOST50} = 1024$

$BPF_{MOST150} = 3072$

Components: parts that are used to build up a module

Data-Dependant Jitter (DDJ): any jitter generated by changes in the transmitted data pattern

Device: an ECU that contains optical or electrical MOST modules

ECU: Electronic Control Unit

Electrical to Optical Converter (EOC): a component that converts an electrical signal into an optical signal

Electromagnetic Compliance (EMC): device, module, or component conformance testing to rules or templates governing EMI generation and tolerance

Electromagnetic Interference (EMI): radiation which is emitted by electrical circuits carrying rapidly changing signals, as a by-product of their normal operation

ePHY: MOST electrical physical layer

Fall Time: the time required for a signal to transition from 90% to 10% of the amplitude

Filter and Transformer, Device output section (FTO): an analog filtering and isolation circuit that converts the raw ePHY stream into a signal suitable for transmission across the link.

Filter and Transformer, Device input section (FTI): an analog filtering and isolation circuit that conditions the ePHY link signal for the receiver.

Generated Jitter: any jitter at the output of a module or device that is not transferred from its input

Generated Wander: any wander at the output of a module or device that is not transferred from its input

Golden PLL: a hardware or software device that is used to recover the clock required to form an eye diagram

Jitter: phase variation with spectral content above 10Hz

Master Delay Tolerance (T_{MDT}): the maximum amount of delay that the master device can accept without failure

Module: an assembly of components that is bounded between two specification points

Network Interface Controller (NIC): a MOST transceiver that can route traffic and manage basic network resources

Network Frame Rate (F_s): the frequency at which new frames are generated by the master device

Numerical Aperture (NA): the sine of the critical angle of an optical fiber

oPHY: MOST optical physical layer

Optical to Electrical Converter (OEC): a component that converts an optical signal into an electrical signal

Phase-variation: any time deviation between the edges of a real signal and the edges of a reference signal

PLL Bandwidth: The frequency at which the PLL attenuates transferred jitter by more than 3dB.

Probability Density Function (PDF): a function representing the relative distribution of the frequency of a continuous random variable

Reference Signal: an ideal signal formed according to the reference timebase

Reference Timebase: the network frame rate as defined by the crystal oscillator of the master device

Rise Time: the time required for a signal to transition from 10% to 90% of the amplitude

Serial Data Analyzer: (SDA): an instrument used to perform industry standard jitter and amplitude measurements and operations on a serial data stream

Specification Point (SP_n): a measurement point at a standardized location in a link where results can be compared

System: a MOST Network consisting of several Devices

Transferred Jitter: any jitter that passes through a jitter filter

Transferred Wander: any wander that passes through a jitter filter

Uncorrelated Jitter (UJ): any jitter that is not correlated to any other jitter source in the system

Unit Interval: the longest interval of which the intervals of all pulses of a reference signal are whole multiples

Wander: any phase-variation with spectral content of 10Hz or below

2 Physical Layer Parameters

2.1 Phase-Variation

Phase-variation describes data-stream timing noise and distortion. Sub-categories based on the spectral content are described below.

2.1.1 Wander

Wander is made up of any phase-variation from DC to 10Hz. All active components in the system will create wander. Wander can have many sources, but is usually a function of the global system temperature drift, and will usually correlate very well from node to node. Typically, wander does not affect alignment jitter eye masks and is usually only a concern for the timing-master device. The golden PLL bandwidth and maximum node count are set at the sub-spec level, and therefore wander specs shall be considered at the sub-spec level as well.

2.1.2 Jitter

Jitter is any phase-variation of frequency greater than 10Hz. Just about every component in the system will create some amount of jitter. As opposed to wander, which almost always correlates from node to node, jitter can either be correlated or uncorrelated. The dominant jitter sources in the system usually consist of PLL noise, link-induced DDJ, sensitivity-induced OEC noise, crosstalk, or system level phenomena such as power supply coupling. Data scrambling is used to eliminate DDJ correlation between nodes.

Jitter can be split up in two categories, depending on their impact on link or system (also shown in Figure 2-1):

Alignment jitter:	effects data recovery in a NIC and influences Eye-Diagram measurement.
Transferred jitter:	effects accumulation of system jitter and therefore timing-master jitter tolerance (no influence on the Eye-Diagram measurement).

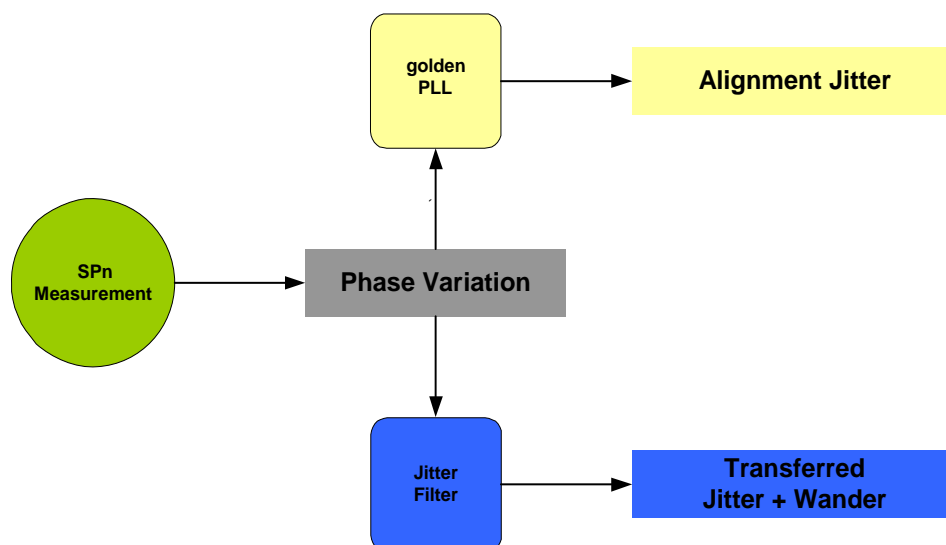


Figure 2-1: Phase Variation Measurements

2.1.3 Clock Recovery and Reference Clock

Phase Variation can be measured directly on a data stream, however to view alignment jitter and transferred jitter independently, special tools are required.

2.1.3.1 Background Information

All MOST networks contain one timing-master which creates the system reference clock. This clock is embedded within the data stream. All other devices are timing-slaves that recover the clock from the data stream. Therefore clock recovery is a basic functionality of a NIC. As the data stream travels through the system, modules and components add phase variation that degrades this clock.

Receiver jitter tolerance and jitter transfer are basic operation properties of any NIC device. The jitter that affects the reception of data is called alignment jitter and is measured by eye diagram formed with a golden PLL. Transferred jitter is measured with a jitter filter.

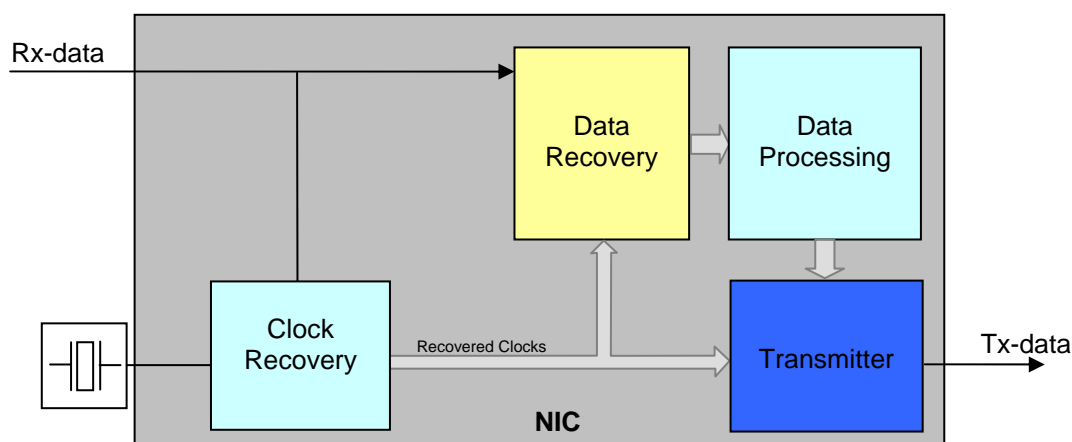


Figure 2-2 Clock recovery example

Figure 2-2 illustrates that input jitter may affect the transmitter and receiver differently. Therefore there is a need for a Golden PLL model and a Jitter Filter model. Together they reflect the required jitter behavior of a NIC.

2.1.3.2 Golden PLL

The golden PLL is a model which describes the behavior of the NIC when jitter is applied to its input. A golden PLL can be constructed out of hardware or software, but must always directly take data in from the measured specification point and output a clock at the UI frequency for eye diagram formation.

The golden PLL must be defined in the sub-specification, and the model shall be linear and shall consist of either a graph, table, or transfer function.

2.1.3.3 Jitter Filter

The jitter filter is a model which describes the worst case NIC jitter transfer function. A jitter filter can be constructed out of hardware or software, but must always directly take data in from the measured specification point and output the RMS value of the transferred jitter at the specification point.

The jitter filter must be defined in the sub-specification, and the model shall be linear and consist of either a graph, table, or transfer function.

2.1.4 Eye-Diagram

The eye diagram is a tool for measuring the predicted performance of a receiver on a serial data stream. As the jitter on the measured signal increases, the eye will close more and more. A keep-out mask is defined to detect possible error traces. If the eye doesn't hit the mask then data recovery is ensured. Mask design depends on the required receiver margin and the nature of the channel. The actual mask shapes, limits, and required hits are defined at the sub-specification level. Different eye-diagrams and their associated masks are shown in Figure 2-3 and Figure 2-4.

Eye Diagram Requirements:

- 1) The eye mask should be kept as simple as possible, and should be constructed of some type of polygon, as curves and other strange shapes are not practical.
- 2) The mask shape should be able to be implemented on state of the art scopes and serial data analyzers (SDA).
- 3) The mask must be designed considering the target bit error rate.

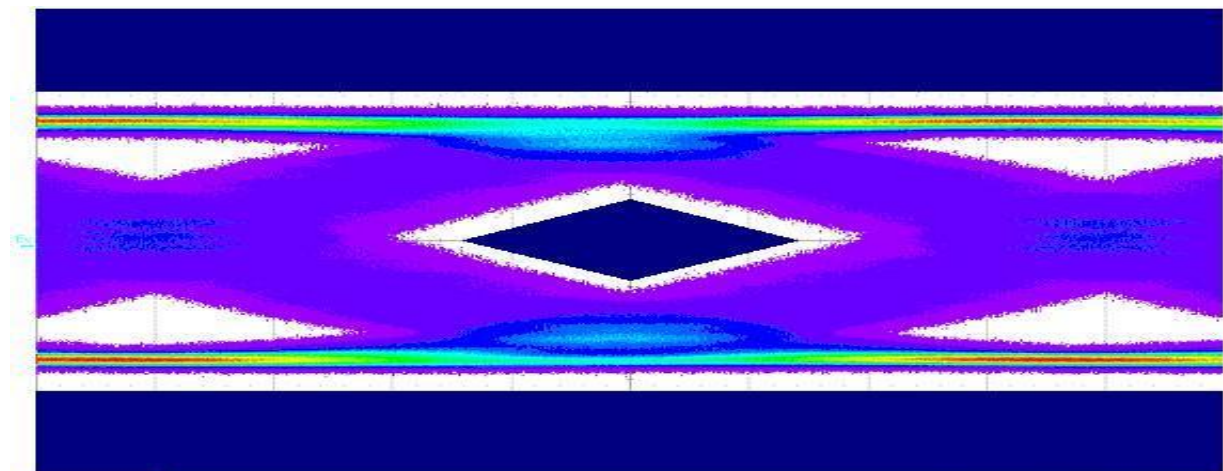


Figure 2-3: First example of a PHY signal eye mask

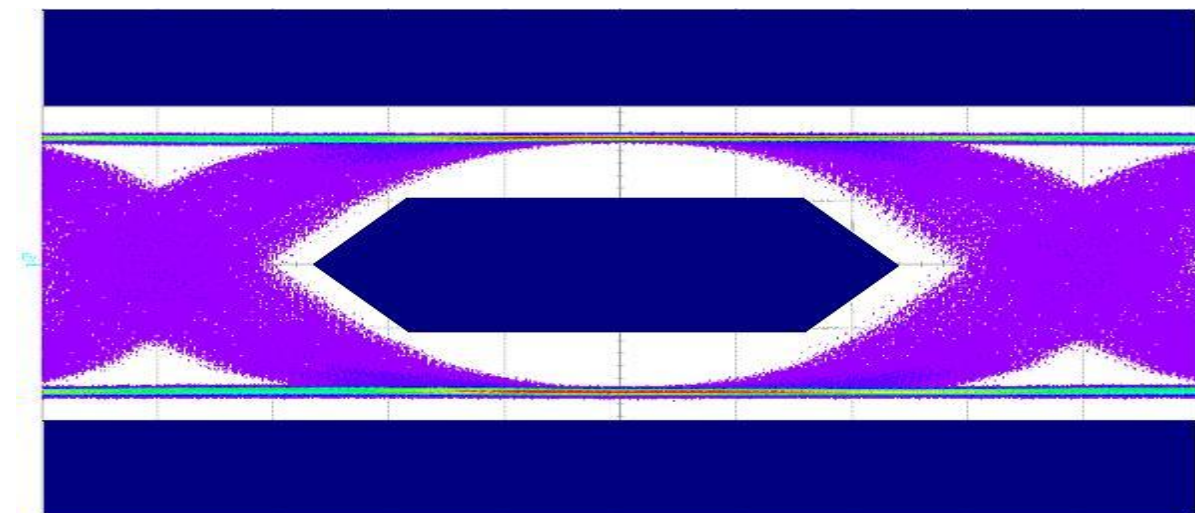


Figure 2-4 Second example of a PHY signal eye mask

2.1.4.1 Receiver Eye Degradation and Eye Diagram

Alignment Jitter, APWD, poor rise and fall times, and excessive signal ringing limit the ability of the receiver to recover the data from the incoming data stream. The eye diagram shows these effects as horizontal or timing and vertical or amplitude eye closure. As the eye diagram is moved down the link or down the system, the horizontal closure will grow and encroach on the link or system margin. All eye diagrams are one unit interval wide. The golden PLL sampling edge is lined up with the center of the eye, and mask boundaries are given in terms of the UI as percentages. An example eye diagram and sampling point are shown in Figure 2-5.

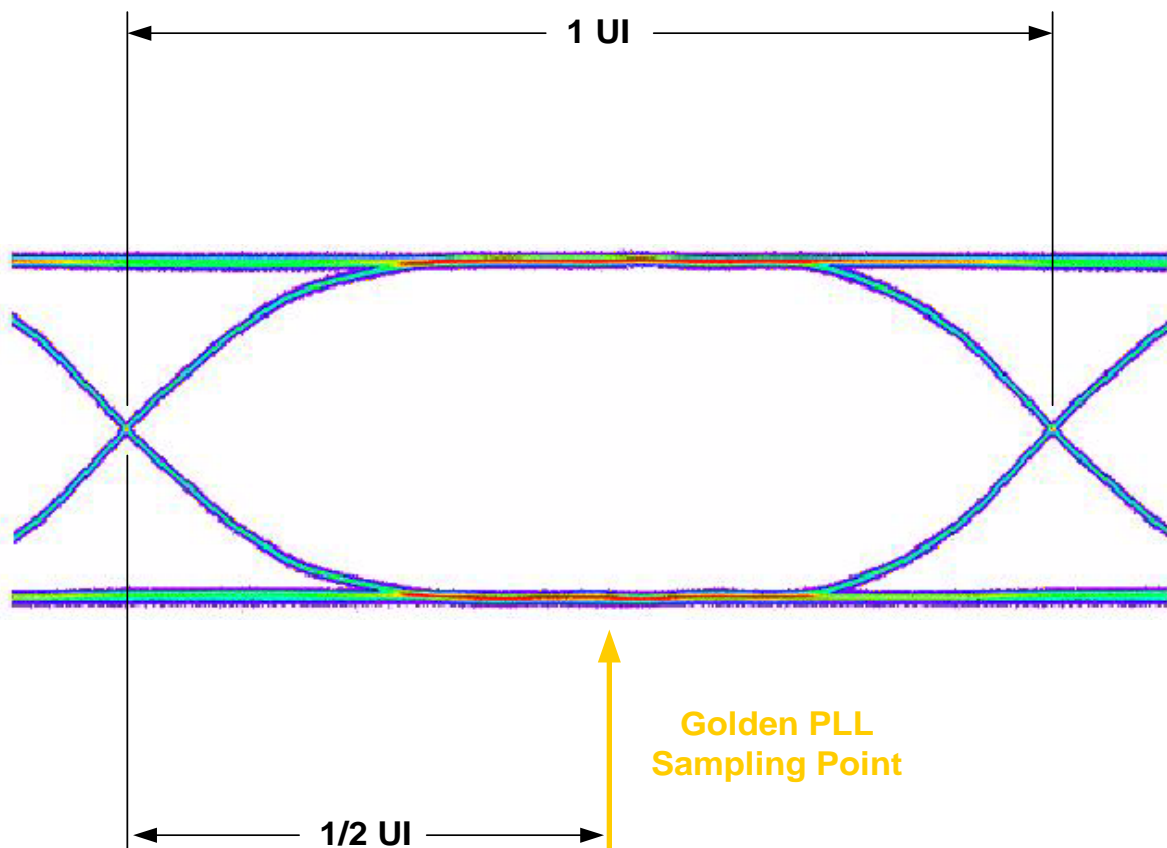


Figure 2-5: Data eye and sampling clock timing relationship

The link quality eye diagram provides a measurement of the alignment jitter margin present at a specification point in a single link. The receiver tolerance eye diagram provides both a specification of required receiver alignment jitter tolerance and a measurement of system alignment jitter margin.

The golden PLL model must emulate the worst-case performance corner. Eye masks define the limits necessary for the required performance.

2.1.5 Link Quality

Link quality describes the minimum performance of components and modules along a single link.

2.1.5.1 Alignment Jitter

Link quality eye diagrams insure both link operation and system level performance. A jitter budget is created top down starting from SP4. The difference between the SP's gives the tolerable contribution of alignment jitter for the respective module or line. As an example, link quality eyes can be required at every point along the link to allow each module's alignment jitter contribution to be specified. Thus module design can be performed to tangible jitter specifications. Likewise module jitter performance can be used to estimate receiver and hence link performance. An example of the possible locations that an eye diagram can be located in a link is shown in Figure 2-6.

For any specification points requiring eye diagrams, the sub-specification must include the following:

- 1) Complete golden PLL model used to form the eye
- 2) Eye mask table detailing all shapes and points necessary to construct the mask
- 3) Bit error rate (BER)

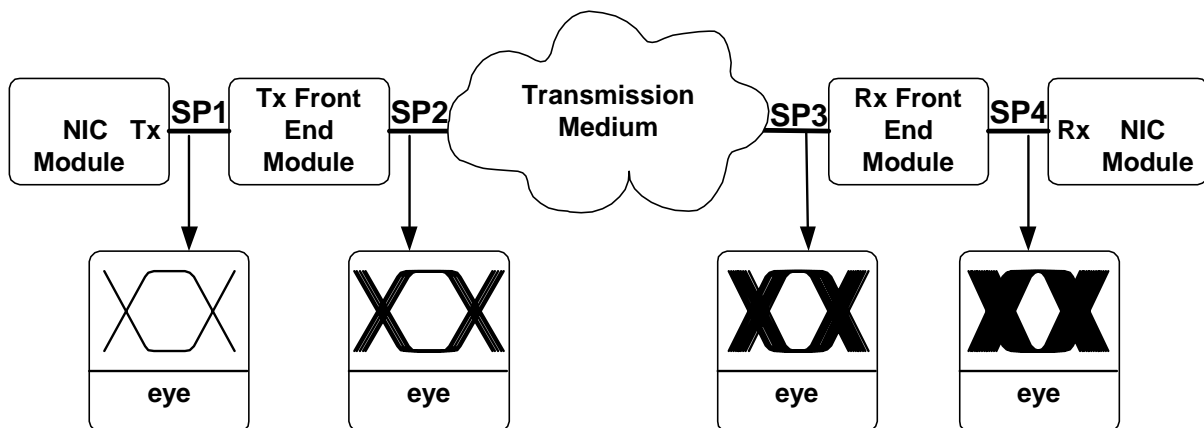


Figure 2-6: Illustration of eye diagrams at possible places in a link

2.1.5.2 Transferred Jitter

A portion of every jitter source on the network will have some spectral content below the jitter filter bandwidth. Jitter passed by the filter will accumulate in the following nodes. Transferred jitter from all sources combines to form accumulated jitter. Accumulated jitter starts small with the first slave and gets larger towards the end of the ring. Therefore, the total jitter at the last SP4 point in the network will have two components, one being the total jitter generated in the final link, and the second being the accumulated jitter from all the links before. This accumulated jitter must be controlled to prevent end of ring eye closure and receiver failure. The timing-master device must be able to tolerate the peak-to-peak swing of this accumulated jitter. Therefore transferred jitter is a measurement critical to system performance. Transferred jitter is measured by filtering the phase-variation at any SPn with a jitter filter. The RMS (standard deviation) of the output of this jitter filter is the amount of jitter contributed to accumulated jitter. When setting a transferred jitter limit, care must be taken to insure that possible correlated jitter sources are controlled, while allowing the manufacturability of devices and components. Transferred jitter specs can be placed at every spec point as shown in Figure 2-7.

For any specification point requiring transferred jitter measurements, the sub-specification must include the following:

- 1) The acceptable jitter limit
- 2) The complete jitter filter model used to calculate the transferred jitter
- 3) A measurement of transferred Jitter must be performed considering the BER

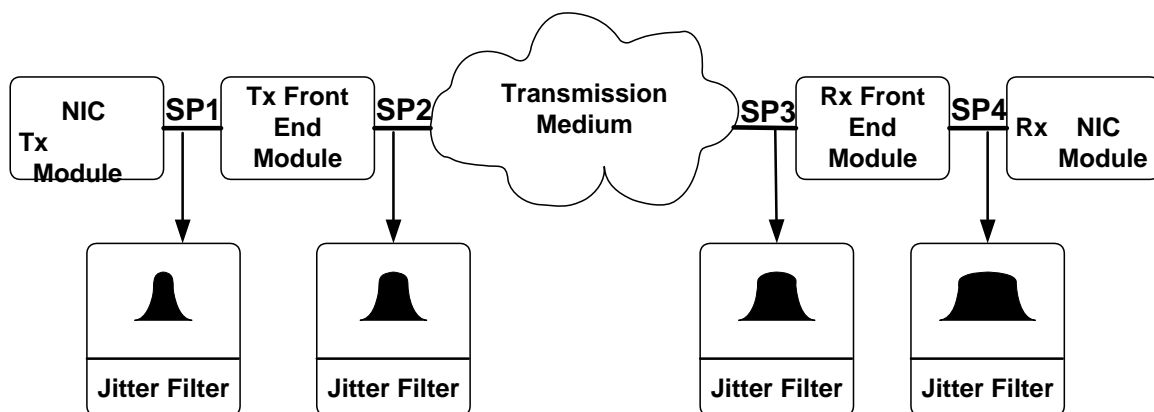


Figure 2-7: Illustration of transferred jitter accumulation at various places in a link

2.1.6 System Quality

2.1.6.1 Receiver Tolerance

Receiver tolerance describes the minimum alignment jitter tolerance of a NIC and the maximum tolerable alignment jitter that may occur at any place in the network.

Receiver Tolerance defines the minimum and maximum limits for the eye pattern. The tolerance is specified as an eye mask that is more closed than the allowable total system jitter. This closure originates from accumulated jitter in the system. A NIC must be able to recover all signals which satisfy the SP4 receiver tolerance mask, while a device shall be able to recover all signals that satisfy the SP3 link quality requirements. These eye patterns can also be used for system analysis as well. Proper system operation is guaranteed for any signals that meet these masks at specified points in the system. Figure 2-8 shows the typical locations in a ring where the SP4 receiver tolerance limits could be applied as a test of system performance.

The sub-specification must specify the following:

- 1) System locations and specification points which require the receiver tolerance mask to be valid.
- 2) Complete golden PLL model used to form the eye

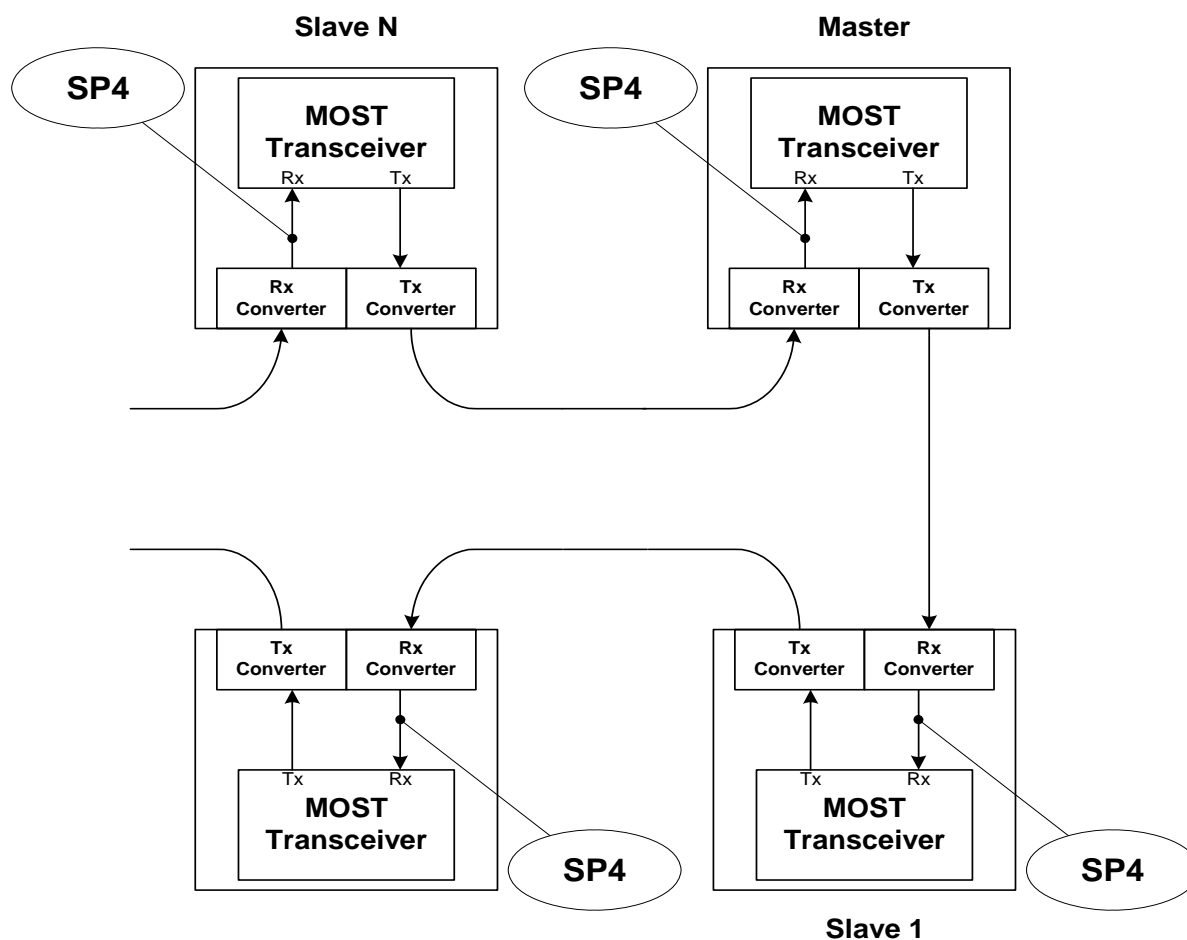


Figure 2-8: Locations where receiver tolerance eye mask can be applied

2.1.6.2 Master Delay Tolerance

An additional limitation for network stability on a system level is determined by the ability of the timing-master node to tolerate the accumulated delay present at the end of the ring. The maximum amount of accumulated delay for a MOST NIC in timing-master mode is called master delay tolerance.

Master delay tolerance is tied to the delay, transferred jitter, transferred wander, and maximum node count. It must be specified at the sub-specification level.

Table 2-1 shows the overall formula determining the minimum value for the Master Delay Tolerance T_{MDT} . The relevance of the delay respectively different types of phase-variation on the accumulate delay is shown in Table 2-2.

Master Delay Tolerance T_{MDT}	
The requirements for the system design are combined in the formula below:	
$T_{MDT} \geq t_{D\ Rx}(Master) + t_{D\ Tx}(Master) + \sum_{n=1}^{m-1} t_D(n) + \sum_{n=1}^m t_W(n) + t_{D\ Medium} + \alpha * \sqrt{\sum_{n=1}^m t_{TJ}(n)^2}$	
T_{MDT} :	Master Delay Tolerance
m :	Number of node links in a ring
$t_{D\ Rx}(n)$:	Delay per node n caused by Rx converter
$t_{D\ NIC}(n)$:	Delay per node n caused by NIC
$t_{D\ Tx}(n)$:	Delay per node n caused by Tx converter
$t_{D\ Medium}$:	Total delay caused by the medium
$t_D(n)$:	Delay per node = $t_{D\ Rx}(n) + t_{D\ NIC}(n) + t_{D\ Tx}(n)$
$t_W(n)$:	Wander (Phase Drift) per node and link (p-p)
$t_{TJ}(n)$:	Transferred Jitter per node (RMS) (i.e. $\alpha = 12$, derived from +/- 6 sigma for BER = 10^{-9})
Assumption:	
t_W is correlated from node to node	
t_{TJ} is uncorrelated from node to node	

Table 2-1: Relationship of Delay and System Jitter Parameters

Delay	Formula	Consequence on Delay
Delay of Timing Master node	$t_{D\ Rx}(Master) + t_{D\ Tx}(Master)$	Delay caused by Rx converter resp. Tx converter of the Timing Master node.
Accumulation of Delay of Timing Slave nodes	$\sum_{n=1}^{m-1} t_D(n)$	Delay caused by the (m-1) Timing Slave nodes. The delay per node is determined by the contribution of Rx converter, NIC and Tx converter, consequently $t_D(n) = t_{D\ Rx}(n) + t_{D\ NIC}(n) + t_{D\ Tx}(n)$.
Delay of the medium	$t_{D\ Medium}$	Total delay caused by the medium (e.g. depending on the length of the medium in use).
Accumulation of Wander	$\sum_{n=1}^m t_W(n)$	Due to the low frequency characteristic of Wander, either most or all of this phase-variation is transferred by a PLL. Wander is generated by all active components of the link and by the MOST NIC chip. Wander is most commonly caused by variations in temperature. It shall be specified in the data sheet of each active component.

Delay	Formula	Consequence on Delay
Accumulation of Transferred Jitter	$\alpha * \sqrt{\sum_{n=1}^m t_{TJ}(n)^2}$	Uncorrelated jitter sources add according to their variance. Scrambled data eliminates the correlation between DDJ on successive nodes. OEC noise and PLL noise sources are typically uncorrelated as well. This p-p number can be directly tied to a bit error rate when the assumed jitter PDF is normal. E.g. $\alpha = 12$ in case of +/- 6 sigma for BER= 10^{-9} .

Table 2-2: System Delay and Jitter Parameters

A MOST System that complies with the formula stated in Table 2-1, will have proper master operation under all conditions.

2.2 Amplitude Distortion

2.2.1 Transition Times

Signal transition times must be carefully considered to prevent excessive EMI generation when they are too fast or excessive jitter generation when they are too slow. Eye masks provide some protection against slow and fast rise times, but may be insufficient in preventing all slow or fast rise time cases in a network.

The sub-specification may specify rise time constraints as either a pulse template or traditional rise time specifications.

2.2.2 Signal Ringing

Signal ringing can produce data-dependant jitter and will produce excessive EMI. Eye mask can be created to control signal overshoot.

The sub-specification may specify bounding bars on top and bottom of the eye mask to place limits on signal ringing.

2.3 Other physical layer parameters

2.3.1 Network Coding

Device coding scheme is required to calculate the bit rate and to insure proper communication between NICs. It must be referenced in the sub-specification.

2.3.2 Bit rate

It is mandatory that the Bit rate is specified (min., typ., max.) in the sub specification (Mbit/s). It is valid for SP1 to SP4.

2.3.3 Node Count

Maximum node count must be specified. This parameter is required to understand the worst-case for all phase-variation related specs.

2.3.4 Diagnostic Functions

Network wide physical layer diagnostic functions should be defined in the sub-specification. An example of this is an optical power stress. This test feature may be used to allow the network to be self-diagnosing in regards to system power and jitter margin. These functions will depend on whether the system is optical or electrical and how much margin the system is required to have.

Diagnostic functions are normally initiated and controlled by higher layers in the network. The physical layer may be responsible for only a sub-set of these functions. This sub-set of functions or features must be thoroughly described in the sub-specification.

2.3.5 Optical Parameters (oPHY only)

Following parameters shall be considered for oPHY sub-specifications (min., typ., max.):

- Peak Wavelength SP2/3
- Average Optical output power or Optical Output Power based on the Optical Modulation Amplitude (OMA) SP2
- Average Optical output power for "Light off" SP2
- Extinction ratio SP2/3
- Optical Overshoot and Signal Ripple SP2/3
- Receivable optical power range for data recovery (average or OMA) SP3
- Receivable optical power range for switching to "Light off state" SP3

2.3.6 Electrical Parameters (ePHY only)

Following parameters shall be considered for ePHY sub-specifications (min., typ., max.):

- EMC, EMI
- Cable details
- Impedances, Matching
- Skewing
- Contact resistance

2.3.7 Switch ON/Off Parameters

There are various options for starting up or shutting down a MOST network. The requirements for the hardware components and modules along the link need to be specified in the respective physical layer sub-specification. These procedures will depend on the type of system and the required on/off transition algorithms. The sub-specification should handle these details with consideration of the hardware modules that are involved in the process. This may result in parameters for SP1 to SP4 like Power-ON delay, Power-OFF delay, and the signaling conditions on the link during those procedures.

2.3.8 Logic Levels

The logic levels at SP1/4 (also SP2/3 at ePHY) shall be specified within the corresponding sub specification. Referring to known standards like LVDS is highly recommended.

2.3.9 Environmental Requirements

Environmental requirements like Temperature Range, Humidity or Vibration are not part of the physical layer specification or of the sub-specifications. However, hints to standards can be given which allude to possible field of applications (automotive, industrial, home networks, etc.)

3 Device Connector

The device connector is part of the corresponding sub-specification. It contains all allowed options, number of electrical or optical contacts and a detailed mechanical drawing of each option.

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Notes:

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