

MOST[®]

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST50 bPHY Automotive Physical Layer
Sub-Specification – Errata 1
Rev. 1.0E1
06/2019**

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1 References

Number	Document
[1]	MOST Specification Rev 3.1
[2]	MOST Physical Layer Basic Specification Rev. 1.0
[3]	Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits (JEDEC No. JESD8C.01)

Table 1-1: References

2 Document History

Revision 1.0E1

Change Ref.	Chapter	Changes
1V0E1_001	6.1	The PSD of the SP2 signal shall remain between the upper and the lower limit of the PSD mask.
1.0E1_002	6.1	Add “8)” at PSD mask in Table 6.1
1.0E1_003	7.3.2	Figure 7-1: EBC Timing Diagrams, upper value: $V_{EBC_OR\ MIN} \rightarrow V_{EBC_OR\ MAX}$.
1.0E1_004	6.1	Add notes: 9) Using MOST50 bPHY stress test pattern: Transferred jitter; Eye-mask 10) Using MOST50 PSD stress test pattern: PSD mask 11) Using MOST50 bPHY stress test pattern or MOST50 PSD stress test pattern: RMS signal amplitude
1.0E1_005	6.1	SP2 Table/Notes with respect to PSD: dBm \rightarrow „dBm/Hz“
1.0E1_006	6.1	8) PSD Power values are equivalent to Differential Signal Amplitude measured at 100 Ω PSD Power [dBm] = (Signal-Amplitude [VRMS]) ² / 100 [Ω] \rightarrow 8) Discrete power values forming the PSD are equivalent to Differential Signal Amplitude measured at 100 Ω . Accumulated power of PSD corresponds to (Signal-Amplitude [VRMS]) ² / 100 [Ω]
1.0E1_007	6.2.2.2	Return loss magnitude in dB shall remain outside the boundaries given in Table 6-4 (p. 21)
1.0E1_008	6.2.2.2	Add test mode for RL measurement: The ECU shall be set into an appropriate test mode. The supplier of the MNC shall enable appropriate test modes for RL evaluation.
1.0E1_009	5.1 5.2	Divide Cut Off Frequency (F_{P1} un F_{J1}) by 2: Table 5-1: $F_{P1} = 62.5$ kHz (instead of 125 kHz) Table 5-2: $F_{J1} = 100$ kHz (instead of 200 kHz)
1.0E1_010	7.3.3	Restricted visibility of STATUS signal, Fig. 7-2 adapted.
1.0E1_011	6.1; 6.3	Shift budget signal amplitude: V_{rms2_min} : 400 mV \rightarrow 360 mV; V_{rms3_min} : 300 mV \rightarrow 260 mV
1.0E1_012	6.1	Realign PSD mask (adaptation, extension,, RBW)

Revision 1.0

Revision	Changes
1.0	Initial version (Not compatible with MOST Electrical Physical Layer Specification Rev 1.1, 06/2006)

3 Terminology and Abbreviations

AFE: Analog Front-End

BPF: Bits Per Frame

BER: Bit Error Rate

BM: Balanced Media (e.g. unshielded twisted pair, shielded twisted pair cable)

BEC: Balanced Media to Electrical Converter

BTR: Balanced Media Transceiver

DC Adaptive Coding (DCA): coding method used for MOST50 bPHY automotive network

DC: Direct Current, referring to a steady state signal

Digital Sum Value (DSV): accumulated DC offset contained in the data

EBC: Electrical to Balanced Media Converter

ECU: electronic control unit

Frequency Reference: A device, usually crystal controlled, which provides an accurate and low drift frequency standard for the MNC and network timing

MNC: MOST network controller

Network Frame Rate (Fs): The frequency at which frames are transmitted on the MOST50 bPHY automotive network

OEM: Original Equipment Manufacturer

PCB: Printed Circuit Board

PSD: Power Spectrum Density

PLL: phase locked loop

RBW: Resolution Bandwidth

RL: Return Loss

RMS: root mean square

RX Data: MOST50 bPHY automotive encoded digital bit stream being received

SP1...4: Specification Points 1 to 4

TDR: Time Domain Reflectometry

TX Data: MOST50 bPHY automotive encoded digital bit stream being transmitted

UI: unit interval (see section 4.2.2)

This sub-specification references additional terms in [2]. Abbreviations that are defined in that specification are also valid here.

3.1 Usage of Expressions

The following table covers usage of expressions:

Expression	Meaning
Shall	Mandatory provision to maintain compliance.
Must	
Shall Not	Prohibition whose violation results in non-compliance
Must Not	
Should	Recommended but not mandatory.
May	Feature might or might not be present, at the option of the implementer, and has no effect on compliance.
Can	

Table 3-1: Meanings of Expressions

3.2 Resolution of Conflicts

If there are any conflicts between the textual information presented in this document and the corresponding figures, the text shall have priority in resolving the conflict.

3.3 Logic Terminology

The following tables serve to clarify the electrical logic descriptions used in this specification.

3.3.1 Single-Ended Low Voltage Digital Signals

The following table relates the words used in this document to the parameters defined in the JEDEC specification [3]. These words are used to describe the logic states of signals /RST and STATUS.

Expression	Corresponding JEDEC Parameter
Low	V_{OL}
Logic 0	
0	
Zero	
High	V_{OH}
Logic 1	
1	
One	

Table 3-2: Meaning of Logic Expressions for Single-Ended Signals

3.3.2 Differential Signals

The following table explains the expressions used to describe the logic states of the differential data signals

Expression	Corresponding Description
Disabled	The P and N terminals are in a high impedance state. Small leakage currents may exist which can cause an indeterminate voltage on the line/load.
Off	
Enabled	Both the P and the N terminals are driving the line/load. The outputs shall be at valid LVDS logic levels provided the input data is valid.
On	
Valid MOST Data	DCA encoded data that meets defined link quality parameters and bit rate requirements

4 General Network Parameters

4.1 Overview

This document describes the physical parameters and limits required to guarantee operation of the MOST50 bPHY (balanced media physical layer) automotive network. This sub-specification is an electrical physical layer specification and references terms and measurement methods defined in [2].

4.2 Network Coding

The following sections describe a technique of encoding digital data called DCA coding. This information is presented in order to assure a better understanding of the network but DCA coding is not a part of the physical layer specification [2].

4.2.1 Pulse Characteristics

MOST50 traffic is scrambled and encoded using DCA coding, resulting in a data-stream that contains timing information and is DC free. Data pulses range from 2 UI to 6 UI, yielding 5 different pulse widths, as shown in Figure 4-1.

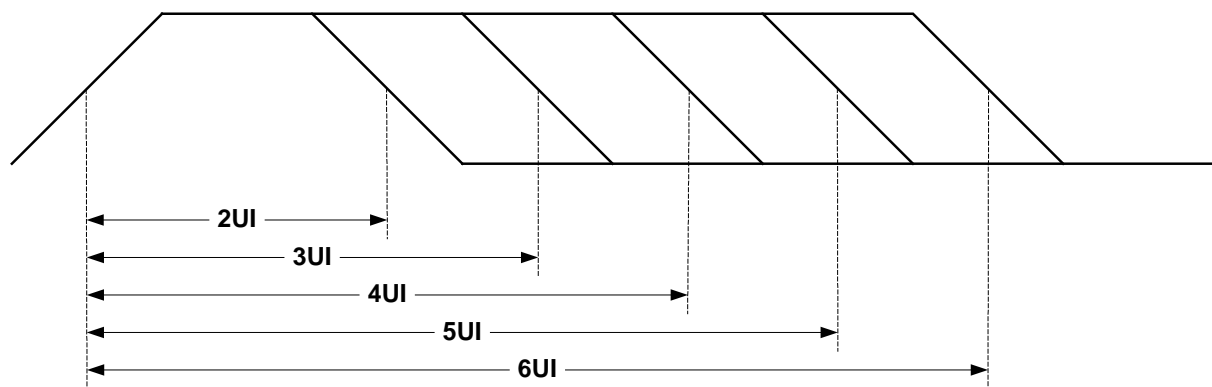


Figure 4-1: Allowable Pulse Widths When Using DCA Coding

4.2.2 Unit Interval Definition

The UI width calculation is shown in Equation 4-1.

$$UI = \frac{1}{F_s * 2 * BPF}$$

Equation 4-1: Unit Interval Calculation

For MOST50, there are 1024 Bits Per Frame (BPF). Using the above formula for a frame rate of 48.000 kHz will result in a Unit Interval of 10.173 ns.

4.2.3 DC Balance

DCA coding is inherently DC-free. However, short term imbalances in offset are required for data transmission. These imbalances are tracked with a running total called the Digital Sum Value (DSV). The DSV is calculated by incrementing the sum for every UI where the data is high, and decrementing the sum for every UI where the data is low. The calculation for DSV is illustrated in Figure 4-2.

Dynamic properties of DCA coding:

- The DSV is periodically driven to zero at least once per frame.
- The range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5}.
- The shortest DCA period is 4 UI.
- The longest DCA period is 10 UI.
- The data stream is guaranteed to have a period of 10 UI at least once per frame.
 - These 10 UI periods can either be made of pulses that are 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

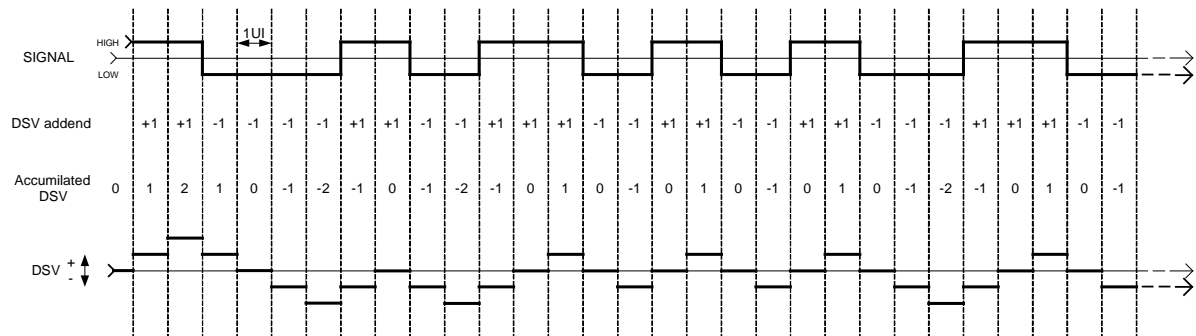


Figure 4-2: DSV Calculation

4.3 Link and interconnect type

This bPHY specification defines a 100 Ω end-terminated interconnect consisting of automotive grade balanced twisted-pair cables and connectors.

The system supports separate interconnects for transmit and receive links. The communication is unidirectional using two separate ports and cables per node.

4.4 Specification Point Details

The MOST Physical Layer Basic Specification [2], chapter 1 defines 4 specification points (SP1 ... SP4) and their respective location in a MOST link. SP1 and SP4 define the electrical signal requirements between a MOST Network Controller (MNC) with its input RX and output TX and a converter. SP1 and SP2 define the transmit converter while SP3 and SP4 define the receive converter. SP2 and SP3 define the properties of the interface between a MOST device and a wiring harness.

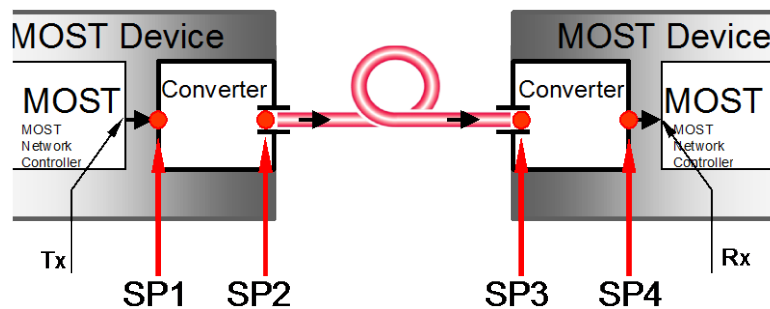


Figure 4-3: General Specification Point Locations

In systems that this sub-specification is applied to, the converters are used to adapt electrical digital signals into differential signals optimized to be fed into balanced media and vice versa. They are called EBC – Electrical to **B**alanced Media **C**onverter and BEC – **B**alanced Media to **E**lectrical **C**onverter. There is also an important section between transceiver pins and balanced media connector, containing further passive circuitry which is called **A**nalog **F**ront-**E**nd (AFE).

For an optimized infrastructure, EBC and BEC are assumed to be integrated in the MNC. Inside the chip, the converter portions are connected with the MNC TX/RX section. In consequence, SP1 and SP4 are moving inside the MNC. There is no direct access possible. Therefore, this sub-specification will omit definitions of SP1 and SP4 and focus instead on SP2 and SP3.

Performance criteria for SP2 include EBC and AFE. SP3 defines the signal characteristic after passing the channel. On the receive side, the signal characteristic at SP3, combined with AFE and BEC, is relevant for SP4 performance. Suppliers for MNCs are responsible to specify their product's signal characteristics at the chip IOs, EBC TX and EBC RX and suggest AFEs in an appropriate way to allow implementers to achieve the specified MOST requirements for SP2 and SP3.

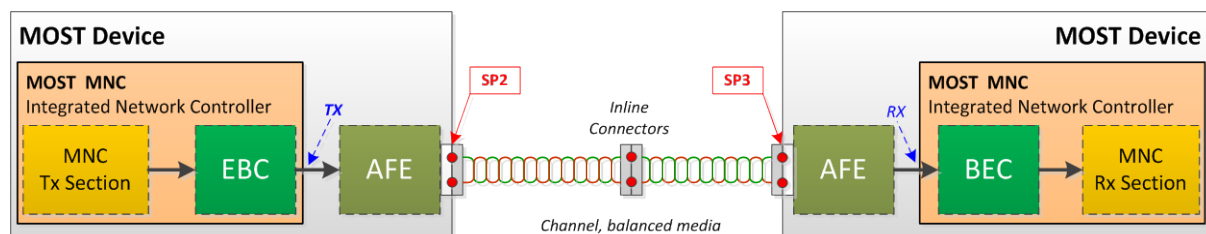


Figure 4-4: Specification Point Locations

Specification Point	Location	Electrical Interface
SP2	Signal at transmit port of balanced media interface	Analog
SP3	Signal at receive port of balanced media interface	Analog

Table 4-1: Specification Point Locations and Interfaces for integrated Transceivers

Analog Front-End

Suppliers of MNCs with integrated Transceivers will provide a connection scheme, defining requirements on connection and layout of the Transceivers with the Media Connector, this will include passive components.

Required properties for AFE and associated characteristics strongly depend on properties of individual transceiver designs (e.g. termination, band filter, common mode rejection, etc.). Various technical solutions may lead to the requested results. Therefore, suppliers of MNCs with integrated transceivers need to define EBC TX and BEC RX performance and AFE requirements for their individual products. The supplier product definition on EBC TX and BEC RX in combination with a suggested AFE shall allow implementers to achieve SP2 and SP3 requirements.

5 Models and Measurement Methods

The following models and methods are used as the basis for measurements in this sub-specification.

5.1 Golden PLL

The Golden PLL describes the required worst-case jitter performance of an MNC, and is used to form receiver eye diagrams. The Golden PLL must reference to the positive edge of the signal. The transfer function is a low-pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above.

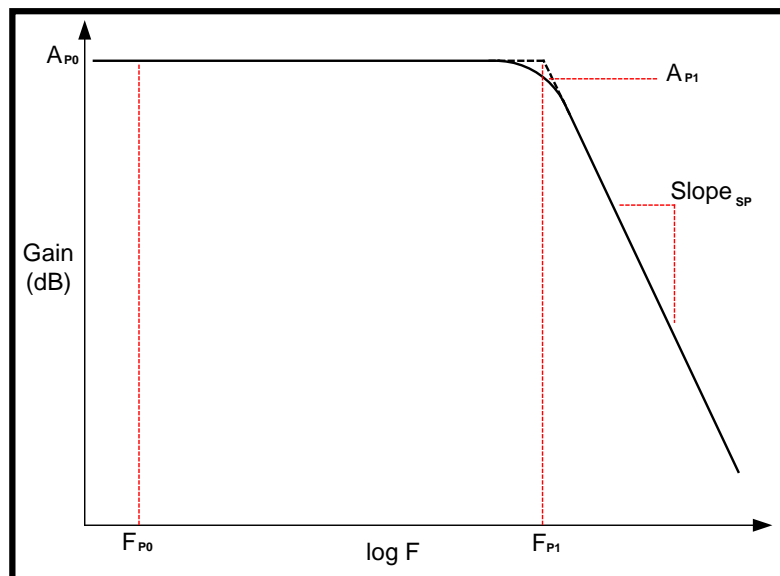


Figure 5-1: Golden PLL Transfer Function

Parameter	Value	Unit
A_{P0}	0	dB
F_{P0}	10	Hz
A_{P1}	-3	dB
F_{P1}	62.5	kHz
$Slope_{SP}$	-20	dB/dec

Table 5-1: Golden PLL Specifications

5.2 Jitter Filter

The jitter filter describes the worst-case jitter transfer function of an MNC, and is used to calculate transferred jitter along the link. The transfer function is a low-pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above. The jitter filter must reference to the positive edge of the signal.

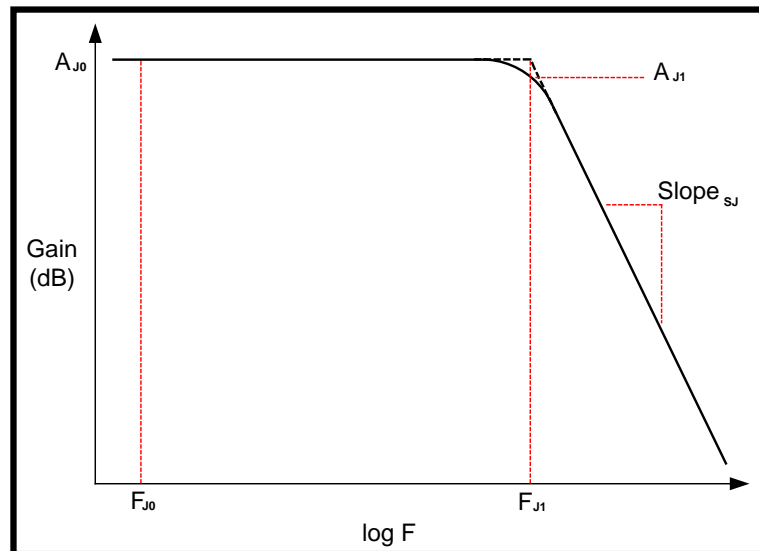


Figure 5-2: Jitter Filter Response

Parameter	Value	Unit
A_{J0}	0	dB
F_{J0}	10	Hz
A_{J1}	-3	dB
F_{J1}	100	kHz
$Slope_{SJ}$	-20	dB/dec

Table 5-2: Jitter Filter Specifications

5.3 Test Pattern

The MOST50 Stress Test Pattern shall be used for the following measurements:

- Signal level detection measurements
- All eye diagrams

The MOST50 PSD Test Pattern shall be used for the following measurements:

- PSD measurements

Description Code	File Name
MOST50 Stress Test Pattern	<i>MOST50_Stress_Pattern-1v0.pat</i>
MOST50 PSD Test Pattern	<i>MOST50_PSD_Pattern-1V0.pat</i>
	Files are available on www.mostcooperation.com

Table 5-3: Description of MOST50 Test Pattern

6 Link Specifications

This specification utilizes various methods to validate characteristics of the serial data link.

The spectral content of a transmitted signal is evaluated per Power Spectrum Density (PSD) method. A PSD mask template gives limit lines in the frequency domain. The PSD mask also puts limits to minimum and maximum signal power.

For jitter and pulse shape evaluation, this specification utilizes eye pattern diagrams and mask templates. A high-quality signal with low jitter and distortion will show a large eye opening, which can be compared to a standardized mask (a diamond shape) placed in the center of the eye. The mask is designed such that a good signal will not touch the mask at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitude, jitter, or pulse width variations will show up as closure in the eye diagram.

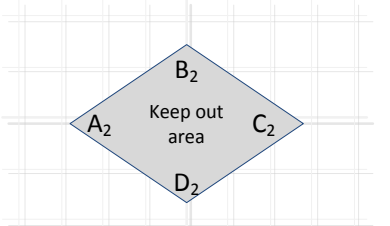
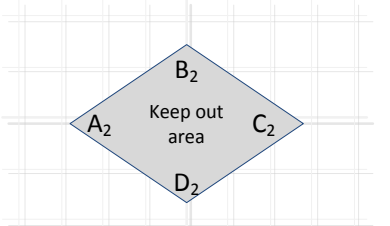
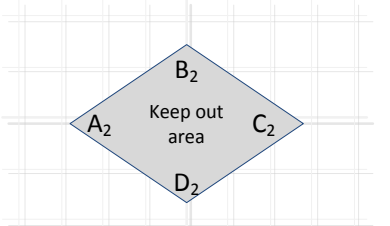
All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9} . Consequently, all of the mask violation parameters have been specified with that goal in mind.

6.1 Specification Point SP2

The signal at SP2 must meet the requirements in Table 6-1 and must not touch the “keep-out” area of the mask. Refer to sections 7.1, 8.3, and 9 for operating conditions and interface standards. All parameters are evaluated using specified MOST50 Stress Test Pattern.

The signal at SP2 is an AC waveform and may be accompanied by a DC offset, especially when transporting power along with the data over the balanced media interconnect / channel. In this instance, the DC level shall be removed before evaluating the signal. Table 6-1 is written assuming the DC value is 0 V.

The PSD of the SP2 signal shall remain between the upper and the lower limit of the PSD mask.

SP2 Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit																																																
RMS signal amplitude	V_{rms2}	4), 6), 11)	360		830	mV RMS																																																
Transferred jitter	J_{tr2}	1), 6), 9)			112	ps RMS																																																
Eye mask	$A_2 \dots D_2$	2), 3), 5), 6), 9)				-																																																
<table><tr><th>Parameter</th><th>Amplitude (mV)</th><th>Timing (UI)</th><th colspan="4">Eye mask</th></tr><tr><td>A_2</td><td>0</td><td>0.150</td><td colspan="4" rowspan="5"></td></tr><tr><td>B_2</td><td>230</td><td>0.500</td></tr><tr><td>C_2</td><td>0</td><td>0.850</td></tr><tr><td>D_2</td><td>230</td><td>0.500</td></tr><tr><td></td><td></td><td></td></tr></table>							Parameter	Amplitude (mV)	Timing (UI)	Eye mask				A_2	0	0.150					B_2	230	0.500	C_2	0	0.850	D_2	230	0.500																									
Parameter	Amplitude (mV)	Timing (UI)	Eye mask																																																			
A_2	0	0.150																																																				
B_2	230	0.500																																																				
C_2	0	0.850																																																				
D_2	230	0.500																																																				
PSD Mask	$U1 \dots U7$ $L1 \dots L4$	7), 8), 10)				dBm/Hz																																																
<table><tr><th>Upper Mask</th><th>Frequency (MHz)</th><th>Limit (dBm/Hz)</th><th>Lower Mask</th><th>Frequency (MHz)</th><th>Limit (dBm/Hz)</th></tr><tr><td>U1</td><td>1</td><td>-75.0</td><td>L1</td><td>4</td><td>-81.0</td></tr><tr><td>U2</td><td>8</td><td>-66.0</td><td>L2</td><td>8</td><td>-81.0</td></tr><tr><td>U3</td><td>14</td><td>-59.0</td><td>L3</td><td>15</td><td>-74.0</td></tr><tr><td>U4</td><td>20</td><td>-59.0</td><td>L4</td><td>30</td><td>-87.0</td></tr><tr><td>U5</td><td>60</td><td>-80.0</td><td></td><td></td><td></td></tr><tr><td>U6</td><td>100</td><td>-80.0</td><td></td><td></td><td></td></tr><tr><td>U7</td><td>≥ 250</td><td>-113.0</td><td></td><td></td><td></td></tr></table>							Upper Mask	Frequency (MHz)	Limit (dBm/Hz)	Lower Mask	Frequency (MHz)	Limit (dBm/Hz)	U1	1	-75.0	L1	4	-81.0	U2	8	-66.0	L2	8	-81.0	U3	14	-59.0	L3	15	-74.0	U4	20	-59.0	L4	30	-87.0	U5	60	-80.0				U6	100	-80.0				U7	≥ 250	-113.0			
Upper Mask	Frequency (MHz)	Limit (dBm/Hz)	Lower Mask	Frequency (MHz)	Limit (dBm/Hz)																																																	
U1	1	-75.0	L1	4	-81.0																																																	
U2	8	-66.0	L2	8	-81.0																																																	
U3	14	-59.0	L3	15	-74.0																																																	
U4	20	-59.0	L4	30	-87.0																																																	
U5	60	-80.0																																																				
U6	100	-80.0																																																				
U7	≥ 250	-113.0																																																				

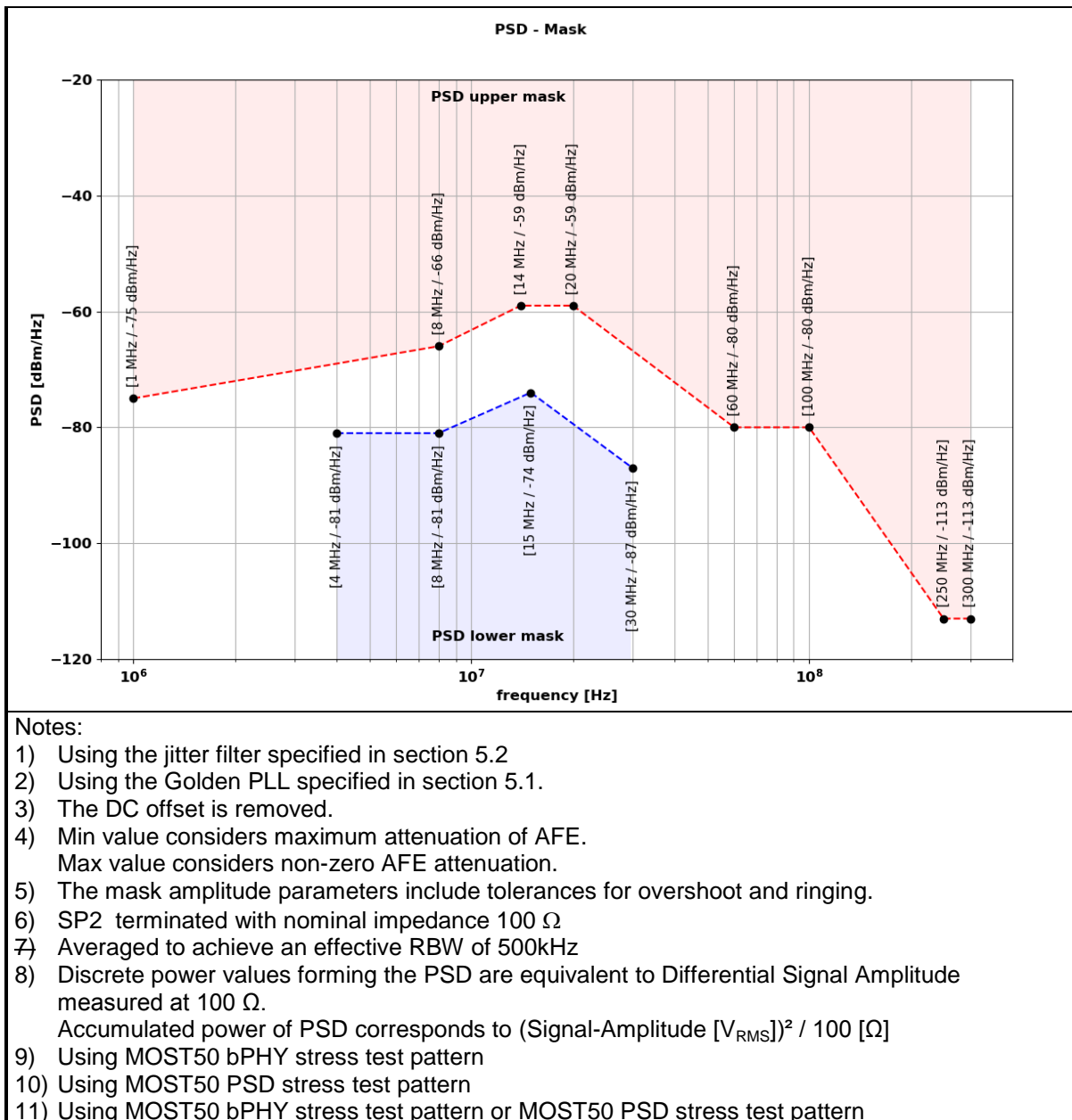


Table 6-1: Link Quality Parameters of SP2

6.2 Electrical Link Requirements

The transmission media is a prominent factor for setting the parameters of a physical layer. Between SP2 and SP3, there can be a single cable piece or a series of cables including inline connectors and device connectors. Together they form the balanced media interconnect.

The MOST50 bPHY specification is referenced to an ideal differential characteristic impedance of 100 Ω for balanced media and attached interfaces. All measurements are defined using a differential 100 Ω termination. However, the system tolerates deviation from 100 Ω in a wider range. It also allows implementations with system characteristic impedance centered with an offset to ideal 100 Ω for better interface matching.

6.2.1 Electrical Interconnect, Length and Attenuation

The maximum balanced media interconnect is given in Table 6-2. This length includes the cables and the connectors (device and in-line). A limitation on the number of in-line connectors is not required as long as the whole interconnect conforms to the specifications given in Table 6-2.

Attenuation of balanced media interconnect shall not exceed limits given by the Attenuation Limit curve in dB.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Electrical interconnect length	L _{ci}	1)	0	-	15	m
Attenuation Limit	Att _{Limit} (f)	1 MHz ... 66 MHz				
	$Att(f) = -0.30335 - \sqrt{\frac{f}{2.2795 * 10^6}} - 2.31979 * 10^{-8} * f$					
Note: 1) Parameter variations due to environmental conditions or mechanical stress being applied to the interconnect shall be considered.						

Table 6-2: Electrical Interconnect Attenuation Parameters

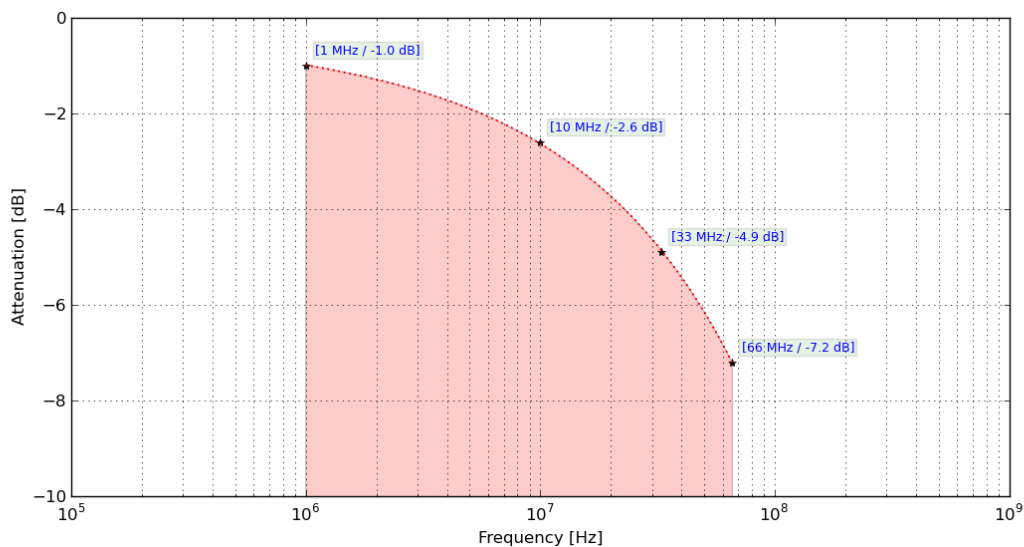


Figure 6-1: Attenuation Limit

Insertion loss considers all kind of losses that occur on an interconnect between SP2 and SP3; this includes losses due to dissipation, radiation, reflection and mode conversion. In the relevant frequency range, connector insertion losses are negligible.

6.2.2 Characteristic Impedance and Return Loss

This section defines requirements for characteristic impedance of components forming a balanced media interconnect and for AFE circuitry connecting to such interconnects. In general, impedance mismatches cause back reflection of a certain portion of the signal energy. The ratio of reflected signal relative to transmitted signal is called Return Loss. The definition of characteristic impedance is either given as impedance [Ω] or as Return Loss [dB], whatever is better suited for the component.

Due to simplex operation, Return Loss on a transmit path means a minor reduction of signal amplitude in transmit direction. Such losses are already included inherently in some of the aforementioned specifications:

- Output signal specification:
This covers amplitude reduction due to Return Losses inside the ECU, caused by an interface impedance mismatch to nominal differential characteristic impedance (100 Ω) of the standard measurement equipment.
- Attenuation requirements (Table 6-2: Electrical Interconnect Attenuation Parameters) for balanced media interconnects:
The measurement of Attenuation inherently includes all losses. Therefore it includes Return losses caused by impedance mismatches within segments of a balanced media interconnect (channel) and by mismatches of the balanced media interconnects to nominal differential characteristic impedance (100 Ω) of the standard Measurement Equipment.
- Amplitude reduction due to Return Losses at Receive Interfaces (such as SP3), caused by mismatch of input impedance must be included in the Receive Tolerance Specification.

6.2.2.1 Electrical Interconnect, Characteristic Impedance and Return Loss

Balanced media interconnect between SP2 and SP3, as a composition of cables and connectors, shall have characteristic impedance as given in Table 6-3.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Characteristic impedance of cable	$Z_{0\text{cable}}$	1)	90	100	140	Ω
Note: 1) Parameter variations, due to environmental conditions or mechanical stress shall be considered. Refer to sections 7.1 and 8.3 for operating conditions.						

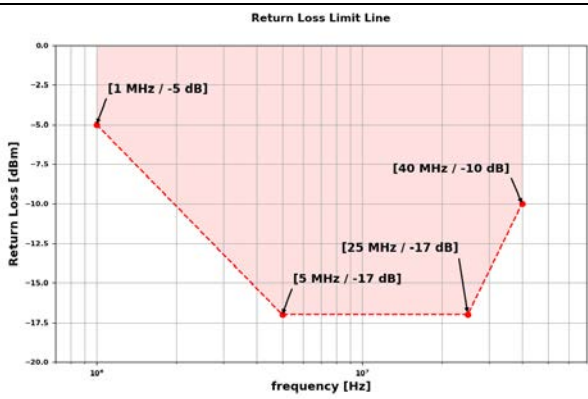
Table 6-3: Electrical Interconnect Characteristic Impedance

6.2.2.2 PCB Interfaces, Characteristic Impedance and Return Loss

Signals going to or coming from balanced media interconnect are electrically connected to the transceivers on the PCB. Specification of SP2 already includes output characteristic and potential losses due to board traces, passive components and board connector. SP3 represents the signal characteristic at the end of a balanced media interconnect, terminated with ideally 100 Ω . Potential signal degradation due to board traces, passive components and board connector between SP3 and transceiver input have to be additionally considered. The combination of board traces, passive components and board connector is summarized under the term analog front-end (AFE). In some cases, the length of the electrical connection between the device connector and the transceiver could be long enough to adversely affect the signal integrity.

Table 6-4 describes the requirements for PCB Interfaces connected to SP2 and SP3.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Return loss of ECU-Interface, measured at device connector	RL _{SP2} RL _{SP3}	A, B, C, D 1), 2), 3)			≤ Limit Line	

	Frequency	Return Loss	Limit Line
A	1 MHz	-5 dB	
B	5 MHz	-17 dB	
C	25 MHz	-17 dB	
D	40 MHz	-10 dB	

Notes:

- 1) Parameter variations, due to environmental conditions or mechanical stress shall be considered. Refer to sections 7.1, 8.3 for operating conditions.
- 2) Nominal Characteristic Impedance 100 Ω.
- 3) The ECU shall be set into an appropriate test mode. The supplier of the MNC shall enable appropriate test modes for RL evaluation.

Table 6-4: PCB-Interface Impedance and Return Loss Parameters

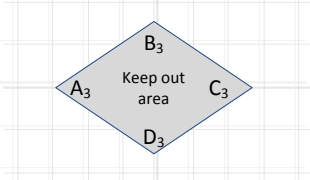
Return loss magnitude in dB shall remain outside the boundaries given in Table 6-4.

6.3 Specification Point SP3

The variations in the signal integrity at SP3 are mainly constrained by the definitions of SP2 link quality (Section 6.1) and the electrical interconnect attenuation requirements (section 6.2.1). Stimuli for SP3 can be calculated by filtering a signal representing a SP2 corner condition (shaped stress pattern, to form minimum/maximum PSD) using a filter with a transfer function given by Table 6-2.

Further signal degradation at SP3 may occur due to amplitude noise coupled on the data signal along the link. Amplitude noise reduces signal-to-noise ratio and may also cause jitter on the signal. Potential noise sources in general are EMC, crosstalk from neighboring signals. Potential deterioration by EMC and crosstalk from neighboring signals is not subject of this specification.

Link Quality SP3	Symbol	Condition	Min.	Typ.	Max.	Unit
RMS signal amplitude	V_{rms3}	4), 6)	260		-	mV RMS
Transferred jitter	J_{tr3}	1)			190	ps RMS
Eye mask	$A_3 \dots D_3$	2), 3), 5)				-

Parameter	Amplitude (mV)	Timing (UI)	Eye mask
A_3	0	0.200	
B_3	120	0.500	
C_3	0	0.800	
D_3	-120	0.500	

Notes:

- 1) Using the jitter filter specified in section 5.2.
- 2) Using the Golden PLL specified in section 5.1.
- 3) The DC offset is removed.
- 4) Min value considers SP2 conditions and Interconnect insertion loss
- 5) The mask amplitude parameters include tolerances for overshoot and ringing.
- 6) SP3, terminated with nominal impedance 100 Ω .

Table 6-5: Link Quality Parameters of SP3

7 Power Up and Power Down

7.1 ECU Requirements

The ECU must provide the following: a stable frequency reference for the MNC, power supply for the MNC, EBC and BEC, and power supply monitoring circuitry.

- Frequency reference:
The frequency reference is typically a crystal-controlled oscillator or derivative. The required accuracy is specified in section 9.1.
- Power supply:
 - Continuous power supply: V_{CCCN} , with a nominal operating range of $3.3\text{ V} \pm 5\%$, which shall always be supplied. This power supply is used to power BEC (or BTR, see section 7.3.1).
 - Switched power supply: V_{CCSW} , with a nominal operating range of $3.3\text{ V} \pm 5\%$, which must be able to be turned off. This power supply is used to power MNC and EBC (or BTR, see section 7.3.1).
- Power supply monitoring circuitry:
The ECU shall provide power supply monitoring circuitry, as specified in section 7.2 for supervising the switched power supply V_{CCSW} . The ECU shall connect the active-low reset signal /RST provided by the power supply monitoring circuitry to the /RST inputs of the EBC (BTR) and the MNC.
In case the BTR is powered by V_{CCCN} only (see section 7.3.1), the ECU design shall ensure that the /RST signal voltage always stays below V_{CCSW} .

7.2 Power Supply Monitoring Circuitry

The power supply monitoring circuitry shall:

- Provide an active-low reset signal /RST, which is valid LVTTTL (JESD8C) signal over the power supply range V_{VALID} , as specified in Table 7-1.
- Set the /RST signal high when the V_{CCSW} ramps above the threshold, V_T . Switching from low to high shall be delayed by a minimum time of t_{D+} to allow the circuitry in the EBC to stabilize, the RX and TX pins of the MNC to be driven, and the local frequency reference to stabilize. Although a maximum time for t_{D+} is not specified, an implicit maximum value exists due to the required start-up time. Refer to the MOST Specification [1] for more details.
- Set the /RST signal to low, when the V_{CCSW} voltage drops below the threshold V_T . Switching from high to low shall occur within a time of t_{D-} .

/RST Signal	Symbol	Condition	Min	Max	Unit
Supply range for valid logic levels	V_{VALID}		1	3.465	V
Logic switching threshold	V_T		2.970	-	V
Logic 0 to 1 time delay	t_{D+}		1	-	ms
Logic 1 to 0 time delay	t_{D-}		0	100	μs

Table 7-1: Specifications for /RST Signal Generation

7.3 Electrical Transceiver, EBC and BEC

System wakeup and shutdown methods require certain functionality to be built into the EBC and BEC sub-sections of a balanced media transceiver.

7.3.1 BTR Requirements

If a BTR has only one power domain (common power supply for EBC and BEC sub-sections) it must

- fulfill $I_{ccsleep}$ requirements defined in Table 7-3 during *Off-State with /RST input driven low* and
- fulfill all the requirements for EBC and BEC, where all power supply related parameters (V_{EBC_OR} , V_{EBC_GR} , V_{EBC_OFF} , and V_{BEC_OR}) are referred to the actual BTR power supply used.

7.3.2 EBC Requirements

The EBC functional requirements are listed below.

- a) The EBC must have an LVTTTL (JESD8C) active low reset input pin (/RST).
- b) The *Off-State* for the EBC is defined as follows:
 - The EBC must not generate output transitions.
- c) The *On-State* for the EBC is defined as follows:
 - The EBC shall produce an output signal, compliant with all the SP2 parameters defined in Table 6-1 when being driven from MNC TX section.
- d) The EBC must not generate any output, capable of waking up a following device, when being supplied with an operating voltage within V_{EBC_OFF} regardless of the state of the MNC TX and /RST inputs.
- e) When /RST input is low, EBC shall produce no output transitions.
- f) When being supplied with an operating voltage within V_{EBC_OR} , the EBC shall settle into operation defined as the *On-State* within a time t_{ON2} when:
 - The /RST input pin is driven high
- g) When being supplied with an operating voltage within V_{EBC_GR} , the EBC enters the *Off-State* within a time t_{OFF2} when
 - The /RST input pin is driven low

The EBC requirements are summarized in Table 7-2. Refer to Figure 7-1 for more details.

EBC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
EBC Operating Voltage Range	V_{EBC_OR}		3.135	3.300	3.465	V
EBC Glitch-Safe Voltage Range	V_{EBC_GR}		2.970	-	3.465	V
EBC Off Voltage Range	V_{EBC_OFF}		0	-	1	V
EBC power on delay	t_{ON2}	1)	-	-	100	μs
EBC power off delay	t_{OFF2}		-	-	2	μs

Note:
1) Valid MOST data at SP2 after t_{ON2} provided that the MNC delivers the valid data according to its specification.

Table 7-2: EBC Power State Requirements

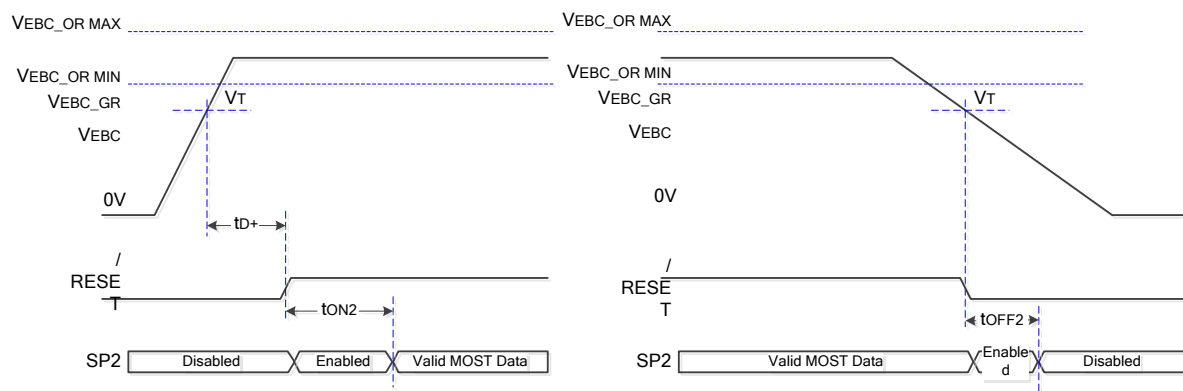


Figure 7-1: EBC Timing Diagrams

7.3.2.1 Example Scenarios

A typical powering up sequence and a typical powering down sequence for the EBC are described below and are referenced to Figure 7-1. In this figure, Valid MOST Data is defined as follows:

For SP2, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-1, and the bit rate requirements defined in Table 9-1.

7.3.2.1.1 Power On Sequence

The power-on sequence starts with the system power supply voltage to the MNC and EBC ramping up. During the time at which the switched power supply voltage is not within the EBC's normal operating range, the /RST pin is pulled low by the power supply monitoring circuitry to prevent edges from being generated at SP2. Immediately after the supply voltage has reached its normal operating level, the circuitry inside the MNC and EBC may not have fully stabilized. The power supply monitoring circuitry provides a time delay from when the supply voltage has reached its normal operating value until /RST goes high so that the local frequency reference, MNC circuitry, and EBC circuitry will have time to stabilize. Some time after the power supply has reached its typical value, the local frequency reference that provides the MNC with timing will have stabilized, /RST is high, the EBC can then drive valid data on SP2 after an allowed short period of undefined data due to the AC-coupling between the output of the EBC and SP2. During this undefined data period the signal will balance, making use of the DC-balancing of the DCA data signal.

7.3.2.1.2 Power Off Sequence

The normal power-off sequence is initiated by MNC TX traffic being stopped. The EMBC, consequently, does not provide any transitions. The power supply to the MNC will be shut down some time later. During the ramp down of the power supply, the /RST pin transitions low before the MNC's power supply drops below the Glitch Safe Voltage Range, preventing any glitches on the output at SP2. The /RST signal is valid down to V_{VALID} min. Below V_{VALID} min, the EBC is responsible for preventing any signal oscillations at SP2 regardless of the state of /RST.

7.3.3 BEC Requirements

The BEC functional requirements are listed below. These requirements are applicable for the BEC when being powered by an operating voltage in the range defined by V_{BEC_OR} in Table 7-3:.

- a) The BEC must provide an output pin (STATUS) in accordance with LVTTTL (JESD8C) [3].
- b) A BEC in the *Off-State* must meet the following requirements:
 - The BEC must keep its STATUS signal high, the MNC RX disabled, and consume no more than the sleep current, $I_{CCSLEEP}$.
 - The BEC must monitor the amplitude and frequency at SP3.
- c) A BEC in the *On-State* must meet the following requirements:
 - The BEC must keep its STATUS signal low. When receiving valid data at SP3, the BEC must convert differential signal to an appropriate signal for the MNC Receive section.
- d) A BEC must transition from the *Off-State* to the *On-State* upon detecting valid wakeup conditions, defined as a signal with valid SP3 amplitude (see section 6.3) and a frequency within F_{ON3} as specified in Table 7-3. The wakeup procedure has the following requirement:
 - The BEC must transition the STATUS signal low within time t_{STATF} after valid wakeup conditions have been detected at SP3.
- e) A BEC in the *On-State* must constantly monitor the input signal frequency and input amplitude. A BEC must transition to the *Off-State* upon detecting valid shutdown conditions. When the signal at SP3 has a frequency within F_{OFF3} as specified in Table 7-3 or a too low SP3 amplitude (see section 6.3 and 6.2.1) the BEC must transition to *Off-State*. The transition procedure to the *Off-State* has the following requirements:
 - The BEC must set STATUS high within a time t_{STATR} upon detecting valid shutdown conditions on SP3.
- f) While F_{ON3} defines the frequency range where the BEC must be on and F_{OFF3} defines the frequency range where the BEC must be off, the actual transition points will be in the region between F_{OFF3} max. and F_{ON3} min.

For an optimized infrastructure, BEC is assumed to be integrated in the MNC (see section 4.4). Inside the chip, the relevant converter portions are connected with the MNC. Visibility of STATUS signal as defined in this section 7.3.2 might be restricted. STATUS as an externally accessible hardware signal is only required for transitioning from unpowered to a powered mode. In an unpowered node, STATUS is used to enable the Switched power supply V_{CCSW} . Once a node is powered, further power state handling is fully controlled by the MNC, which is most likely based on a MNC internal STATUS signal. Therefore, in powered state, external STATUS might be used for other purposes. Such restricted visibility of STATUS is acceptable as long as full testability of BEC Power States as specified in Table 7-3 is given.

The BEC must meet the requirements listed in Table 7-3. Refer to Figure 7-2 for more details.

BEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
Powering On						
Input signal RMS range for <i>On-State</i> operation	V_{ON3_RMS}		190			mV RMS
Frequency range of input at SP3 for <i>On-State</i> operation	F_{ON3}	1)	12.288	-	24.576	MHz
Delay to STATUS falling	t_{STATF}	2)	50	-	700	μs
BEC Operating Voltage Range	V_{BEC_OR}		3.135	3.300	3.465	V
Powering Off						
Input signal RMS range for <i>Off-State</i> operation	V_{OFF3}				67	mV RMS
Frequency range of input at SP3 for <i>Off-State</i> operation	F_{OFF3}		0	-	10	kHz
Delay to STATUS rising	t_{STATR}	3)	-	-	100	μs
Current consumption in the <i>Off-State</i>	$I_{CCSLEEP}$		-	-	50	μA
Notes: 1) The BEC can still be in the On-State above this frequency. 2) Time from valid wakeup condition to STATUS low, see section 7.3.3 d). 3) Time from signal off to STATUS high, see section 7.3.3 e).						

Table 7-3: BEC Power State Requirements

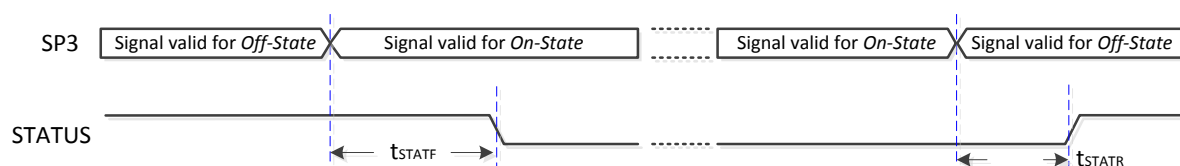


Figure 7-2: BEC Timing Diagram

7.3.3.1 Example Scenarios

The typical sequences explained below provide a description of the timing shown in Figure 7-2. Initially it is assumed, that the BEC is powered, but in its *Off-State* with STATUS high and the MNC RX disabled. In the above figure, Valid MOST Data is defined as follows:

- For SP3, Valid MOST Data is DCA encoded data that meets the link quality parameters according to section 6.2.2.1 and the bit rate requirements listed in Table 9-1.

7.3.3.1.1 Power On Sequence

A BEC that is in the *Off-State* monitors the input SP3 signal. The BEC verifies that the amplitude and signal frequency meet specifications before exiting the *Off-State*. If valid wakeup conditions are present, the BEC sets STATUS low, enables the BEC Receive circuitry. After a settling time, valid logic levels for the MNC internal receive domain are present although valid MOST data may not be on the bus yet. After a short period, the BEC is fully on and valid MOST data are being passed from SP3 to the internal MNC RX section.

7.3.3.1.2 Power Off Sequence

A BEC that is in the *On-State* is always monitoring the signal frequency at SP3. If the frequency does not meet specifications, the BEC begins transitioning to the *Off-State* by driving the STATUS pin high. Then the BEC disables the MNC RX and enters the *Off-State*.

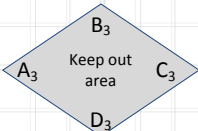
8 System Specifications

8.1 SP3 Receiver Tolerance

The mask is designed such that a good signal will not touch it at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitudes, jitter, or pulse width variations will show up as closure in the eye diagram. Signals with excessively high amplitudes will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.

All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9} . Consequently, all of the mask violation parameters have been specified with that goal in mind. Refer to sections 7.1, 8.3, and 9 for operating conditions and interface standards.

Receive Tolerance SP3	Symbol	Condition	Min.	Typ.	Max.	Unit
Eye mask	$A_{3T...}$ D_{3T}	1), 2), 3), 4), 5)				-

Parameter	Amplitude (mV)	Timing (UI)	Eye mask
A_3	0	0.225	
B_3	100	0.500	
C_3	0	0.775	
D_3	-100	0.500	

Notes:

1) Using the Golden PLL specified in section 5.1.

2) The DC offset is removed.

3) The mask amplitude parameters include tolerances for overshoot and ringing.

4) SP3, terminated with nominal impedance 100 Ω.

5) Input signal RMS range, according to V_{ON3_RMS} , Table 7-3.

Table 8-1: Receiver Tolerance Parameters of SP3

8.2 Master Delay Tolerance

The master delay is the sum of all static phase (delay) and phase variation measured between the RX input relative to the TX output of the TimingMaster device. The master delay and the total node count must not exceed the maximums shown in Table 8-2.

System Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Node Count	N		-	-	20	nodes
Master Delay Tolerance	T_{MDT}		-	-	$\frac{0.5}{F_s}$	μs

Table 8-2: Master Delay Tolerance Requirements

8.3 Environmental Considerations and Requirements

From the automotive OEM perspective, there are additional specifications which are considered to be minimum requirements. Nevertheless, certain OEMs may have additional requirements:

- The given parameters for all specification points have to be guaranteed by the ECU and its consisting subcomponents, under “automotive worst-case conditions”, which have to be considered as OEM specific requirements. Ambient conditions like temperature range, humidity, vibration and shock, resistance against chemical agents, EMC/EMI and lifetime are defined for the ECU in these OEM specifications. To fulfill these conditions:
 - Electrical cables and connectors shall be characterized and qualified to comply with the appropriate OEM specifications.
 - MNCs, BTR, EBC and BEC shall be characterized and qualified according to the AEC-Q100 requirements.
 - MOST interfaces shall utilize an EMC optimized design

Other functional requirements that must be considered:

- The BTR, EBC and BEC shall operate in an ambient environment with an operating temperature range of $T_A = -40^{\circ}C$ to $+105^{\circ}C$.

9 Electrical Interfaces

9.1 Bit Rate and Frequency Tolerance

Specifications for the operating bit rates are shown in Table 9-1. Each MOST50 automotive node requires a local frequency reference. Manufacturable frequency references operate at some frequency offset tolerance around the nominal F_s (48 kHz). System interoperation relies on these offsets being minimized. The Time Base Deviation, Δ_{FS} , is this offset and is measured in parts per million (ppm).

Bit Rate and Frequency Tolerance Parameters	Symbol	Min.	Typ.	Max.	Unit
Time Base Deviation	Δ_{FS}	-200	0	+200	ppm
Bit Rate for 48.0 kHz frame rate	BR_{48}	49.14217	-	49.16183	Mbit/s

Table 9-1: Bit Rate and Frequency Tolerance

The nominal Bit Rate is obtained by multiplying the frame rate by 1024. The minimum values are obtained by taking the nominal frame rates and subtracting the time base deviation. The maximum values are obtained by taking the nominal frame rates and adding the time base deviation.

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