

MOST

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST150 oPHY Automotive Physical Layer
Sub-Specification Rev. 1.1**

Errata 2

Rev. 1.1E2

12/2012

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Bibliography

Number	Document	Revision
[1]	MOST150 oPhy Automotive Sub-Specification [MOST150]	Rev. 1.1
[2]	MOST Specification	Rev. 3.0
[3]	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits (TIA/EIA-644-A-2001)	

Table 1-1 Bibliography

Document History

Changes

Change Ref.	Section	Changes
1V1-00	2	First Issue
1V1-01	2	Modify chapter 9.12 LVDS

1 Introduction

This document is a supplement to the MOST150 oPhy Automotive Sub-Specification Rev. 1.1 [1].

2 Errata

Legend: → means “will be substituted by”

1.)

Section 7.3.2 OEC Requirements,
Table 7-3: OEC Power State Requirements

OEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in the <i>Off-State</i>	I _{CCSLEEP}		-	-	30	μA

→

OEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in the <i>Off-State</i>	I _{CCSLEEP}	-40°C...70°C 70°C...95°C	-	-	30 45	μA

2.)

Specification of a further exception for the requested compliance to the referenced LVDS-standard in section 9.1.

9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. One exception is listed in Table 9-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for wiring harness. All electrical signals must maintain the correct polarity from OEC to NIC and from NIC to EOC

Exception regarding LVDS [3]	Symbol	Condition	Min.	Max.	Unit
Common-mode Input Voltage range	V_{CM}		0.05	$V_{cctx} - 1.2V$	V

Table 9-1: Exception regarding LVDS [3]

→

9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. Exceptions are listed in Table 9-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for wiring harness. All electrical signals must maintain the correct polarity from OEC to NIC and from NIC to EOC.

Exception regarding LVDS [3]	Symbol	Condition	Min.	Max.	Unit
Common-mode Input Voltage range	V_{CM}		0.05	$V_{cctx} - 1.2V$	V
Combined impedance of receiver loads connected to the bus	R_{CRL}	1), 2)		30	kOhm
Notes:					
1) The 30 kOhm resistors represent the combined impedance of 4 receiver loads connected to the bus					
2) Refers to chapter 4.1.1 "Full Load Measurements" in [3]					

Table 9-1: Exception regarding LVDS [3]

Notes: