

MOST[®]

Media Oriented Systems Transport

Multimedia and Control
Networking Technology

**MOST150 cPHY Automotive Physical Layer
Sub-Specification**

**Rev. 1.1
04/2015**

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See page 3 for the terms of disclosure



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1 References

Number	Document
[1]	MOST Specification Rev 3.0
[2]	MOST Physical Layer Basic Specification Rev. 1.0
[3]	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits (TIA/EIA-644-A-2001)
[4]	Interface Standard for Nominal 3 V / 3.3 V Supply Digital Integrated Circuits (JEDEC No. JESD8C.01)
[5]	Road vehicles -- 50 ohms impedance radio frequency connection system interface (ISO 20860-1:2008)
[6]	EN 50289-1-11:2002 Communication cables - Specifications for test methods - Part 1-11: Electrical test methods; Characteristic impedance, input impedance, return loss.

Table 1-1: References

2 Document History

Revision 1.1

Revision	Changes
1.0	First Issue
1.1	Revised version

3 Terminology and Abbreviations

BPF: Bits Per Frame

BER: Bit Error Rate

CEC: Coaxial to Electrical Converter

CTR: Coaxial Transceiver

DC Adaptive Coding (DCA): coding method used for MOST150 cPHY Automotive network

DC: Direct Current, referring to a steady state signal

Digital Sum Value (DSV): accumulated DC offset contained in the data

ECU: electronic control unit

ECC: electrical to coaxial converter

Frequency Reference: A device, usually crystal controlled, which provides an accurate and low drift frequency standard for the NIC and network timing

LVDS: Low Voltage Differential Signal

Network Frame Rate (Fs): The frequency at which frames are started on the MOST150 cPHY Automotive network

NIC: network interface controller

OEM: Original Equipment Manufacturer

PCB: Printed Circuit Board

PLL: phase locked loop

RL: Return Loss

RMS: root mean square

RX Data: MOST150 cPHY Automotive encoded digital bitstream being received

SMB: SubMiniature version B (type of coaxial connector)

SP1...4: Specification Points 1 to 4

TDR: Time Domain Reflectometry

TX Data: MOST150 cPHY Automotive encoded digital bitstream being transmitted

UI: unit interval (see Section 4.2.2)

This sub-specification references additional terms in [2]. Abbreviations that are defined in that specification are also valid here.

3.1 Usage of Expressions

The following table covers usage of expressions:

Expression	Meaning
Shall	Mandatory provision to maintain compliance.
Must	
Shall Not	Prohibition whose violation results in non-compliance
Must Not	
Should	Recommended but not mandatory.
May	Feature might or might not be present, at the option of the implementer, and has no effect on compliance.
Can	

Table 3-1: Meanings of Expressions

3.2 Resolution of Conflicts

If there are any conflicts between the textual information presented in this document and the corresponding figures, the text shall have priority in resolving the conflict.

3.3 Logic Terminology

The following tables serve to clarify the electrical logic descriptions used in this specification.

3.3.1 Single-Ended Low Voltage Digital Signals

The following table relates the words used in this document to the parameters defined in the JEDEC specification [4]. These words are used to describe the logic states of signals **/RST** and **STATUS**.

Expression	Corresponding JEDEC Parameter
Low	V_{OL}
Logic 0	
0	
Zero	
High	V_{OH}
Logic 1	
1	
One	

Table 3-2: Meaning of Logic Expressions for Single-Ended Signals

3.3.2 Differential LVDS Signals

This document does not precisely follow the conventions shown in the TIA/EIA specification [3] because that document labels device output terminals A and B while this specification uses a P and an N to denote the two terminals of the LVDS signal. The following table explains the expressions used to describe the logic states of the LVDS signals and follows the intent of the wording in the TIA/EIA specification.

Expression	Corresponding TIA/EIA Description
Low	The P terminal shall be negative with respect to the N terminal for a binary 0 state.
Logic 0	
0	
Zero	
High	The P terminal shall be positive with respect to the N terminal for a binary 1 state.
Logic 1	
1	
One	

Table 3-3: Meaning of Logic Expressions for LVDS Signals

The paired P and N LVDS signals are called a bus. The TIA/EIA specification only defines logic levels for a two-state bus. Since some of the devices specified in this document use a tri-state LVDS interface, the following table defines some additional expressions:

Expression	Corresponding Description
Disabled	The P and N terminals are in a high impedance state. Small leakage currents may exist which can cause an indeterminate voltage on the line/load.
Off	
Enabled	Both the P and the N terminals are driving the line/load. The outputs shall be at valid LVDS logic levels provided the input data is valid.
On	
Valid LVDS Signal	Toggling data or a Zero with LVDS voltage levels.

Table 3-4: Meaning of Expressions for LVDS Bus States

4 General Network Parameters

4.1 Overview

This document describes the physical parameters and limits required to guarantee operation of the MOST150 Coaxial Phy (cPHY) Automotive network. This sub-specification is electrical physical layer specification and references terms and measurement methods defined in [2].

4.2 Network Coding

The following sections describe a technique of encoding digital data called DCA coding. This information is presented in order to assure a better understanding of the network but DCA coding is not a part of the physical layer specification [2].

4.2.1 Pulse Characteristics

MOST150 traffic is scrambled and encoded using DCA coding, resulting in a data-stream that contains timing information and is DC free. Data pulses range from 2 UI to 6 UI yielding 5 different pulse widths, as shown in Figure 4-1.

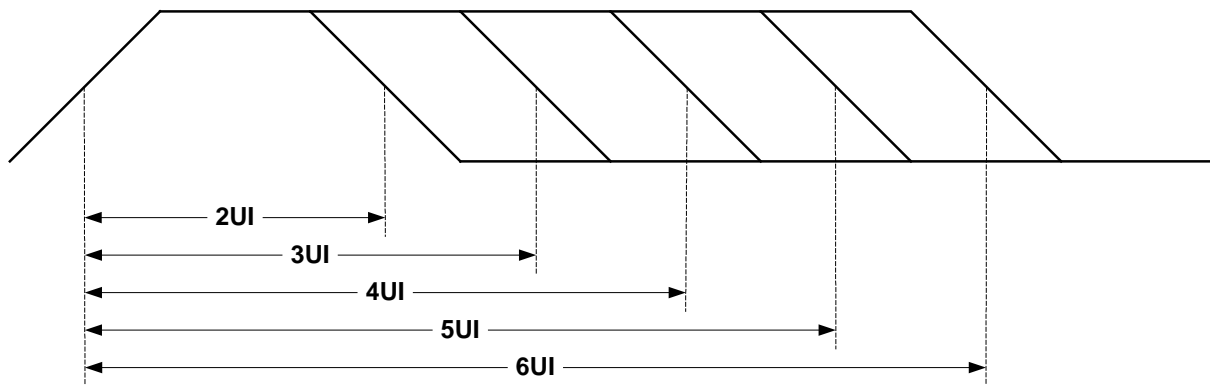


Figure 4-1: Allowable Pulse Widths When Using DCA Coding

4.2.2 Unit Interval Definition

The UI width calculation is shown in the following Equation 4-1.

$$UI = \frac{1}{F_s * 2 * BPF}$$

Equation 4-1: Unit Interval Calculation

For MOST150, there are 3072 Bits Per Frame (BPF). Using the above formula for a frame rate of 48.000 kHz will result in a Unit Interval of 3.391 ns. A frame rate of 44.100 kHz will have a Unit Interval of 3.691 ns.

4.2.3 DC Balance

DCA coding is inherently DC-free. However, short term imbalances in offset are required for data transmission. These imbalances are tracked with a running total called the Digital Sum Value (DSV). The DSV is calculated by incrementing the sum for every UI where the data is high, and decrementing the sum for every UI where the data is low. The calculation for DSV is illustrated in Figure 4-2.

Dynamic properties of DCA coding:

- The DSV is periodically driven to zero at least once per frame.
- The range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5}.
- The shortest DCA period is 4 UI.
- The longest DCA period is 10 UI.
- The data stream is guaranteed to have a period of 10 UI at least once per frame.
 - These 10 UI periods can either be made of pulses that are 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

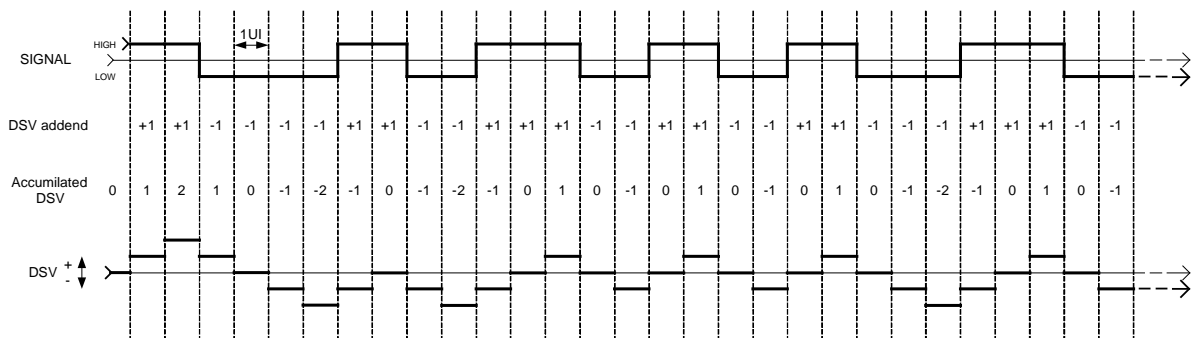


Figure 4-2: DSV Calculation

4.3 Link and interconnect type

The cPHY specification defines a 50 Ω end-terminated interconnect consisting of automotive grade coaxial cables and connectors. Depending on the specific application, there are two interconnect types:

- Simplex (unidirectional) interconnect – The transmit and receive links are separate and unidirectional using two separate ports (device connectors) and cables.
- Duplex (bidirectional) interconnect – The transmit and receive links share the same cable using one port (device connector). Communication is full-duplex. A Coaxial Transceiver (CTR - combination of an ECC and a CEC) is responsible for separating the transmit and receive signal components.

Three connector port types are defined:

- Transmit port (of a Simplex Interconnect)
- Receive port (of a Simplex Interconnect)
- Bi-directional port (of a Duplex Interconnect)

These ports shall be uniquely encoded to prevent accidental misconnections being made. All connectors must conform to the electrical specifications as defined in Section 6.3. See Appendix A for mechanical information and connector keying.

4.4 Specification Point Details

Specification point locations and details are shown in the following table and figures.

Specification Point	Location	Electrical Interface
SP1	ECC electrical input pins at LVDS termination	LVDS
SP2	Signal at transmit port of Coaxial interface	Analog
SP3	Signal at receive port of Coaxial interface	Analog
SP4	CEC electrical output pins at LVDS termination	LVDS

Notes: For special cases see Appendix B.

Table 4-1: Specification Point Locations and Interfaces

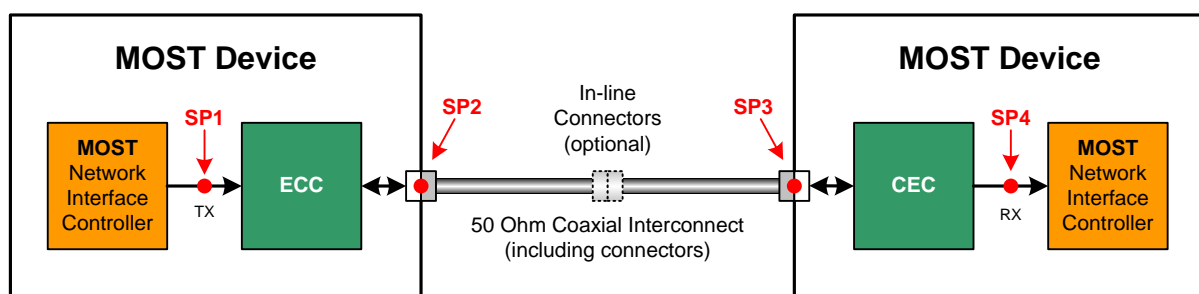


Figure 4-3: Specification Point Locations for Simplex Interconnect

Viewed from one node, a duplex interconnect consists of two links – one transmit, (or forward) and one receive (or reverse). In the duplex scenario, the two links must be considered independently. Figure 4-4 illustrates a duplex interconnect. Points SP1, SP2, SP3 and SP4 indicate the forward signal path. Points SP1*, SP2*, SP3* and SP4* indicate the reverse signal path. Note, the reverse path uses the asterisk notation only for clarity of discussion. The forward and reverse measurements and requirements are the same, but performed independently. A method to separate the forward and reverse components must be utilized when measuring duplex interconnects.

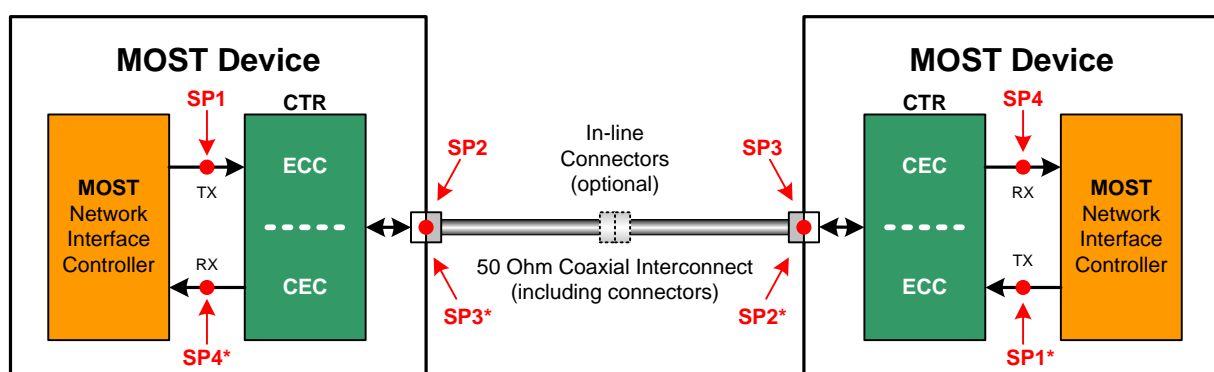


Figure 4-4: Specification Point Locations for Duplex Interconnect

4.4.1 Analog Frontend

Suppliers of Coaxial Transceivers will provide a connection scheme, defining requirements on connection and layout of the Transceivers with Coaxial connector, this may include passive components. The section between Transceiver Pins and coaxial connector is called Analog Frontend (AFE). Performance criteria for SP2 include ECC and analog Frontend. SP3 defines the Signal characteristic after passing the coaxial interconnect. Analog Frontend and CEC are relevant for SP4.

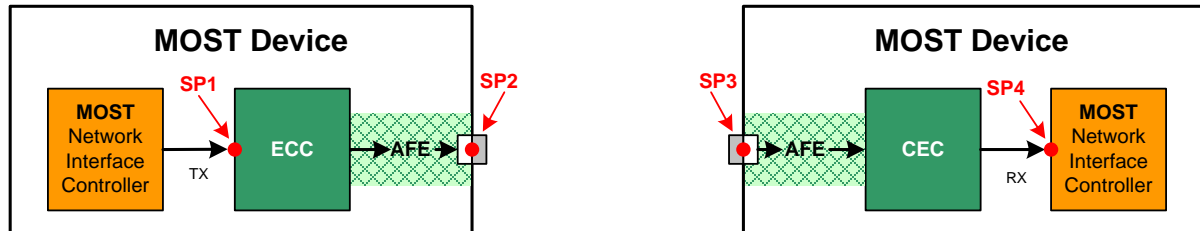


Figure 4-5: Analog Frontend

4.4.2 Integration of Coaxial Transceiver

Coaxial Transceivers may be realized as separate standalone components, Connections between Coaxial Transceiver and Network Interface Controller then are formed as traces on the PCB (e.g. SP1, SP4). This configuration allows usage of Coaxial Transceivers and Network Interface Controllers from different suppliers. For such configurations, the specification for SP1 and SP4 defines the relevant interfaces requirements, which need to be guaranteed by the component suppliers as well as by the instance, creating application.

For optimization of infrastructure Coaxial Transceiver may also be integrated in the Network Interface controller. Inside the chip, the Coaxial Transceiver portion will be connected with the Network Interface section. In consequence, there is no external SP1 and SP4. Suppliers of such integrated versions are solely responsible for their inherent SP1-/SP4-performance. From a standardization point of view, relevant interfaces for integrated Coaxial Transceivers are SP2 and SP3 only.

Specification Point	Location	Electrical Interface
SP2	Signal at transmit port of Coaxial interface	Analog
SP3	Signal at receive port of Coaxial interface	Analog
Notes: For special cases see Appendix B.		

Table 4-2: Specification Point Locations and Interfaces for integrated Coaxial Transceivers

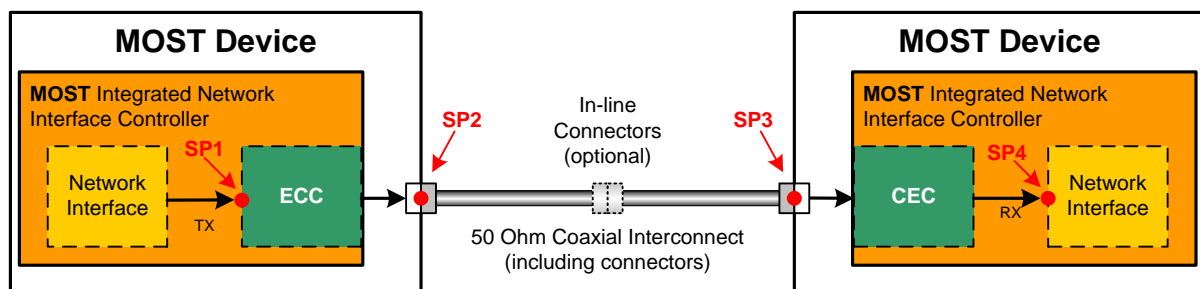


Figure 4-6: Specification Point Locations for Simplex Interconnect with integrated Coaxial Transceivers

Integration of Coaxial Transceivers may also exist for duplex scenarios.

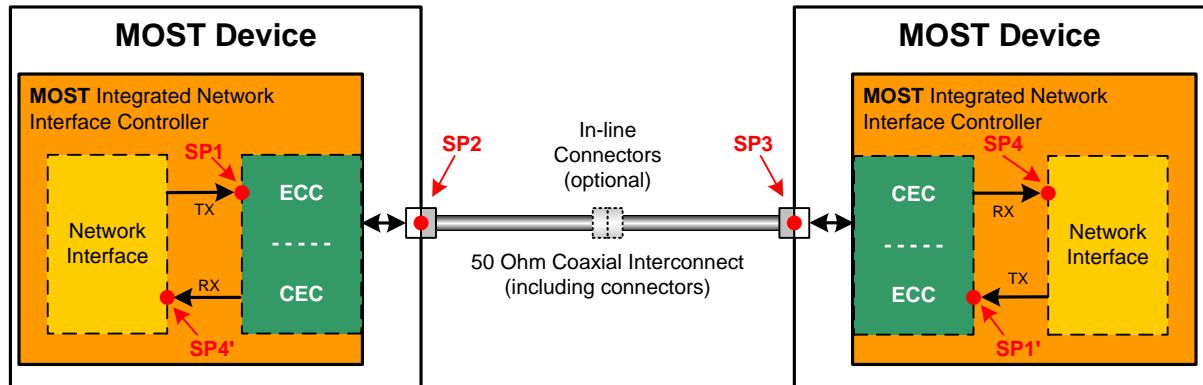


Figure 4-7: Specification Point Locations for Duplex Interconnect with integrated Coaxial Transceivers

5 Models and Measurement Methods

The following models and methods are used as the basis for measurements in this sub-specification.

5.1 Golden PLL

The golden PLL describes the required worst-case jitter performance of a NIC, and is used to form receiver eye-diagrams. The golden PLL must reference to the positive edge of the signal. The transfer function is a low pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above.

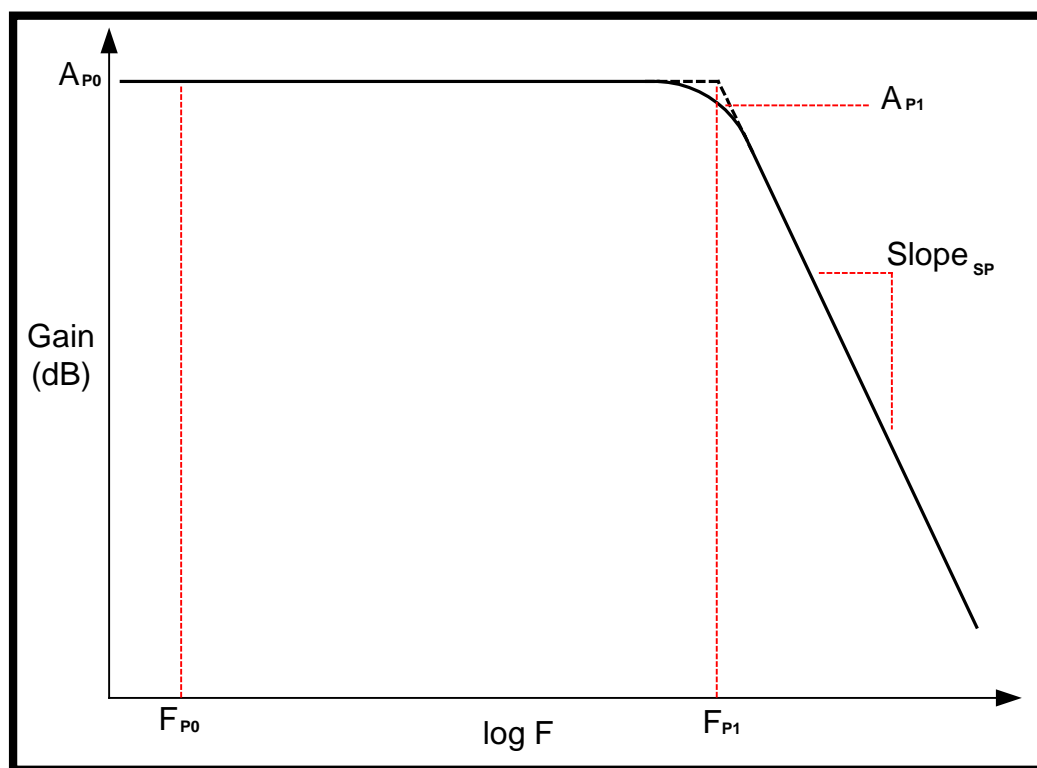


Figure 5-1: Golden PLL Transfer Function

Parameter	Value	Unit
A_{P0}	0	dB
F_{P0}	10	Hz
A_{P1}	-3	dB
F_{P1}	125	kHz
$Slope_{SP}$	-20	dB/dec

Table 5-1: Golden PLL Specifications

5.2 Jitter Filter

The jitter filter describes the worst-case jitter transfer function of a NIC, and is used to calculate transferred jitter along the link. The transfer function is a low pass filter with unity gain at DC, but for practicality of measurements is specified for 10 Hz and above.

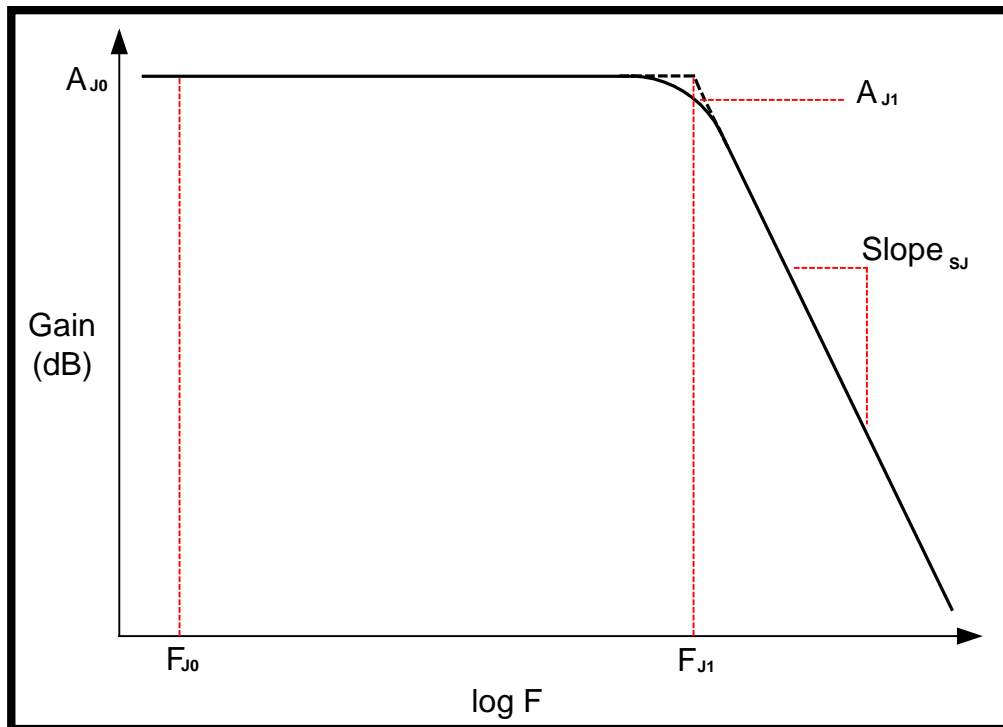


Figure 5-2: Jitter Filter Response

Parameter	Value	Unit
A_{J0}	0	dB
F_{J0}	10	Hz
A_{J1}	-3	dB
F_{J1}	200	kHz
Slope_{SJ}	-20	dB/dec

Table 5-2: Jitter Filter Specifications

5.3 Test Pattern

The MOST150 Test Pattern shall be used for the following measurements:

- Signal level detection measurements
- All eye-diagrams

Description Code	File Name
MOST150 Test Pattern	<i>MOST150_Stress_Pattern-1v0.pat</i>
	Files are available on www.mostcooperation.com

Table 5-3: Description of MOST150 Test Pattern

6 Link Specifications

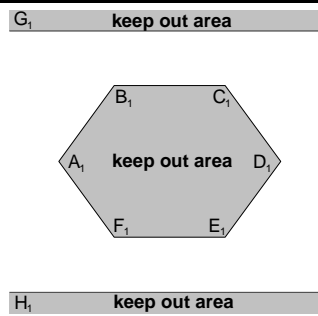
This specification utilizes eye pattern diagrams and mask templates to validate the serial data link. A high-quality signal with low jitter and distortion will show a large eye opening, which can be compared to a standardized mask (a hexagon shape) placed in the center of the eye. The mask is designed such that a good signal will not touch the mask at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitude, jitter, or pulse width variations will show up as closure in the eye diagram. Signals with excessively high amplitude will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.

All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9} . Consequently, all of the mask violation parameters have been specified with that goal in mind.

6.1 Specification Point SP1

The signal at SP1 must meet the requirements in Table 6-1 and must not touch the “keep-out” areas of the mask. Refer to Sections 7.1, 8.3, and 9 for operating conditions and interface standards.

SP1 Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Transferred jitter	J_{tr1}	1)	-	-	50	ps RMS
Eye-mask	$A_1 \dots H_1$	2), 3)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)	Eye-mask
A_1	0	0.075	
B_1	100	0.325	
C_1	100	0.675	
D_1	0	0.925	
E_1	-100	0.675	
F_1	-100	0.325	
G_1	636	-	
H_1	-636	-	

Notes:

- 1) Using the jitter filter specified in Section 5.2.
- 2) Using the Golden PLL specified in Section 5.1.
- 3) The signal must comply with the minimum input signal amplitude (see Section 9.1).

Table 6-1: Link Quality Parameters of SP1

6.2 Specification Point SP2

The signal at SP2 must meet the requirements in Table 6-2 and must not touch the “keep-out” area of the mask. Refer to Sections 7.1, 8.3, and 9 for operating conditions and interface standards.

The signal at SP2 is an AC waveform and may be accompanied by a DC offset, especially when transporting power along with the data over the coaxial interconnect. In this instance the DC level shall be removed before evaluating the signal. Table 6-2 is written assuming the DC value is 0 V.

SP2 Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Rise time	t_{r2}	20% - 80%	700	-	1400	ps
Fall time	t_{f2}	80% - 20%	700	-	1400	ps
Transferred jitter	J_{tr2}	1)	-	-	112	ps RMS
Steady-state amplitude	V_{ss2}	4)	300	-	420	mV
Eye-mask	$A_2 \dots H_2$	2), 3), 5)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)	Eye-mask
A_2	0	0.150	
B_2	125	0.400	
C_2	125	0.600	
D_2	0	0.850	
E_2	-125	0.600	
F_2	-125	0.400	
G_2	235	-	
H_2	-235	-	

Notes:

- 1) Using the jitter filter specified in Section 5.2.
- 2) Using the golden PLL specified in Section 5.1.
- 3) The DC offset is removed.
- 4) Difference between high-state and low-state of bimodal waveform.
- 5) The mask Amplitude parameters include tolerances for overshoot and ringing.

Table 6-2: Link Quality Parameters of SP2

6.3 Coaxial Link Requirements

The transmission media is a prominent factor for setting the parameters of a physical layer. MOST150 cPhy specification defines the usage of 50 Ohm coaxial cable and connectors. Between SP2 and SP3 there can be a single coaxial cable or a series of coaxial cables including inline connectors and device connectors. Together they form the coaxial interconnect.

Following the signal path beyond SP2 and SP3, there are additional portions of the signal channel realized on the PCB. These PCB Interface sections shall also form a 50Ohm system and adapt with minimum discontinuities to the coaxial Interconnect.

The coaxial interconnect shall comply with the requirements defined in Sections 6.3.1. and 6.3.2.1.
The PCB Interfaces shall comply with the requirements defined in Section 6.3.2.2.

The relevant frequency range for MOST150 data over coaxial interconnect is defined as 1MHz to 450 MHz. The upper corner is constrained by the bandwidth and the minimum rise and fall time of the transmitted signal.

6.3.1 Coaxial Interconnect, Length and Attenuation

The coaxial interconnect parameter requirements are the same for both Simplex and Duplex interconnects. The maximum coaxial interconnect length is given in Table 6-3. This length includes the coaxial cables and the connectors (device and in-line). A limitation on the number of in-line connectors is not required as long as the whole interconnect conforms to the specifications given in Table 6-3.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Coaxial interconnect length	L_{ci}	1)	0	-	15	m
DC loss	DC_{loss}	1)	0		0.5	dB
Skin-effect loss	F_{skin}	1)	9.2×10^6		∞	Hz/dB ²
Attenuation conformance	A_C	F = 1 MHz – 450 MHz 1)	-1	-	1	dB
Notes: 1) Parameter variations due to environmental conditions or mechanical stress being applied to the coaxial interconnect shall be considered						

Table 6-3: Coaxial Interconnect Attenuation Parameters

For Signal Integrity, the following loss parameters for coaxial cable and connector must be considered:

- Connector insertion loss
- DC resistance loss
- Skin effect loss
- Dielectric loss

In the MOST150 frequency range of interest, dielectric and connector insertion losses (e.g. according to [5]) are negligible. Therefore, it is sufficient to consider only DC resistance and skin effect losses of the coaxial cable as coaxial interconnect attenuation sources.

The amount of attenuation is mainly dependent on the length of the coaxial interconnect. For any given Interconnect length and for any combination of cable segments and couplers in an Interconnect, the DC resistance and skin effect losses will have unique values.

For the MOST150 frequency range of interest, the theoretical transfer function of the coaxial interconnects can be expressed with the following equation:

$$H_{theo}(f) = 10^{-\left(\frac{dc_{loss} + \sqrt{\frac{f}{f_{skin}}}}{20}\right)l} e^{-i\left(\frac{lpd*f + \sqrt{\frac{f}{f_{skin}}}}{20 \log_{10}(e)}\right)l}$$

Equation 6-1: Complex coaxial cable transfer function versus frequency

The complex equation exists of 2 terms, both of them are cable-length dependent (l). The first term of the complex equation represents the frequency dependent attenuation in [ratio/m], while the second term describes the phase over frequency in [rad/m].

The characteristic Interconnect coefficients in this equation are related to length:

dc_{loss}	represents the DC Attenuation
f_{skin}	represents skin effect losses and also contributes into the phase term
lpd	stands for linear phase delay and represents a constant propagation delay

The receiver circuitry in the CEC must include an equalizer designed to compensate for attenuation. Variations in the coaxial interconnect characteristics which do not follow the theoretical transfer function above cannot be compensated for and will degrade the CEC output signal. Therefore, the attenuation characteristic of a coaxial interconnect has to closely resemble that of an ideal coaxial cable.

The Interconnect Attenuation Parameters, given in Table 6-3 are focusing on Attenuation only. Attenuation in dB-scale, is given by the first term of the transfer function. For a Coaxial Interconnect of length l (within L_{ci}) Attenuation can be expressed with:

$$Attenuation(f) = -DC_{loss} - \sqrt{\frac{f}{F_{skin}}}$$

Equation 6-2: Attenuation versus frequency (in dB)

The resulting values of the parameters **DC_{loss}** and **F_{skin}** for a particular Interconnect of length l are unique for exactly this configuration of cables. The resulting parameter values inherently consider the length of the particular Interconnect. The parameters are derived from measured transfer characteristic (attenuation over frequency). The numerical values then are determined using analytic or experimental (e.g. curve fitting) approaches, for description and an example see Appendix C. The resulting values for **DC_{loss}** and **F_{skin}** must meet the ranges given in Table 6-3.

To put constraints on the coaxial interconnect variations, this specification defines the following parameter: Attenuation conformance (A_C). A_C , as shown in Figure 6-1, specifies the maximum deviation from the theoretical cable transfer function (Equation 6-1) for a given set of DC resistance and skin effect losses (as defined by the interconnect length and quality). The coaxial interconnect attenuation shall always fit within the boundaries defined by the minimum and maximum values of parameter A_C .

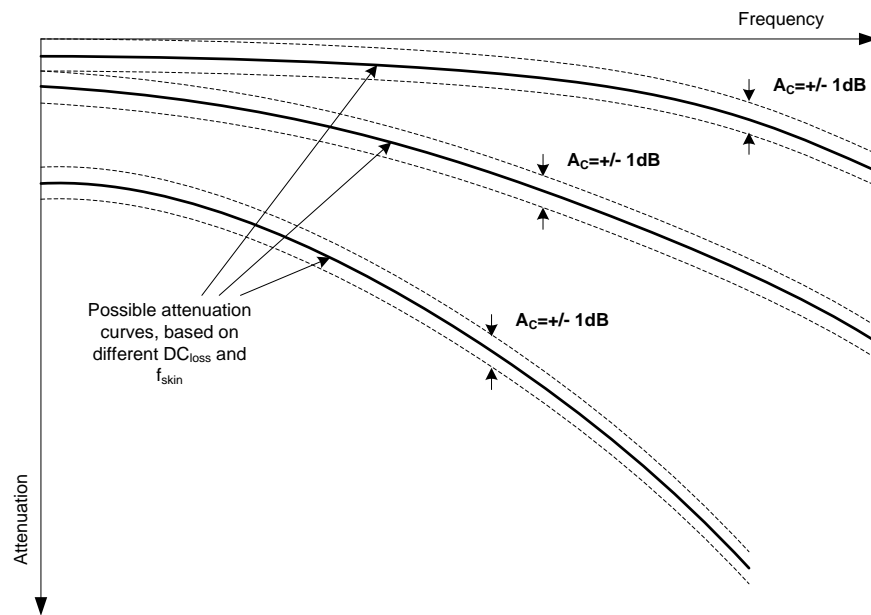


Figure 6-1: Attenuation Conformance Curves

Equation 6-1 allows to calculate the temporal impulse response, taking into consideration also the phase of the signal. f_{skin} being infinite and DC_{loss} being zero, corresponds to a transfer function of zero length cable. Finite f_{skin} and non-zero DC_{loss} corresponds to a coaxial cable with a non-zero length.

1)

6.3.2 Characteristic impedance and Return Loss

This section defines requirements for characteristic impedance of components forming a coaxial link. Impedance mismatches causes back reflection of a certain portion of the signal energy. The ratio of reflected Signal relative to transmitted Signal is expressed Return Loss. The definition of Characteristic Impedance is either given as Impedance [Ohm] or as Return Loss [dB], whatever is better suited for component.

On a communication link, Return Loss has different importance for SIMPLEX and DUPLEX operation.

In SIMPLEX operation, Return Loss on a transmit path means a minor reduction of signal amplitude in transmit direction. Such losses are already included in

- SP2 output signal specification
(this covers amplitude reduction due to Return Losses inside the ECU)
- Attenuation requirements (Table 6-3) for coaxial Interconnects
(measurement of Attenuation inherently includes losses due to RL).

Not covered are losses due to impedance mismatches at SP3, between coaxial Interconnect and the PCB-Interface.

Crosstalk, as another possible form of signal degradation, in SIMPLEX would require double reflections, which is negligible within given limits.

For DUPLEX, Return Loss causes a minor reduction of signal amplitude in transmit direction. More important here is added noise due to reflections. Signal edges generated on an ECC of a node will trigger reflections when passing impedance mismatches. Multiple mismatches along that link cause multiple Reflections which will overlay with each other. Such Reflections will overlay as crosstalk with the signal on the receive path, being sent from the opposite node. Therefore the accumulation of relevant Return Loss contributions along a link forms a crosstalk-signal which compromises the data signal being sent to that node. Cable attenuation will reduce amplitude of reflections. For DUPLEX links, calculation of minimum CEC-input Signal-quality must consider losses along the coaxial interconnect as well as added crosstalk.

The mismatch of a load Impedance Z_L to a source Impedance Z_S results in a reflection coefficient $T = (Z_L - Z_S) / (Z_L + Z_S)$. The impedances can be complex, the magnitude of the reflection coefficient is given by: $p = \text{mag}(T)$. Return Loss can be expressed by $RL = -20 * \log_{10}(p)$.

In this Specification, Return Loss limits are given in the frequency range of 1 MHz to 450 MHz.

The worst case accumulation of Return Losses for impedance mismatches a, b, etc.:

$$RL_{acc} = -20 * \log_{10}(10^{(-RL_a/20)} + 10^{(-RL_b/20)} + \dots)$$

Equation 6-3: Accumulation of Return Loss (in dB)

6.3.2.1 Coaxial Interconnect, Characteristic impedance and Return Loss

Coaxial cables and connectors shall have characteristic impedance as given in Table 6-4
The end-to-end (SP2 to SP3) coaxial interconnect shall have a Return Loss as specified in Table 6-4.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Return Loss of Harness-connectors and inline connectors	RL _{con}	f=1 MHz–450 MHz 1), 2), 5), 6)			-15.6	dB
Return Loss of coaxial Interconnect	RL _{Intercon}	f=1 MHz–450 MHz 1), 3), 4), 5), 6)	-	-	-20	dB
Characteristic impedance of coaxial cable	Z _{0cable}	1), 2), 4), 7)	47	50	53	Ω
Notes: 1) Parameter variations, due to environmental conditions or mechanical stress shall be considered. Refer to Sections 7.1, 8.3 for operating conditions. 2) For Simplex and Duplex. 3) For Duplex only. 4) Relevant for accumulated Return Loss. 5) Measured using rise _{TDR} = 400 ps. 6) Nominal Characteristic Impedance 50 Ohm. 7) See [6].						

Table 6-4: Coaxial Interconnect Characteristic Impedance and Return Loss Parameters

For DUPLEX, the maximum number of cable segments within a coaxial Interconnect is limited by the deviation of the cable pieces from the nominal characteristic Impedance. The summation of mismatches in an Interconnect shall result in a Return Loss, equal or less than specified for RL_{Intercon}.

6.3.2.2 PCB Interfaces, Characteristic impedance and Return Loss

Signals going to or coming from coaxial interconnect are electrically connected to the coaxial Transceivers on the PCB. Specification of SP2 already includes ECC output characteristic and potential losses due to board traces, passive components and board connector. SP3 represents Signal characteristic at the end of a coaxial interconnect, terminated with ideally 50Ohm. Potential signal degradation due to board traces, passive components and board connector between SP3 and CEC-input have to be additionally considered. The entity of board traces, passive components and board connector is summarized under the term analog front end AFE. In some cases the length of the electrical connection between device connector and the CEC/ECC could be long enough to adversely affect the signal integrity.

Table 6-5 describes the requirements for PCB Interfaces connected to SP2 and SP3.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Return Loss of ECU connector	RL _{con}	f=1 MHz–450 MHz 1), 2), 3), 5), 6)			-15.6	dB
For SIMPLEX: Return loss of ECU-Interface, measured at device connector	RL _{SP2} RL _{SP3}	- A, B, C, D 1), 2), 5), 6)			- ≤ Limit Line	
For DUPLEX: Return loss of ECU-Interface, measured at device connector	RL _{SP2_SP3}	A, B, C, D 1), 3), 4), 5), 6)			≤ Limit Line	

	Frequency	Return Loss	Limit Line
A	1 MHz	-5 dB	
B	10 MHz	-22 dB	
C	100 MHz	-22 dB	
D	450 MHz	-10 dB	

Notes:

- 1) Parameter variations, due to environmental conditions or mechanical stress shall be considered. Refer to Sections 7.1, 8.3 for operating conditions.
- 2) For Simplex.
- 3) For Duplex.
- 4) Relevant for accumulated Return Loss.
- 5) Measured using rise_{TDR} = 400 ps.
- 6) Nominal Characteristic Impedance 50 Ohm.

Table 6-5: PCB-Interface Impedance and Return Loss Parameters

6.4 Specification Point SP3

The variations in the signal integrity at SP3 are mainly constrained by the definitions of SP2 link quality (Section 6.2) and the coaxial interconnect attenuation requirements (Section 6.3.1). Stimuli for SP3 can be calculated by filtering a signal representing a SP2 corner condition (minimum/maximum amplitude V_{ss2} , minimum/maximum rise/fall time, etc.) using a filter with a transfer function given by Equation 6-1. The transfer function parameters DC_{loss} and F_{skin} shall be within the allowed range as specified in Table 6-3.

Further Signal degradation at SP3 may occur due to amplitude noise coupled on the data-Signal along the link. Amplitude noise reduces signal-to-noise ratio and may also cause jitter on the signal. Potential noise sources in general are EMC, Crosstalk from neighboring signals and reflections. Reflections are caused by Impedance mismatches on the transmit link and can be controlled by constraining component performances. Potential deterioration by EMC and Crosstalk from neighboring signals is not subject of this specification.

For SIMPLEX Transmission, only double reflections would be relevant for a noise budget on SP3. Due to the given specifications on Impedance and Return Loss (section 6.3.2.1 and 6.3.2.2) this contribution can be neglected.

For DUPLEX Transmission, impedance mismatches may cause relevant reflections. Transitions of a downstream signal will trigger reflections, which will accumulate over a link and add to the upstream data signal. A limitation for signal-to-noise ratio is inherently given by the specification of components Return Loss (see 6.3.2.1 and 6.3.2.2), the definition of accumulation of relevant Return Loss (see Equation 6-3), and by the specification of maximum attenuation (see 6.3.1).

6.5 Specification Point SP4

The signal at SP4 must meet the requirements in Table 6-6 and must not touch the “keep-out” areas of the mask. Refer to Sections 7.1, 8.3, and 9 for operating conditions and interface standards.

SP4 Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transferred jitter	J_{tr4}	1)	-	-	230	ps RMS
Eye-mask	$A_4 \dots H_4$	2), 3), 4)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)	Eye-mask
A_4	0	0.275	
B_4	148	0.425	
C_4	148	0.575	
D_4	0	0.725	
E_4	-148	0.575	
F_4	-148	0.425	
G_4	636	-	
H_4	-636	-	

Notes:

- 1) Using the jitter filter specified in Section 5.2.
- 2) Using the Golden PLL specified in Section 5.1.
- 3) The mask parameters include tolerances for overshoot and ringing.
- 4) The steady-state differential voltage must not be less than that specified in [3].

Table 6-6: Link Quality Parameters of SP4

7 Power Up / Power Down

7.1 ECU Requirements

The ECU must provide the following: a stable frequency reference for the NIC; power supply for the NIC, ECC and CEC; and power supply monitoring circuitry.

- Frequency reference:
The frequency reference is typically a crystal controlled oscillator or derivative. The required accuracy is specified in Section 9.2.
- Power supply:
 - Continuous Power Supply: V_{CCCN} , with a nominal operating range of $3.3V \pm 5\%$, which shall always be supplied. This power supply is used to power CEC (or CTR, see Section 7.3.1).
 - Switched Power Supply: V_{CCSW} , with a nominal operating range of $3.3V \pm 5\%$, which must be able to be turn off. This power supply is used to power NIC and ECC (or CTR, see Section 7.3.1).
- Power supply monitoring circuitry:
The ECU shall provide power supply monitoring circuitry, as specified in Section 7.2 for supervising the switched power supply V_{CCSW} . The ECU shall connect the active-low reset signal $/RST$ provided by the power supply monitoring circuitry to the $/RST$ inputs of the ECC (CTR) and the NIC.
In case CTR is powered by V_{CCCN} only (see Section 7.3.1), ECU design must ensure the $/RST$ signal voltage must always stay below V_{CCSW} .

7.2 Power Supply Monitoring Circuitry

The power supply monitoring circuitry shall:

- Provide an active-low reset signal $/RST$, which is valid LVTTTL (JESD8C) signal over the power supply range V_{VALID} , as specified in Table 7-1.
- Set the $/RST$ signal high when the V_{CCSW} ramps above the threshold, V_T . Switching from low to high shall be delayed by a minimum time of t_{D+} to allow the circuitry in the ECC to stabilize, the LVDS pins of the NIC to be driven, and the local frequency reference to stabilize. Although a maximum time for t_{D+} is not specified, an implicit maximum value exists due to the required start-up time. Refer to the MOST Specification [1] for more details.
- Set the $/RST$ signal to low, when the V_{CCSW} voltage drops below the threshold V_T . Switching from high to low shall occur within a time of t_{D-} .

$/RST$ Signal	Symbol	Condition	Min	Max	Unit
Supply range for valid logic levels	V_{VALID}		1	3.465	V
Logic switching threshold	V_T		2.970	-	V
Logic 0 to 1 Time Delay	t_{D+}		1	-	ms
Logic 1 to 0 Time Delay	t_{D-}		0	100	μs

Table 7-1: Specifications for $/RST$ Signal Generation

7.3 Coaxial Transceiver, ECC and CEC

System wakeup and shutdown methods require certain functionality to be built into the ECC and CEC sub-sections of a coaxial transceiver.

7.3.1 CTR Requirements

In case a CTR has only one power domain (common power supply for ECC and CEC sub-sections) it must:

- fulfill $I_{ccsleep}$ requirements defined in Table 7-3 during *Off-State with /RST input driven low* and
- fulfill all the requirements for ECC and CEC, where all power supply related parameters (V_{ECCOR} , V_{ECCGR} , V_{ECCOFF} , V_{CECOR}) are referred to the actual CTR power supply used.

7.3.2 ECC Requirements

The ECC functional requirements are listed below.

- a) The ECC must have an LVTTTL (JESD8C) active low reset input pin (**/RST**).
- b) The ECC must be capable of performing transition detection at its input. Transition detection is the ability to monitor the input frequency of the signal at SP1 and make a logical decision as to whether the frequency meets the specifications of F_{OFF1} or F_{ON1} .
- c) The *Off-State* for the ECC is defined as follows:
 - The ECC must not generate output transitions.
 - The ECC must perform transition detection at SP1 in order to check for a valid wakeup condition, defined as the input signal frequency being within F_{ON1} .
- d) The *On-State* for the ECC is defined as follows:
 - The ECC shall produce an output signal, compliant with all the SP2 parameters defined in Table 6-2 when being driven by valid SP1 data.
 - The ECC must perform transition detection at SP1 in order to check for a valid shutdown condition, defined as the input signal frequency being within F_{OFF1} .
- e) The ECC must not generate any output, capable of waking up a following device, when being supplied with an operating voltage within V_{ECCOFF} regardless of the state of the SP1 and **/RST** inputs.
- f) When **/RST** input is low, ECC shall produce no output transitions.
 - When being supplied with an operating voltage within V_{ECCGR} , the internal circuitry of the ECC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+} .
- g) When being supplied with an operating voltage within V_{ECCOR} , the ECC shall settle into operation defined as the *On-State* within a time t_{ON2} when:
 - The **/RST** input pin is driven high AND
 - The frequency of the SP1 signal is within F_{ON1} (transition detection).
- h) When being supplied with an Operating Voltage within V_{ECCGR} , the ECC shall be capable of performing transition detection and shall enter the *Off-State* within a time t_{OFF2} when
 - The **/RST** input pin is driven low OR
 - The frequency of the SP1 signal is within F_{OFF1} (transition detection).
- i) While F_{ON1} defines the frequency range where the ECC **must** be on and F_{OFF1} defines the frequency range where the ECC **must** be off, the actual transition points will most likely be in the region between F_{OFF1} max. and F_{ON1} min.

The ECC requirements are summarized in Table 7-2. Refer to Figure 7-1: for more details.

ECC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
ECC Operating Voltage Range	V_{ECCOR}		3.135	3.300	3.465	V
ECC Glitch-Safe Voltage Range	V_{ECCGR}		2.970	-	3.465	V
ECC Off Voltage Range	V_{ECCOFF}		0	-	1	V
ECC On frequency range at SP1	F_{ON1}	1)	12	-	73.743	MHz
ECC Off frequency range at SP1	F_{OFF1}		0	-	10	kHz
ECC power on delay	t_{ON2}	2)	-	-	400	μ s
ECC output settle	t_{OS2}		-	-	5	μ s
ECC power off delay	t_{OFF2}		-	-	2	μ s

Notes:
1) The ECC can still be in the On-State above this frequency.
2) t_{ON2} includes t_{OS2} .

Table 7-2: ECC Power State Requirements

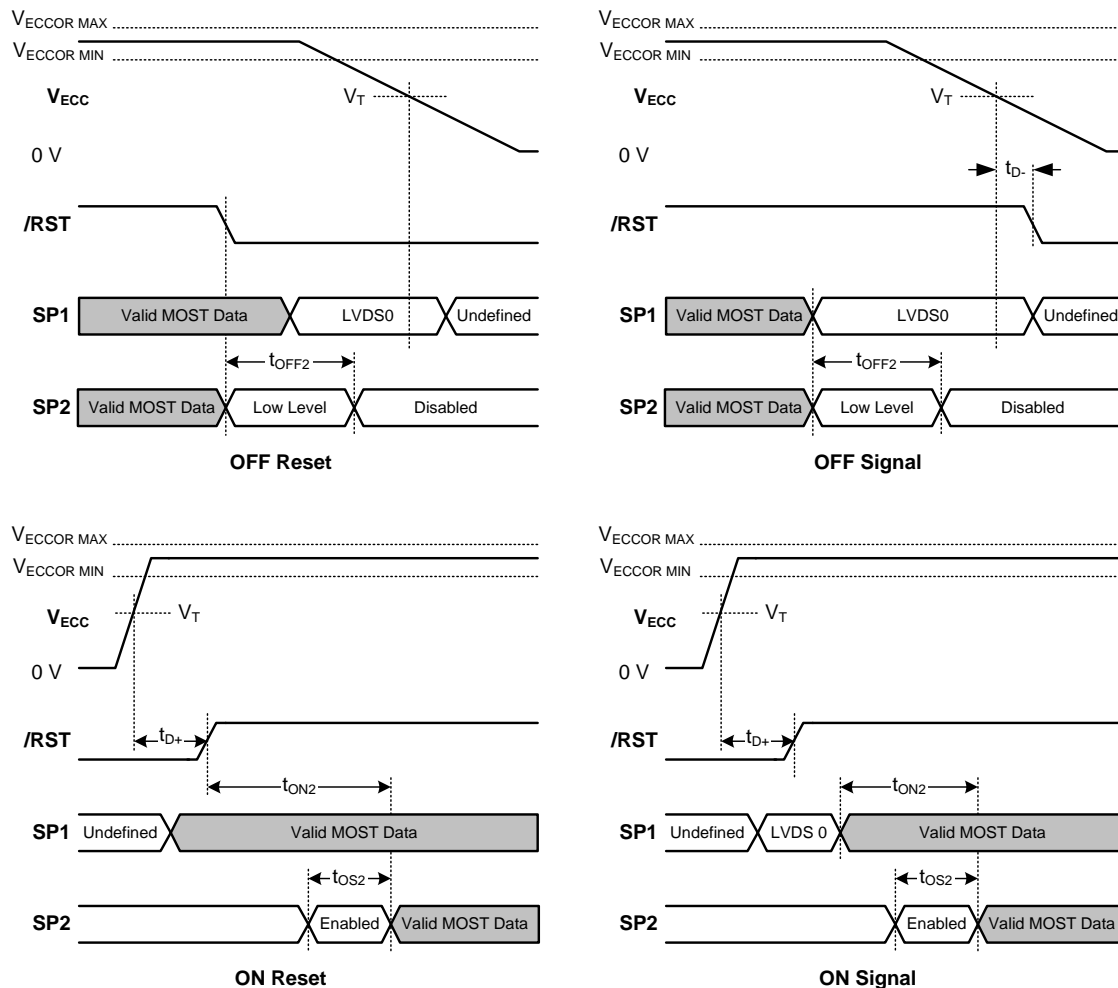


Figure 7-1: ECC Timing Diagrams

7.3.2.1 Example Scenarios

A typical powering up sequence and a typical powering down sequence for the ECC are described below and are referenced to Figure 7-1: In the above figure, Valid MOST Data is defined as follows:

- For SP1, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-1 and the bit rate requirements defined in Table 9-2.
- For SP2, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in Table 6-2, and the bit rate requirements defined in Table 9-2.

7.3.2.1.1 Power On Sequence

The power-on sequence starts with the system power supply voltage to the NIC and ECC ramping up. During the time at which the switched power supply voltage is not within the ECC's normal operating range, the **/RST** pin is pulled low by the power supply monitoring circuitry to prevent edges from being generated at SP2. Immediately after the supply voltage has reached its normal operating level, the circuitry inside the NIC and ECC may not have fully stabilized. The power supply monitoring circuitry provides a time delay from when the supply voltage has reached its normal operating value until **/RST** goes high so that the local frequency reference, NIC circuitry, and ECC circuitry will have time to stabilize. Some time after the power supply has reached its typical value, the local frequency reference that provides the NIC with timing will have stabilized, and valid LVDS logic levels will be generated by the NIC at SP1. Once the proper frequency is detected at SP1 and **/RST** is high, the ECC can then drive valid data on SP2 after an allowed short period of undefined data due to the AC-coupling between the output of the ECC and SP2. During this undefined data period the signal will balance, making use of the DC-balancing of the DCA data signal.

7.3.2.1.2 Power Off Sequence

The normal power-off sequence is initiated by SP1 traffic being driven to logic 0 by the NIC. The ECC detects this event using its internal transition detection circuit and disables the output by driving SP2 to logic level 0. The power supply to the ECC will be shut down some time later. During the ramp down of the power supply, the **/RST** pin transitions low before the ECC's power supply drops below the Glitch Safe Voltage Range, preventing any glitches on the output at SP2. The **/RST** signal is valid down to V_{VALID} min. Below V_{VALID} min, the ECC is responsible for preventing any signal oscillations at SP2 regardless of the state of **/RST**.

7.3.3 CEC Requirements

The CEC functional requirements are listed below. These requirements are applicable for the CEC when being powered by an operating voltage in the range defined by V_{CECOR} in Table 7-3:.

- a) The CEC must provide an output pin (**STATUS**) in accordance with LVTTTL (JESD8C) [4].
- b) A CEC in the *Off-State* must meet the following requirements:
 - The CEC must keep its **STATUS** signal high, the SP4 bus disabled, and consume no more than the sleep current, $I_{CCSLEEP}$.
 - The CEC must monitor the amplitude and frequency at SP3.
- c) A CEC in the *On-State* must meet the following requirements:
 - The CEC must keep its **STATUS** signal low and must provide valid output data that meets all the SP4 specifications in Table 6-6 when receiving valid data at SP3.
- d) A CEC must transition from the *Off-State* to the *On-State* upon detecting valid wakeup conditions, defined as a signal with valid SP3 amplitude (see Section 6.3.2.1) and a frequency within F_{ON3} as specified in Table 7-3:.. The wakeup procedure has the following requirements:
 - The CEC must transition the **STATUS** signal low within time t_{STATF} after valid wakeup conditions have been detected at SP3.
 - The CEC must enable the SP4 LVDS bus and produce a valid LVDS signal within time t_{LVDSV4} from when **STATUS** was set low.
 - The CEC must enter the *On-State* within time t_{ON4} from when the valid wakeup MOST data was detected.
- e) A CEC in the *On-State* must constantly monitor the input signal frequency and must transition to the *Off-State* upon detecting valid shutdown conditions. When the signal at SP3 has a frequency within F_{OFF3} as specified, the CEC must be in *Off-State*. The transition procedure to the *Off-State* has the following requirements:
 - The CEC must force the signal at SP4 to LVDS 0 and set **STATUS** high within a time t_{STATR} upon detecting valid shutdown conditions on SP3. The CEC must maintain a valid LVDS signal during the detection phase.
 - The CEC must maintain its LVDS output at a logical 0 for a hold time of t_{LVDSH4} after **STATUS** transitions high.
 - The CEC must enter the *Off-State* within time t_{OFF4} from when the valid shutdown conditions occurred.
- f) While F_{ON3} defines the frequency range where the CEC **must** be on and F_{OFF3} defines the frequency range where the CEC **must** be off, the actual transition points will be in the region between F_{OFF3} max. and F_{ON3} min.

The CEC must meet the requirements listed in Table 7-3:.. Refer to Figure 7-2: for more details.

CEC Power State Requirements	Symbol	Condition	Min.	Typ.	Max.	Unit
Powering On						
Frequency range of input at SP3 for <i>On-State</i> operation	F_{ON3}	1)	12	-	73.743	MHz
CEC power-on delay	t_{ON4}	2)	-	-	9.7	ms
Delay to STATUS falling	t_{STATF}	3)	200	-	700	μ s
STATUS falling to LVDS valid	t_{LVDSV4}		-	-	100	μ s
CEC Operating Voltage Range	V_{CECOR}		3.135	3.300	3.465	V
Powering Off						
Frequency range of input at SP3 for <i>Off-State</i> operation	F_{OFF3}		0	-	10	kHz
CEC power-off delay	t_{OFF4}	4)	-	-	1	ms
CEC LVDS hold time	t_{LVDSH4}		1	-	-	μ s
Delay to STATUS rising	t_{STATR}	5)	-	-	2	μ s
Current consumption in the <i>Off-State</i>	$I_{CCSLEEP}$		-	-	30	μ A
Notes: 1) The CEC can still be in the On-State above this frequency. 2) t_{ON4} is the sum of t_{STATF} , t_{LVDSV4} and an additional time required for SP4 to be valid MOST traffic. 3) Time from valid wakeup condition to status low, see Section 7.3.3 d). 4) t_{OFF4} is the sum of t_{STATR} and t_{LVDSH4} . 5) Time from signal off to status high, see Section 7.3.3 e).						

Table 7-3: CEC Power State Requirements

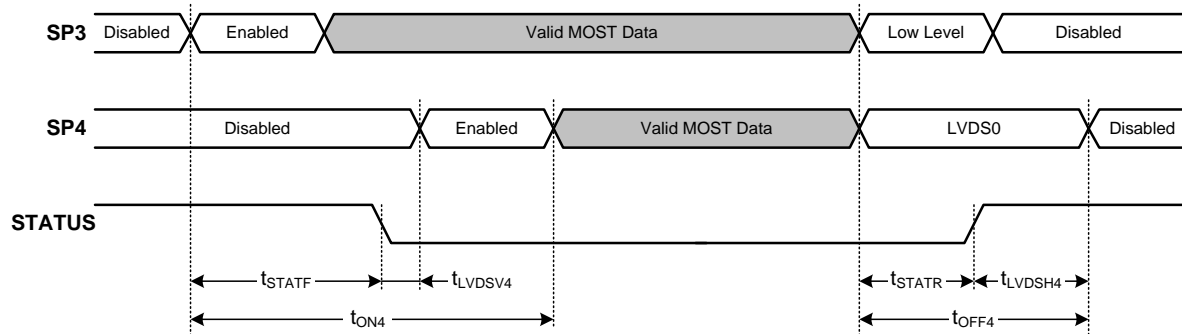


Figure 7-2: CEC Timing Diagram

7.3.3.1 Example Scenarios

The typical sequences explained below provide a description of the timing shown in Figure 7-2. Initially it is assumed, that the CEC is powered, but in its *Off-State* with **STATUS** high and the SP4 bus disabled. In the above figure, Valid MOST Data is defined as follows:

- For SP3, Valid MOST Data is DCA encoded data that meets the link quality parameters according to Section 6.3.2.1 and the bit rate requirements listed in *Table 9-2*.
- For SP4, Valid MOST Data is DCA encoded data that meets the link quality parameters defined in *Table 6-6* and the bit rate requirements listed in *Table 9-2*.

7.3.3.1.1 Power ON Sequence

A CEC that is in the *Off-State* monitors the input SP3 signal. The CEC verifies that the amplitude and signal frequency meet specifications before exiting the *Off-State*. If valid wakeup conditions are present, the CEC sets **STATUS** low, enables the SP4 LVDS bus. After a settling time, valid LVDS logic levels are present although valid MOST data may not be on the bus yet. After a short period, the CEC is fully on and valid MOST data is on the SP4 bus.

7.3.3.1.2 Power OFF Sequence

A CEC that is in the *On-State* is always monitoring the signal frequency at SP3. If the frequency does not meet specifications, the CEC begins transitioning to the *Off-State* by setting the SP4 output to LVDS 0 and driving the **STATUS** pin high. The SP4 bus is then maintained at LVDS 0 for a hold time while **STATUS** is high. After this hold time, the CEC disables the SP4 bus and enters the *Off-State*.

8 System Specifications

8.1 SP4 Receiver Tolerance

The mask is designed such that a good signal will not touch it at any location. A pattern that touches the mask must be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitudes, jitter, or pulse width variations will show up as closure in the eye diagram. Signals with excessively high amplitudes will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.

All the components along the link must operate with a Bit Error Rate (BER) lower than 10^{-9} . Consequently, all of the mask violation parameters have been specified with that goal in mind. Refer to Sections 7.1, 8.3, and 9 for operating conditions and interface standards.

Receiver tolerance SP4	Symbol	Condition	Min.	Typ.	Max.	Unit
Eye-Mask	$A_{4T} \dots H_{4T}$	1), 2), 3)	-	-	-	-

Parameter	Amplitude (mV)	Timing (UI)	Eye-mask
A_{4T}	0	0.300	
B_{4T}	80	0.500	
C_{4T}	-80	0.500	
D_{4T}	0	0.700	
G_{4T}	636	-	
H_{4T}	-636	-	

Notes:

- 1) Using the Golden PLL specified in Section 5.1.
- 2) The difference between the SP4 Eye-mask and the SP4 Receiver Tolerance Eye-mask in the horizontal timing direction is due to accumulated jitter along the link.
- 3) Additional vertical closure on the mask is caused by the large amount of jitter present on the signal. The signal must still comply with the LVDS specification regarding the minimum signal amplitude. The signal must still comply with the minimum input signal amplitude (see Section 9.1).

Table 8-1: Receiver Tolerance Parameters of SP4

8.2 Master Delay Tolerance

The master delay is the sum of all static phase (delay) and phase variation measured between the Rx input relative to the Tx output of the master device. The master delay and the total node count must not exceed the maximums shown in Table 8-2.

System Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Node Count	N		-	-	20	nodes
Master Delay Tolerance	T_{MDT}		-	-	$\frac{0.5}{F_s}$	μs

Table 8-2: Master Delay Tolerance Requirements

8.3 Environmental Considerations and Requirements

From the automotive OEM perspective, there are additional specifications which are considered to be minimum requirements. Nevertheless, certain OEMs may have additional requirements:

- The given parameters for all specification points have to be guaranteed by the ECU and its consisting subcomponents, under “automotive worst case conditions”, which have to be considered as OEM specific requirements. Ambient conditions like temperature range, humidity, vibration and shock, resistance against chemical agents, EMC/EMI and lifetime are defined for the ECU in these OEM specifications. To fulfill these conditions:
 - Coaxial cables and connectors shall be characterized and qualified to comply with the appropriate Automotive Application Recommendation.
 - Network Interface Controllers, CTR, ECC and CEC shall be characterized and qualified according to the AEC-Q100 requirements.
 - MOST interfaces shall utilize an EMC optimized design

Other functional requirements that must be considered:

- The CTR, ECC and CEC shall operate in an ambient environment with an operating temperature range of $T_A = -40^{\circ}C$ to $+105^{\circ}C$.

9 Electrical Interfaces

9.1 LVDS

All component-level RX data and TX data electrical interfaces must be LVDS [3] compliant. Exceptions are listed in Table 9-1. All PCB-level RX data and TX data electrical interfaces must be designed such that components compliant with [3] shall operate correctly. This requirement applies to PCB-level components only and is not intended for wiring harness. All electrical signals must maintain the correct polarity from CEC to NIC and from NIC to ECC.

Exception regarding LVDS [3]	Symbol	Condition	Min.	Max.	Unit
Common-mode Input Voltage range	V_{CM}		0.05	$V_{cctx} - 1.2V$	V
Steady-state Input Amplitude	V_{ISS}	1), 2)	0.30		V
Combined impedance of receiver loads connected to the bus	R_{CRL}	3), 4)		30	kOhm
Transition Times	$t_r ; t_f$	5)	200		ps
Notes: 1) Refers to chapter 4.2.4 "Receiver input sensitivity measurements" in [3]. 2) Difference between high-state and low-state of bimodal waveform. 3) The 30kOhm resistors represent the combined impedance of 4 receiver loads connected to the bus. 4) Refers to chapter 4.1.1 "Full Load Measurements" in [3]. 5) t_r : 20% -80% , t_f : 80% -20%.					

Table 9-1: Exception regarding LVDS [3]

9.2 Bit Rate and Frequency Tolerance

Specifications for the operating bit rates are shown in Table 9-2. Each MOST150 cPHY Automotive node requires a local frequency reference. Manufacturable frequency references operate at some frequency offset tolerance around the nominal F_s (either 44.1 kHz or 48 kHz). System interoperation relies on these offsets being minimized. The Time Base Deviation, Δ_{FS} , is this offset and is measured in parts per million (ppm).

Bit Rate and Frequency Tolerance Parameters	Symbol	Min.	Typ.	Max.	Unit
Time Base Deviation	Δ_{FS}	-200	0	+200	ppm
Bit Rate for 44.1 kHz frame rate	BR_{44}	135.448105	-	135.502295	Mbits/s
Bit Rate for 48.0 kHz frame rate	BR_{48}	147.426509	-	147.485491	Mbits/s

Table 9-2: Bit Rate and Frequency Tolerance

The nominal Bit Rate is obtained by multiplying the frame rate by 3072. The minimum values are obtained by taking the nominal frame rates and subtracting the time base deviation. The maximum values are obtained by taking the nominal frame rates and adding the time base deviation.

Appendix A: Connectors Mechanical Specifications and Keying

This specification recommends connectors compliant to [5] to be used for cPhy Automotive ECUs, but does not limit the connector to only those specified. Additional connector requirements may be set by the OEM.

Connector mechanical coding is not subject of that specification and is OEM specific.

Appendix B: Specification Points – Special Cases

In some special cases a MOST device may not have connectors directly at the device housing, but rather a cable connection with a connector at the end (sometimes called a “Pigtail”) as shown on the figure below.

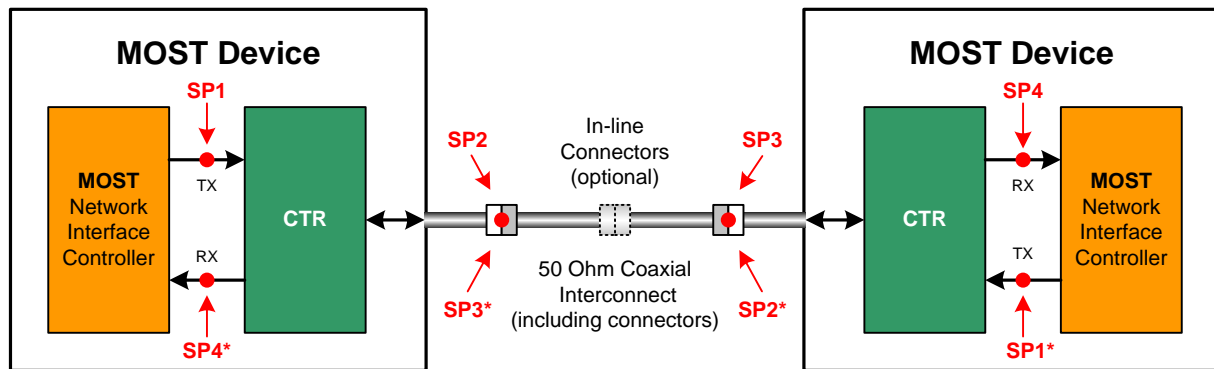


Figure B-1: “Pigtail” connection

In these cases specification points SP2 and SP3, respectively SP2* and SP3* are to be assumed at the connector of the cable end. The requirements, as defined in in this specification, are applicable for the signal path from the connector (including “pigtail” cable) to the CTR.

Appendix C: Coaxial Interconnect Attenuation

Using curve fitting, it can be determined whether the cable attenuation characteristics of a possible coaxial interconnect is close enough to such an ideal cable.

Therefore a comparison is made with a fitted transfer curve whereby the allowable fitting curves are limited to typical cable-like behavior.

A coaxial cable including inline connectors shall have attenuation versus frequency characteristic exhibiting cable-like behavior over the frequency ranges from 1 MHz to 450 MHz.

The following formula shall be used for fitting, where f is the frequency in Hz:

$$Attenuation(f) = -DC_{loss} - \sqrt{\frac{f}{F_{skin}}}$$

Equation C-1: Attenuation versus frequency (in dB)

DC_{loss} (in dB) is a fitting parameter that takes care of the DC attenuation, and the second term takes care of the frequency dependent loss, whereby F_{skin} is representative for the skin effect loss.

The fitting is based on maximum likelihood estimation, with equal weights for all measurements based on the least mean squares method. During the fitting process, DC_{loss} and F_{skin} are each free to change. For fitting, at least 40 measurement points per decade (logarithmically spaced) shall be used. The fitting residue is to be determined and must comply with table 6-4.

Example: A 15 m coaxial interconnect is measured in the lab from 1 MHz to 450MHz. See Figure C-1. The cable is of good quality since the norm of the fit residue that is always below 1 dB. In this case the obtained fit parameters are $DC_{loss} = 0.17$ dB and $f_{skin} = 9.2 \times 10^6$ Hz/dB².

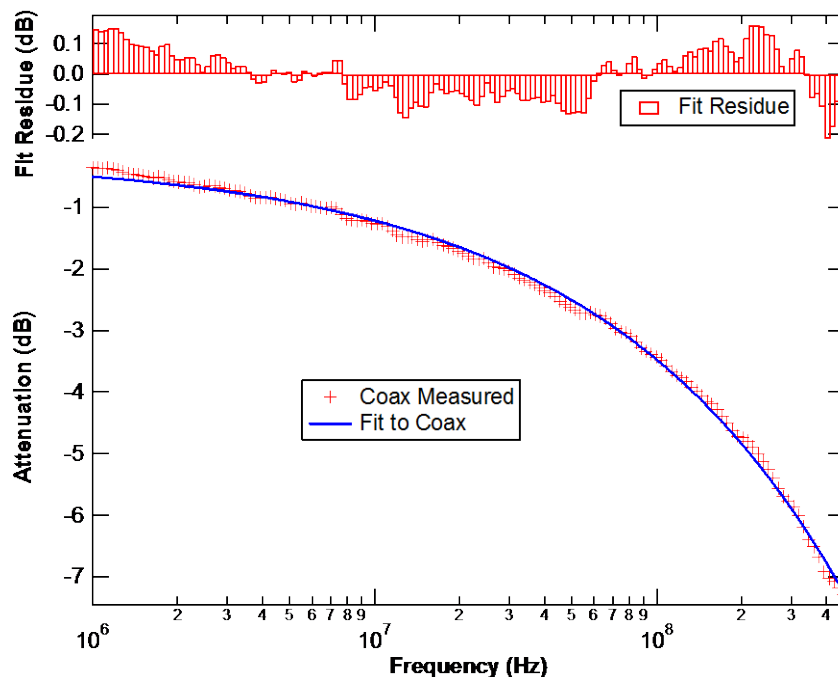


Figure C-1: Deviation from normal attenuation behavior versus frequency

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