MOST

Media **O**riented **S**ystems **T**ransport

Multimedia and Control Networking Technology

MOST150 Physical Layer Stress Test Tool
Rev 1.1
05/2017

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For more information on the MOST technology, please contact:

MOST Cooperation
Administration
Emmy-Noether-Str. 14
76131 Karlsruhe
Germany

Tel: (+49) (0) 721 966 50 00

E-mail: contact@mostcooperation.com
Web: www.mostcooperation.com

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Contents

Document References

All documents, which are referenced by this MOST document are listed here with the actual revision this document is referring to.

Number	Document	Revision
[1]	MOST Physical Layer Basic Specification	1.0
[2]	MOST150 oPHY Automotive Physical Layer Sub-Specification	1.1
[3]	MOST150 oPHY Compliance Verification Procedure – Physical Layer	1.1
[4]	MOST150 cPHY Automotive Physical Layer Sub-Specification	1.1
[5]	MOST150 cPHY Compliance Verification Procedure – Physical Layer	1.0
[6]	MOST Specification	3.0

Document History

Change Ref.	Section	Changes
V1.1	-	Release version

Change Ref.	Section	Changes
V1.0.1-0d1	2	Updated Fig. 2-1
V1.0.0-0d1	-	Initial revision

Glossary

Term	Definition
API	Application Programming Interface
ATE	Automated Test Equipment
BERT	Bit Error Rate Tester
DC	Direct current
DUT	Device Under Test
E/O converter	Electrical / Optical converter
FB ENC	Function Block ExtendedNetworkControl
FB ET	Function Block EnhancedTestability
FOT	Fiber Optic Transmitter
INIC	Intelligent Network Interface Controller
LED	Light Emitting Diode
MOST	Media Oriented System Transport
OEM	Original Equipment Manufacturer
PhLSTT	Physical Layer Stress Test Tool
Phy	Physical
PLL	Phase Locked Loop
POF	Plastic Optical Fiber
PWD	Pulse Width Distortion
TO	Test Operator
UI	Unit Interval

1 Introduction

For limited compliance testing of MOST150 components the MOST150 Limited Physical Layer Compliance Specification [3], [5] defines a set of setups for measuring specific parameters as defined in MOST150 oPHY Automotive Physical Layer Sub-Specification [2] and MOST150 cPHY Automotive Physical Layer Sub-Specification [4]. Parts of these setups are:

- The MOST150 component to be tested, named “Device Under Test (DUT)” for the scope of this document,
- A set of state-of-the-art (commercially available) optical (such as: optical mode mixer, programmable optical attenuator, POF splitters, etc.) and electrical (such as: oscilloscope, optical power meter/detector, multi-meter, programmable power supply, temp. chamber, etc.) test equipment as defined in the corresponding test and
- A custom tool, named “Physical Layer Stress Test Tool (PhLSTT)” for the scope of this document, which represents the tool described within this document.

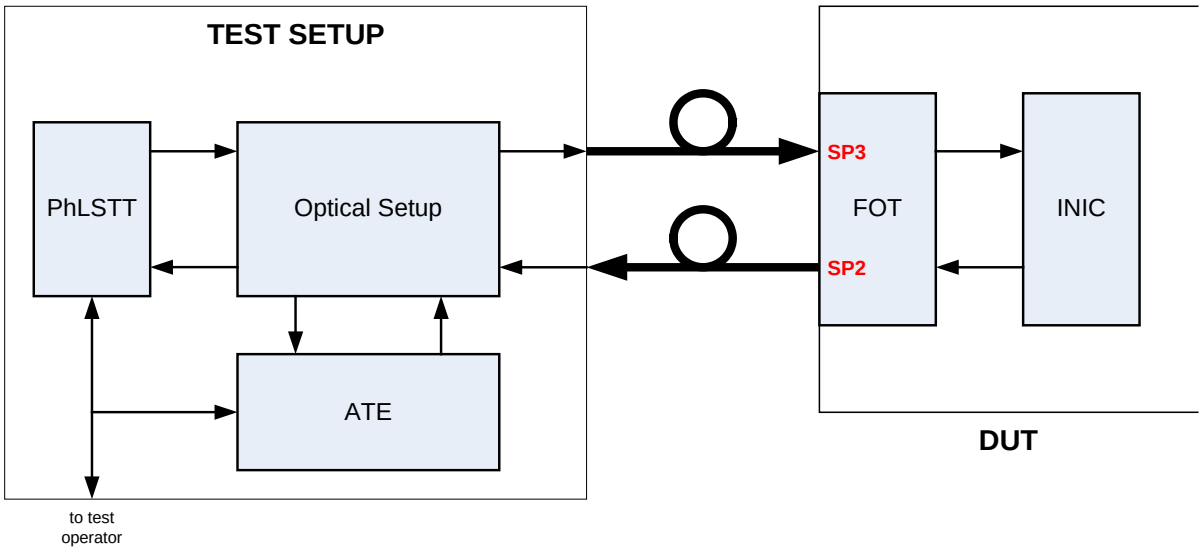

Figure 1-1: Generalized Test Setup

The main purpose of the PhLSTT is to feed the DUT with the Stress Test Pattern defined in [2], [4] and to check the DUT’s response for errors. At the time of creation of this document no state-of-the-art tools are known to exist that incorporate all the features required for the tool described herein. E.g., a state-of-the-art signal generator cannot be directly synchronized to the MOST network of the DUT and cannot compare the incoming data stream to the reference data stream. Another example is a state-of-the-art Bit Error Rate Tester (BERT). No available BERT is capable of generating the specific MOST150 Stress Test Pattern [2], [4] and offers the needed memory depth. Moreover, none of the listed tools have MOST functionality.

The PhLSTT’s primary usage will be in the limited layer compliance testing process at a certified compliance test house, but also for pre-compliance testing or as a development support tool at an OEM.

The tool is implemented as:

- A standalone custom-made tool or
- A combination of commercially available tools or
- A combination of commercially available tools including some custom hardware.

2 Description

The figure below depicts a basic functional block diagram of the PhLSTT.

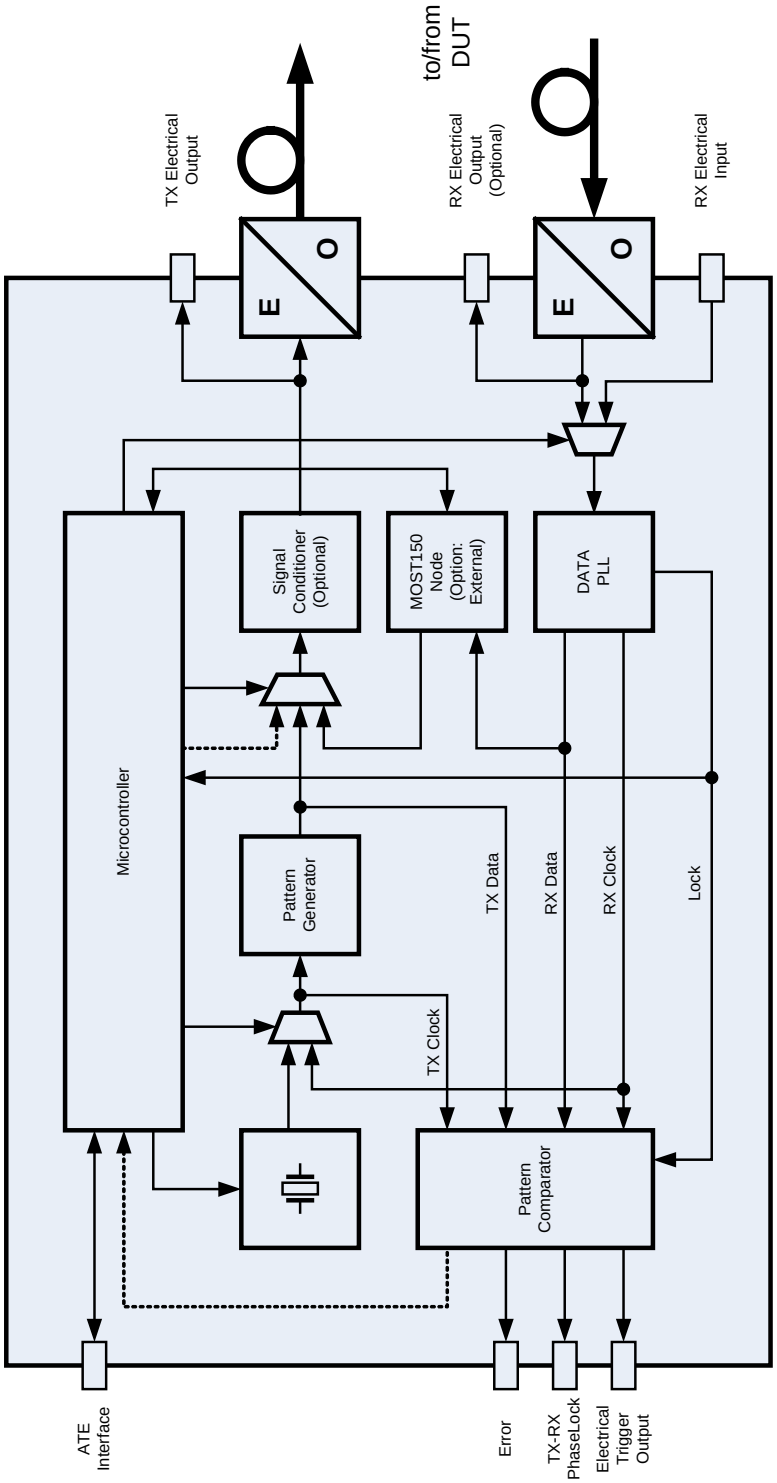

Figure 2-1: PhLSTT Basic Functional Block Diagram

2.1 Functional Description

The tool main function is the generation of the stress pattern. Depending on the DUT there are four functionally different operation modes of the PhLSTT:

- MOST network with TimingMaster DUT
- MOST network with TimingSlave DUT
- Stress testing of TimingMaster DUT
- Stress testing of TimingSlave DUT

Both MOST network modes are used for communication with the DUT in order to initialize it and to initiate stress test mode as well as to read back the result of the test. The PhLSTT contains a MOST150 node or connects the DUT to an external MOST150 node.

Stress testing modes do not provide MOST networking functionality and are used for testing the MOST150 Physical Layer only.

When performing a test with a TimingMaster DUT, the DUT is the timing reference for the MOST ring and the stress pattern generated by the PhLSTT shall be synchronous to the DUT timing. For this purpose, the PhLSTT receives the MOST signal from the DUT and extracts the clock from it by means of the DATA PLL function. The pattern generator uses the recovered clock as a time base for generation of the stress pattern, ensuring the stress pattern is synchronous to the TimingMaster DUT (clock) timing.

When performing a test with a TimingSlave DUT, the pattern generator uses a local oscillator as a time base for the generated stress pattern.

A Signal conditioner function allows calibration of the output signal's PWD prior to a test (in case the E/O converter does not provide such). Optionally, the block could be used for static PWD manipulation for the purposes of the test.

The operation of the PhLSTT is supervised and controlled by a microcontroller, which is also responsible for interfacing to the Test Operator (TO) or the Automated Test Equipment (ATE) by means of an industry established communication interface.

The pattern comparator function compares the input and the output data streams, taking into account the phase difference (propagation + input-to-output delay) between them. It flags the errors if data differences (Error output) or sudden phase jumps (Phase Lock output) are detected. The Error and the Phase Lock outputs could be used to trigger external equipment (such as oscilloscopes, etc.) to allow narrowing down eventual problems. The data integrity and status information shall also be made available to ATE through the dedicated interface.

2.2 Test Flow Overview

The figure below depicts an overview of the test flow.

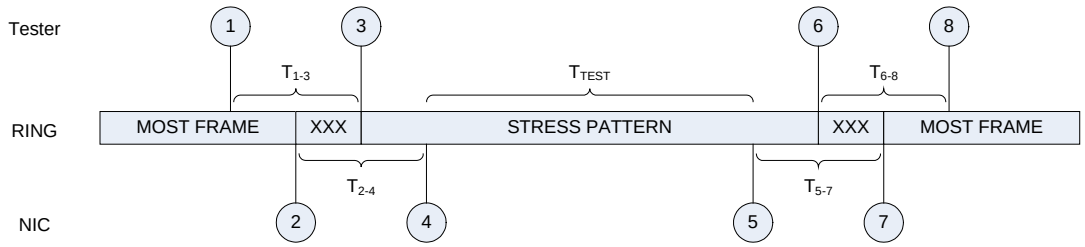

Figure 2-2: Test Flow Overview

1 – PhLSTT sends command to DUT over MOST150 (FB ET or FB ENC) to enter Test Mode.
2 – DUT enters Retimed Bypass Mode.
3 – PhLSTT starts transmitting the Stress Pattern.
4 – DUT clears the Error Counter and Lock Log.

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5 – DUT reads back Error Counter and Lock Log.
6 – PhLSTT switches to MOST150 Communication Mode.
7 – DUT switches back to its original MOST150 Mode.
8 – PhLSTT reads back the result.

Switching times (T_{X-Y}) are in the range 10 ms – 500 ms with accuracy better than or equal to 10 ms;

Lead-in / Lead-out: typ. 1000 ms (min. 500 ms; max. 2000 ms).

T_{TEST} time is in the range 1 sec – 1000 sec with accuracy better than or equal to 10 ms.

Duration: max. 1000 seconds.

2.3 Feature List

2.3.1 Mandatory Features

2.3.1.1 Functional Requirements

- Possibility to test TimingMaster and TimingSlave DUT

  The corresponding mode shall be set by the tool operator or by the automated setup depending on the type of the DUT being tested. The function implies that the PhLSTT is able to recover the clock from the data stream of a TimingMaster DUT and use it as a time base for its output, with the result that the output stream is synchronous to the DUT (clock) timing.

- Possibility to test 48.0 kHz frame rate network (44.1 kHz optional)

  The tool shall have internal time base capable of generating a signal with (clock) timing suitable for testing a DUT built for 48.0 kHz (44.1 kHz optional) MOST150 network frame rate. The corresponding mode shall be set by the tool operator or by the automated setup depending on the type of the DUT being tested (48.0 kHz being default mode).

- MOST150 networking functionality

  The MOST network functionality shall be either built in or provided through an external MOST device function, which allows the tester device to talk to FBlock ET (FBlockID 0x0F) or FBlock ENC (FBlockID 0x0A), respectively, of the DUT (through the MOST port to be tested) in order to:

  - Establish a stable NET ON (NetInterface Normal Operation) condition.
  - Initiate physical layer stress test mode with the corresponding parameters.
  - Exit stress test mode
  - Read back the result (error counter)

- Possibility to generate stress pattern.
  - Pattern rate: 294.912 MSample per second (270.9504 MSample per second)
  - Pattern length: 36864 UI
  - Synchronous to
    - Local oscillator or
    - Optical signal from TimingMaster DUT
  - Pattern content as defined in [2], [4] (for future purposes – possibility for arbitrary pattern definition)

- Pattern comparator function

  - Lock output (also readable through ATE interface)
  - Error output (also readable through ATE interface)
  - Straight or edge based comparison (compare against 1:1 and inverted pattern)

- Signal conditioner function

  Signal conditioner shall allow adjustment of the PWD of the output signal within range of at least: -1 ns to +1 ns with at least 20 equidistant steps.

- Possibility to output DC light, respectively produce low frequency DC light stimuli (< 1 MSample per second)

- Possibility to detect light-off condition at its input

- ATE interface

  The ATE interface shall have an open protocol (respectively open driver API) allowing integration of the tool in custom automated setups. An example GUI is beneficial, but not mandatory.

  During the test status information (data match, TX-RX phase lock, etc.) of the pattern comparator function shall be available through the ATE interface.

  After the test, the following information shall be available through the ATE interface:

    - Status DUT:
        - Error counter (FB ET function)
        - Lock flag (FB ET function)
    - Status Pattern Comparator (depending on the architecture):
        - Error counter/flag,
        - Phase-Lock status (flag or phase-shift value)

2.3.1.2 Physical Requirements

- Operating conditions

  The tool shall be designed for laboratory use, therefore limited temperature and humidity range are required:
  - Operating Temperature: 10°C – 35°C
  - Operating Relative Humidity: 20 % – 80 % (not condensing)

- Interfaces

  - TO / ATE interface

    PhLSTT shall have a means (interface) to communicate to Test Operator or Automated Test Equipment though a low complexity bidirectional interface such as RS232 (for sending commands and read back the result).

  - Electrical signal output (direction TESTER → DUT)

    Differential output – 100 Ohm terminated, suitable for direct interface to state-of-the art E/O modules (LED, Laser, etc.).

  - Electrical Trigger output

    Electrical signal, which pulses “High” with every start of the repeating stress pattern during the test time (T_{TEST}).

  - Optical output (Direction TESTER → DUT)

    Standard MOST receptacle as defined in [2].

    Laser based optical emitter with minimum +1 dBm optical power output to allow compensation of the insertion loss of the optical setup elements.

  - Electrical input (Direction DUT → TESTER)

    AC coupled differential input – 100 Ohm terminated, suitable for direct interface to state-of-the art O/E modules.

  - Optical input (Direction DUT → TESTER)

    Standard MOST receptacle as defined in [2]

2.3.1.3 Signal Requirements

- Input signals

  The PhLSTT's input shall be able to successfully recover (BER < 10^{-9}):

  - Optical signal compliant with all specifications for SP3 according to [2]
  - Electrical signal compliant with all specifications for SP4 according to [2]

- Output signals

  The PhLSTT shall produce at its output:

  - Optical signal compliant with all specifications for SP2 (or better) according to [2]
  - Electrical signal compliant with all specifications for SP1 (or in combination with external EOC – optical signal compliant with SP2 or better) according to [2]

2.3.2 Optional Features

The following features are optional:

- RX electrical output
- 44.1 kHz support

3 Appendix A: List of Figures

Notes: