MOST

Media **O**riented **S**ystems **T**ransport

Multimedia and Control
Networking Technology

MOST Specification
MOST Compliance Test of Physical Layer
Rev 1.0
12/2003

Version 1.0-00

MOST COOPERATION

Legal Notice

COPYRIGHT

LICENSE DISCLAIMER

Nothing on any MOST Cooperation Web Site, or in any MOST Cooperation document, shall be construed as conferring any license under any of the MOST Cooperation or its members or any third party's intellectual property rights, whether by estoppel, implication, or otherwise.

CONTENT AND LIABILITY DISCLAIMER

MOST Cooperation or its members shall not be responsible for any errors or omissions contained at any MOST Cooperation Web Site, or in any MOST Cooperation document, and reserves the right to make changes without notice. Accordingly, all MOST Cooperation and third party information is provided "AS IS". In addition, MOST Cooperation or its members are not responsible for the content of any other Web Site linked to any MOST Cooperation Web Site. Links are provided as Internet navigation tools only.

MOST COOPERATION AND ITS MEMBERS DISCLAIM ALL WARRANTIES WITH REGARD TO THE INFORMATION (INCLUDING ANY SOFTWARE) PROVIDED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT. Some jurisdictions do not allow the exclusion of implied warranties, so the above exclusion may not apply to you.

In no event shall MOST Cooperation or its members be liable for any damages whatsoever, and in particular MOST Cooperation or its members shall not be liable for special, indirect, consequential, or incidental damages, or damages for lost profits, loss of revenue, or loss of use, arising out of or related to any MOST Cooperation Web Site, any MOST Cooperation document, or the information contained in it, whether such damages arise in contract, negligence, tort, under statute, in equity, at law or otherwise.

FEEDBACK INFORMATION

Any information provided to MOST Cooperation in connection with any MOST Cooperation Web Site, or any MOST Cooperation document, shall be provided by the submitter and received by MOST Cooperation on a non-confidential basis. MOST Cooperation shall be free to use such information on an unrestricted basis.

TRADEMARKS

MOST Cooperation and its members prohibit the unauthorized use of any of their trademarks. MOST Cooperation specifically prohibits the use of the MOST Cooperation LOGO unless the use is approved by the Steering Committee of MOST Cooperation.

SUPPORT AND FURTHER INFORMATION

For more information on the MOST technology, please contact:

MOST Cooperation
Administration
P. O. Box 4327
D-76028 Karlsruhe
Germany

Tel: (+49) (0) 721 966 50 00
Fax:(+49) (0) 721 966 50 01
E-mail: contact@mostcooperation.com
Web: www.mostcooperation.com

MOST Compliance Test of Physical Layer
Rev. 1.0

Contents

1 INTRODUCTION 9
1.1 General Remarks 10
1.1.1 Terminology of Naming Within this Document 10
1.1.2 Terminology of Specification Points 11
1.1.3 Timing Distortion Parameters 11
1.1.4 Test Pattern 11
1.1.4.1 Worst-Case Pattern for Pulse Width Variation (WCPWV) 12
1.1.4.2 Worst-Case Pattern for Data Dependent Jitter (WCDDJ) 13
1.1.4.3 Worst-Case Signal for Uncorrelated Jitter (WCUJ) 14
1.1.5 Workflow of Pulse Width Distortion Parameter Measurements 15
1.1.6 Measurement of Phase Variation Parameters 18
1.1.6.1 Examples for Test Setups Using Real MOST Devices 20
1.1.6.2 Example for Data Dependent Jitter (Optical Link) 22
1.1.6.3 Example for Uncorrelated Jitter (Optical Link) 23
1.1.7 Error Rate 24
1.1.7.1 Pulse-Width-Distortion vs. Error Rate 24
1.1.7.2 Example for Minimum Acquisition Time 24
1.1.7.3 Measurement of PWV vs. Error Rate Using a “Tail Fitting Procedure” 25
1.2 Measurement Tools 28
1.2.1 State of the Art Tools 28
1.2.2 Measurement - Adapter for SP2 29
1.2.3 Measurement - Adapter for SP3 30
1.2.4 Additional Measurement Requirements 30
2 PARAMETERS OF SPECIFICATION POINTS 31
2.1 SP1 32
2.1.1 Bit Rate 32
2.1.2 Logic Levels 33
2.1.3 Fall and Rise Times 33
2.1.4 Pulse-Width-Variation and Average Pulse Width Distortion 33
2.1.5 Data Dependent Jitter and Uncorrelated Jitter 34
2.1.6 Input Resistance and Input Capacitance 35
2.2 SP2 37
2.2.1 Bit Rate 38
2.2.2 Peak Wavelength 38
2.2.3 Full Width at Half Maximum (FWHM) 38
2.2.4 Optical Output Power 38
2.2.5 Optical Output Power for “Light Off” 39
2.2.6 Extinction Ratio 39
2.2.7 Fall and Rise Times 40
2.2.8 Pulse-Width-Variation and Average Pulse Width Distortion 41
2.2.9 Data Dependent Jitter and Uncorrelated Jitter 42
2.2.10 Positive and Negative Overshoot 43
2.2.11 High Level Signal Ripple 43
2.3 SP3 44
2.3.1 Bit Rate 44
2.3.2 Receivable Optical Power Range for Data Recovery 44
2.3.3 Receivable Optical Power Range for Switching to "Light Off State" 45
2.3.4 Extinction Ratio 45
2.3.5 Rise and Fall Time 46
2.3.6 Pulse-Width-Variation and Average Pulse Width Distortion 46
2.3.7 Data Dependent Jitter and Uncorrelated Jitter 47
2.4 SP4 48
2.4.1 Bit Rate 49
2.4.2 Logic Levels 49
2.4.3 Rise / Fall Time 49
2.4.4 Pulse-Width-Variation and Average Pulse Width Distortion 50

2.4.5 Data Dependent Jitter and Uncorrelated Jitter 51

3 ACCUMULATED JITTER 52

3.1 Additional Test Signals and Requirements 53
3.2 System Measurements 54
3.2.1 Measurement of System Wander 54
3.2.2 Measurement of Total DDJ and UJ 57
3.2.3 Split Measurement of Accumulated DDJ and UJ 58
3.2.3.1 Worst-Case Measurement of DDJ+UJ up to the Last Slave Node 58
3.2.3.2 Measurement of Link Jitter Between Last Slave and Master 61
3.2.4 Measurement of Application Specific DDJ+UJ 62

APPENDIX A: LIST OF FIGURES 64

APPENDIX B: LIST OF TABLES 65

APPENDIX C: ABBREVIATIONS 66

Bibliography

Number/ Keyword	MOST related Documents
[1]	MOST Specification Framework
[2]	MOST Specification
[3]	MOST High Protocol Specification
[8]	MOST FunctionCatalog
[9]	MOST Specification of Physical Layer
[10]	MOST Compliance Test of Physical Layer
[11]	MOST Compliance Requirements

Number/ Keyword	Other Documents
-	IEC958
-	EN/IEC 61280-2-2
-	IEC 60825-1/-2

Document History

Change Ref.	Chapter	Changes
V0.8	All	First draft
V1.0	All	First release

1 Introduction

This document "*MOST Compliance Test Of Physical Layer"* [10] is strictly related to the document "*MOST Specification Of Physical Layer V1.1*" [9]. Parameters and Limits within this document have to be adapted to newer versions of the "*MOST Specification Of Physical Layer"* as necessary.
The "*MOST Compliance Test Of Physical Layer"* [10] describes how to analyze physical interfaces, in terms of fulfilling the requirements of a MOST compliant interface. There are four specification points along an individual "point-to-point-link" that give those requirements. For details see "*MOST Specification Of Physical Layer*" [9]. See also Figure 1-1 and Table 1-1.

The process of compliance verification is defined in the MOST document "MOST Compliance Requirements [11]. It describes how to achieve compliance certification for MOST subsystems (devices) and components.

Suppliers of MOST compliant hardware do not develop "interfaces" but components and devices. To become MOST compliant, a component or a sum of combined components must fit into two MOST specified interfaces. It is committed to call components or combined components EOC (= Electrical Optical Components) that are bordered by SP1 and SP2 and OEC (= Optical Electrical Components) that are bordered by SP3 and SP4. Suppliers that want to offer MOST compliant EOCs and OECs have to confirm MOST compliance concerning their interfaces.

Suppliers of MOST devices (e.g. CD-Changer) will use MOST compliant hardware, which is developed by their own or delivered by sub supplier. Basically, the general functionality of a MOST device is based on MOST compliance confirmed hardware. Nevertheless, due to system requirements it is necessary to confirm MOST physical layer compliance of MOST devices additionally. For achieving MOST compliance, it is not sufficient to simply connect single MOST compliant components within the respective device. Compliance can be achieved only by an "over all" approach, i.e. the complete circuitry behavior must be tested.

It has to be pointed out, that this document will not describe detailed test procedures for developers and suppliers of components and devices, but it is the base for such test procedures.

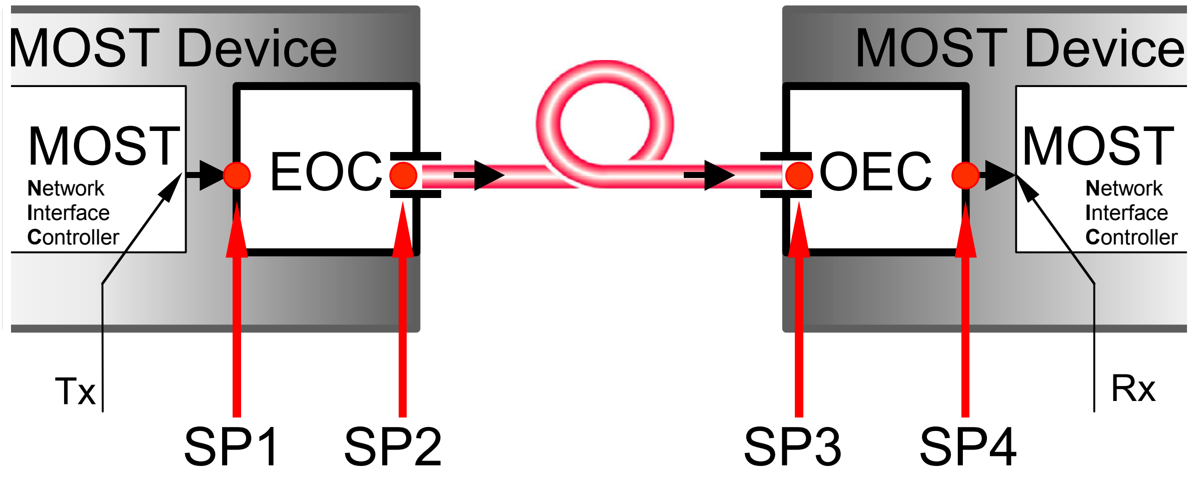


Figure 1-1: Location of specification points along a MOST point-to-point-link

	Signal at SP	Location of SP
SP1	Electrical input signal	Data input Pin of EOC
SP2	Radiated optical output signal	End face of the optical contact of the EOC (see also connector interface drawings)
SP3	Coupled optical input signal	Light input behind the end face of the optical contact of the OEC (see also connector interface drawings)
SP4	Electrical output signal	Data Output Pin of OEC, including a defined load

Table 1-1: Description of specification points.

1.1 General Remarks

1.1.1 Terminology of Naming Within this Document

System:	MOST Network consisting of several devices.
Device:	Electronic Control Unit (ECU) that contains optical MOST modules.
Module:	Assembly of components that are bounded between two specification points (e.g. EOC, OEC see Figure 1-1)
Component:	Parts that are used to build up modules (e.g. Fiber optical transceivers, connector Housing).

1.1.2 Terminology of Specification Points

All Parameters of every Specification Point are marked with the number of the corresponding Specification Point. For example the rise time along the consecutive Specification Points are marked as t_{r1}, t_{r2}, t_{r3}, and t_{r4}.

Please note: In case of general explanations the parameters are marked without numbers within the indices (e.g. rise time: t_r).

Components developers are recommended to use the same terminology of the specification points in their data sheets.

1.1.3 Timing Distortion Parameters

Deviations from ideal signal timing are called timing distortion. For details refer to *"MOST Specification Of Physical Layer"* [9] chapter 2.1.1.

1.1.4 Test Pattern

For testing the physical layer of MOST devices, - modules, -components it is essential to generate data-patterns simulating the worst-case situation of an active MOST Network. To do this there are two possibilities:

(a) Using a static worst-case pattern created by a pattern generator (useable for components and modules only, e.g. EOC/OEC). The worst-case depends on the characteristics of the hardware, which is under investigation, different hardware-concepts probably need different patterns.
Please note: The pattern does not need to fully fulfill the bi-phase coding rules. The pattern has to be DC-free (equal number of Ones and Zeros) and has to contain 1UI-, 2UI- and 3UI-elements.

(b) Using a worst-case MOST pattern (useable for all hardware components, modules and devices which are under investigation & test). The data pattern has to be routed to the synchronous and asynchronous section (whole data range) of the MOST Frame (see Figure 1-2).

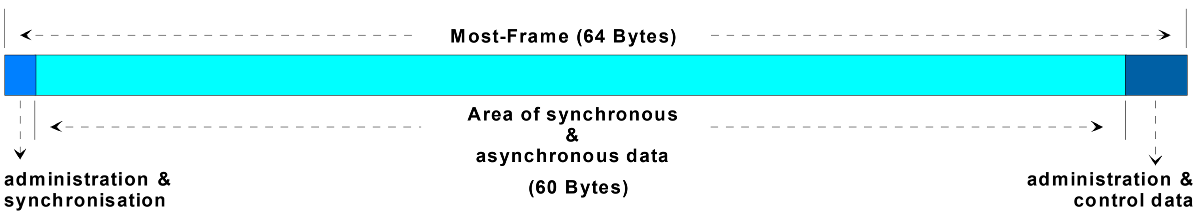


Figure 1-2: Structure of the MOST frame.

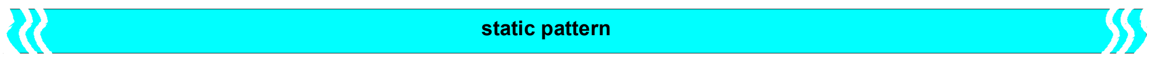
Please note:
For measuring Timing Distortion, each kind of distortion parameter requires its own pattern. These patterns are described in the following tables.

Example of generating test pattern according to (b):

1. In order to allow only synchronous data on the whole frame set SBC register (Synchronous Boundary Control) to 0x0F on the timing master. Note: Due to this SBC – setting no asynchronous data transmission is possible!
2. Route the corresponding test signal (from ADC, source port, etc.) to the whole frame.
3. Take care that the nodes in the ring do not modify the content of the synchronous range.

1.1.4.1 Worst-Case Pattern for Pulse Width Variation (WCPWV)

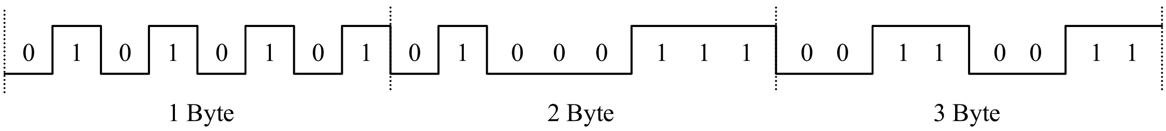
Proposal according (a)



A static pattern based on 1UI, 2UI and 3UI data elements has to be used.

Example:

The pattern is programmed in a bit generator and is permanently repeated. 1 Byte includes 8 UIs. The pattern is DC-free (equal number of Ones and Zeros).



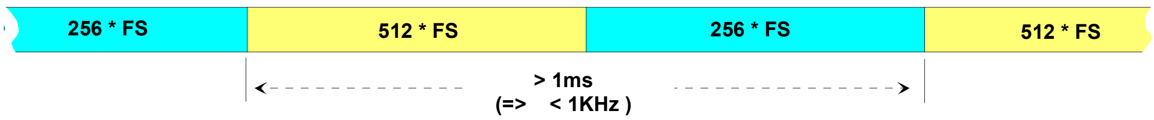
Proposal according (b)

Random Data on the MOST frame can be achieved by using an analog white-noise signal which is feed to an ADC (Analog to Digital Converter). The digital output signal of the ADC should be routed to all channels of the MOST frame.

Table 1-2: Table of worst-case pattern for pulse width variation.

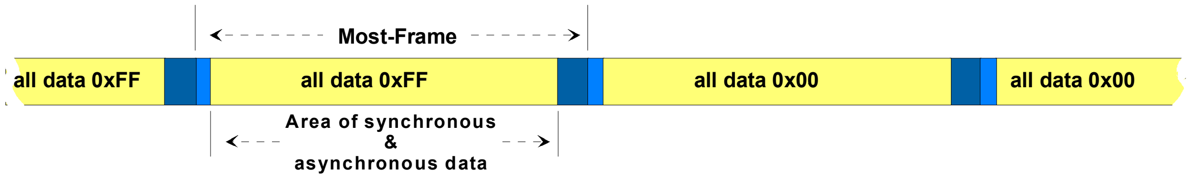
1.1.4.2 Worst-Case Pattern for Data Dependent Jitter (WCDDJ)

Proposal according (a)



A WCDDJ Pattern according to (a) can be achieved by using a programmable rectangle generator (50% duty cycle) which toggles between 256 * FS (11.289MHz @ FS = 44.1kHz) and 512 * FS (22.579MHz @ FS = 44.1kHz) with a toggle frequency of less than 1kHz. The alternation between both frequencies can also be applied in two steps.

Proposal according (b)

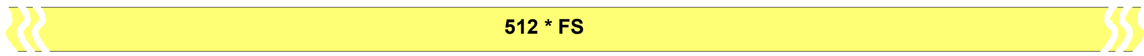


A WCDDJ MOST Pattern according to (b) can be achieved by routing a rectangle - signal (TTL, < 1kHz) to all the synchronous channels of the MOST frame (see example in chapter 1.1.4). This causes the MOST signal to change from “all zeros” to “all ones” or to toggle between 11.289MHz and 22.579MHz (@ FS= 44.1kHz), which is the lower and higher border of the MOST signal (except influence of the preamble). Timing distortion due to the preamble elements have to be removed from the measurement result.

Table 1-3: Table of worst-case pattern for data dependent jitter.

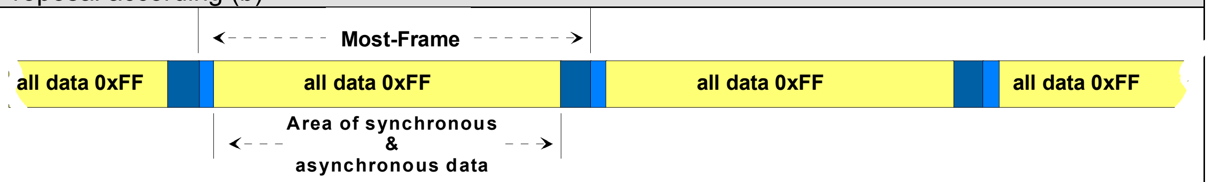
1.1.4.3 Worst-Case Signal for Uncorrelated Jitter (WCUJ)

Proposal according (a)



A 512 * FS rectangle signal (duty cycle = 50%, jitter < 500ps) can be used. This is 22.579MHz @ FS = 44.1kHz

Proposal according (b)



The WCUJ according to (b) is a MOST signal with a high frequency content (22.579MHz @ FS = 44.1kHz) in order to generate random noise as much as possible. It can be generated in the same way as WCDDJ, only the test signal is permanent high. Timing distortion due to 2UI and 3UI elements (Preamble and administration data) have to be removed from the measurement result.

Table 1-4: Table of worst-case pattern for uncorrelated jitter.

1.1.5 Workflow of Pulse Width Distortion Parameter Measurements

The MOST Physical Layer Specification defines two parameters:

- Pulse-Width-Variation t_{pwv}
- Average Pulse-Width-Distortion t_{apwd}

They describe the maximum tolerances for Pulse-Width-Distortion on a point-to-point link within a MOST Network:

The limits for the pulse width variation are valid for all data elements (Length of high pulse = n*UI; n=1,2,3).

Workflow of Parameter Check (see Table 1-5 below)

1. *The min- / max-pulse-lengths (t_{pwmx}, t_{pwmn}) are results of a real measurement (line 4 and 5 of Table 1-5)*
2. *All measured pulse lengths have to be within the limits ($t_{pwv(max)}$, $t_{pwv(min)}$) (line 2 and 3 of Table 1-5)*
3. *The Average Pulse Width Distortion APWD is calculated as $t_{apwd(calc)} = (t_{pwmx} + t_{pwmn} - 2*n*UI)/2$ (see line 9 of Table 1-5)*
4. *The calculated Average Pulse Width Distortion (line 9 of Table 1-5) has to be within the limits $t_{apwd(min)}$ and $t_{apwd(max)}$ (line 7 and 8 of Table 1-5)*

	Symbol	Relations	Remarks
1	T_{pwv}	$= t_{pwv(max)} - t_{pwv(min)}$	**P**ulse **W**idth **V**ariation (Specified Range)
2	$t_{pwv(min)}$		Lower Limit of specified Range PWV
3	$t_{pwv(max)}$		Upper Limit of specified Range PWV
4	t_{pwmn}	$t_{pwmn} \geq t_{pwv(min)}$	Minimum measured Pulse Length
5	t_{pwmx}	$t_{pwmx} \leq t_{pwv(max)}$	Maximum measured Pulse Length
6	T_{apwd}	$= t_{apwd(max)} - t_{apwd(min)}$	**A**verage **P**ulse **W**idth **D**istortion (Specified Range)
7	$t_{apwd(min)}$		Lower Limit of specified Range APWD
8	$t_{apwd(max)}$		Upper Limit of specified Range APWD
9	$t_{apwd(calc)}$	$= (t_{pwmx} + t_{pwmn} - 2*n*UI)/2$ $t_{apwd(min)} \leq t_{apwd(calc)} \leq t_{apwd(max)}$	Calculated APWD based on measurements n = 1, 2, 3

Table 1-5: Table of abbreviations regarding signal distortion.

The following Figure 1-3 and Table 1-6 show the introduced workflow based on a realistic measurement on SP4 at 1UI and 44.1kHz FS.

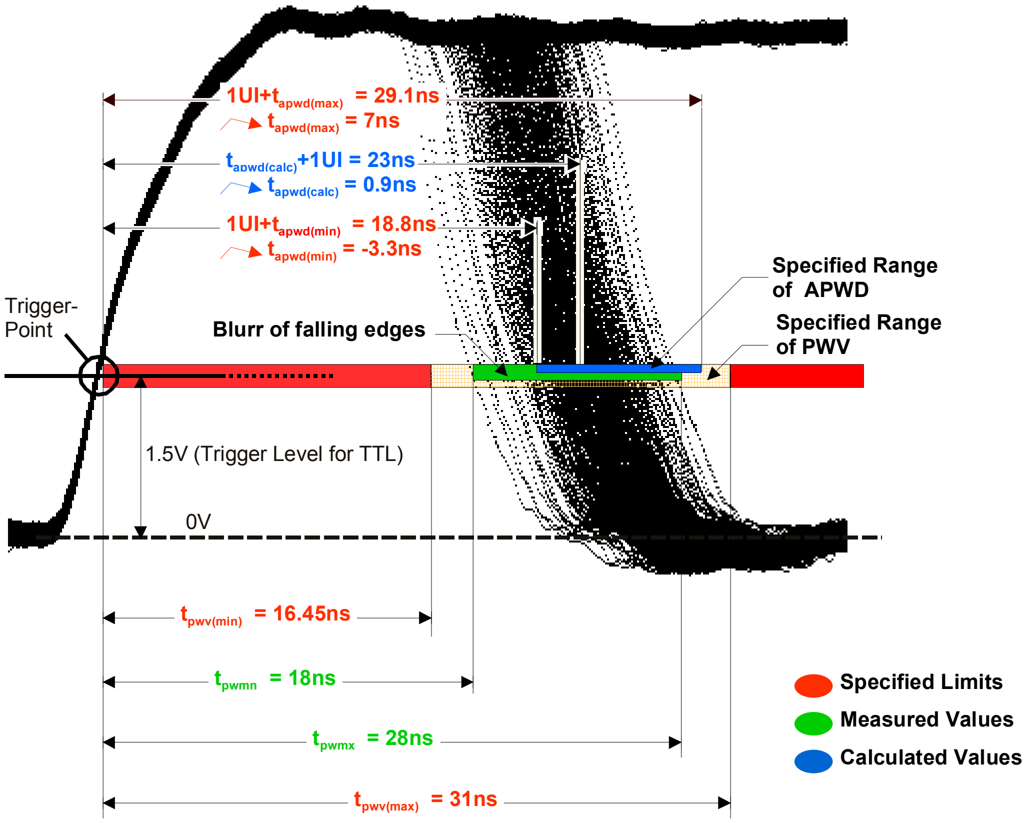


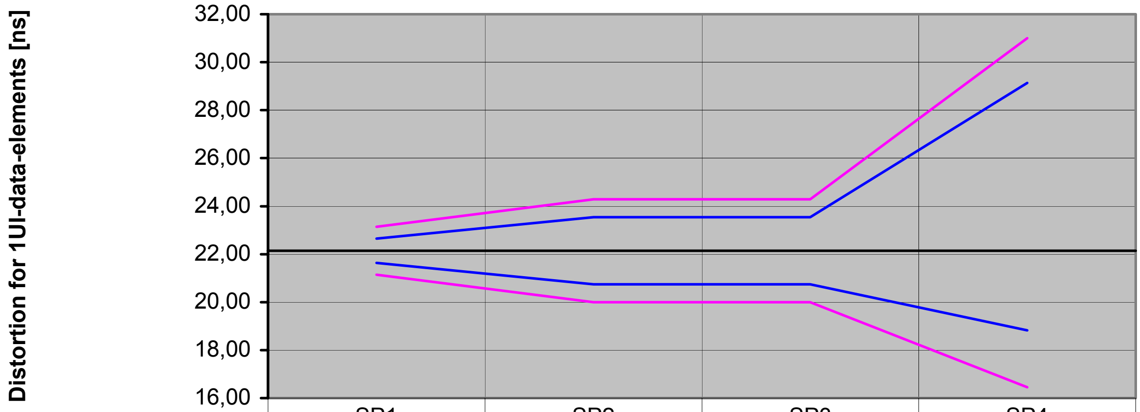
Figure 1-3: Sketch regarding signal distortion (typical signal of SP4 @ FS = 44.1kHz).

	Symbol	Relations	Remarks
1	T_{pwv}	$= t_{pwv(max)} - t_{pwv(min)}$	**P**ulse **W**idth **V**ariation (Specified Range)
2	$t_{pwv(min)}$	**16.45ns**	Lower Limit of specified Range PWV
3	$t_{pwv(max)}$	**31ns**	Upper Limit of specified Range PWV
4	t_{pwmn}	$t_{pwmn} \geq t_{pwv(min)}$ **18ns** ≥ **16.45ns**	Minimum measured Pulse Length **Condition fulfilled**
5	t_{pwmx}	$t_{pwmx} \leq t_{pwv(max)}$ **28ns** ≤ **31ns**	Maximum measured Pulse Length **Condition fulfilled**
6	T_{apwd}	$= t_{apwd(max)} - t_{apwd(min)}$	**A**verage **P**ulse **W**idth **D**istortion (Specified Range)
7	$t_{apwd(min)}$	**-3.3ns (relative to 1/2/3 UI)** **18.8ns**	Lower Limit of specified Range APWD **Absolute number for given example (1UI)**
8	$t_{apwd(max)}$	**+7ns (relative to 1/2/3 UI)** **29.1ns**	Upper Limit of specified Range APWD **Absolute number for given example (1UI)**
9	$t_{apwd(calc)}$	$= (t_{pwmx} + t_{pwmn} - 2UI)/2$ = (**28ns** + **18ns** - 44.28ns)/2 = **0.9ns** $= t_{apwd(min)} \leq t_{apwd(calc)} \leq t_{apwd(max)}$ = **-3.3ns** ≤ **0.9ns** ≤ **7ns**	Calculated APWD based on measurements **Calculated value** **Condition fulfilled**

Table 1-6: Table of example, measured values based on Figure 1-3

Figure 1-4 shows all tolerances of SP1 to SP4 for 1UI at 44.1kHz FS in a graphical manner.

Note: Here and in the following chapters the value of APWD is usually related to the relevant pulse width (1UI, 2UI, 3UI). If so it is named as APWD~! (tAPWD~ = tAPWD + n*UI)



	SP1	SP2	SP3	SP4
tPWV (min)	21,15	20,00	20,00	16,45
tPWV (max)	23,14	24,29	24,29	31,00
tAPWD~ (min)	21,63	20,75	20,75	18,82
tAPWD~ (max)	22,65	23,54	23,54	29,14

Specification Points

Figure 1-4: Tolerance-scheme for SP1 to SP4 regarding signal distortion @ 44.1kHz FS.

1.1.6 Measurement of Phase Variation Parameters

Phase Variations can be interpreted as timing distortion on a single point-to-point link (“Link Jitter”) or from system point as accumulation of all phase variations around the ring (“System Jitter”). The given parameters for the specification points SP1 … SP4 are defining the maximum tolerances for Phase Variation on a single optical link (Link-Jitter). Phase Variation from system point of view is discussed in chapter 3.

The MOST Physical Layer Specification defines three different parameters, which influence the Phase Variation:

Type of Phase Variation	Consequence
Wander	Relevant only on system level (see chapter 3)
Data dependent Jitter (DDJ)	Relevant on link-level and on system-level
Uncorrelated Jitter (UJ)	Relevant on link-level and on system-level

Table 1-7: Summary phase variations.

Operating conditions like temperature, power supply variation and optical input power at OECs influence these parameters.

The given limits for DDJ and UJ are restrictions for an optical link to ensure a proper function of the MOST NIC (MOST Network Interface Controller) following SP4. From system point of view all parts of timing distortion that possibly will accumulate around the network should be kept as small as possible.

The following describes the measurement procedure to measure DDJ and UJ on an optical link.

- The test pattern is generated by a MOST NIC (node) or a pattern-generator.
- The TX of the previous node / pattern-generator is used for triggering.
- The measurements for DDJ and UJ can be taken at SP1 ... SP4

Figure 1-5 shows the test-setup for the measurement of Phase Variation at every specification point SP1…SP4 on a single optical link. The required patterns for DDJ and UJ-measurement are defined in chapter 1.1.4.

Note: Phase Variation has to correspond to that edge of the signal the PLL driven by SP4 does locks to. Phase Variation due to OECs and EOCs may be different on the rising and the falling edge. This means, the transition that is used by the MOST NIC chip for clock recovery, has to be taken into consideration. Therefore the "active edge" has to be defined in the MOST NIC's data sheet.

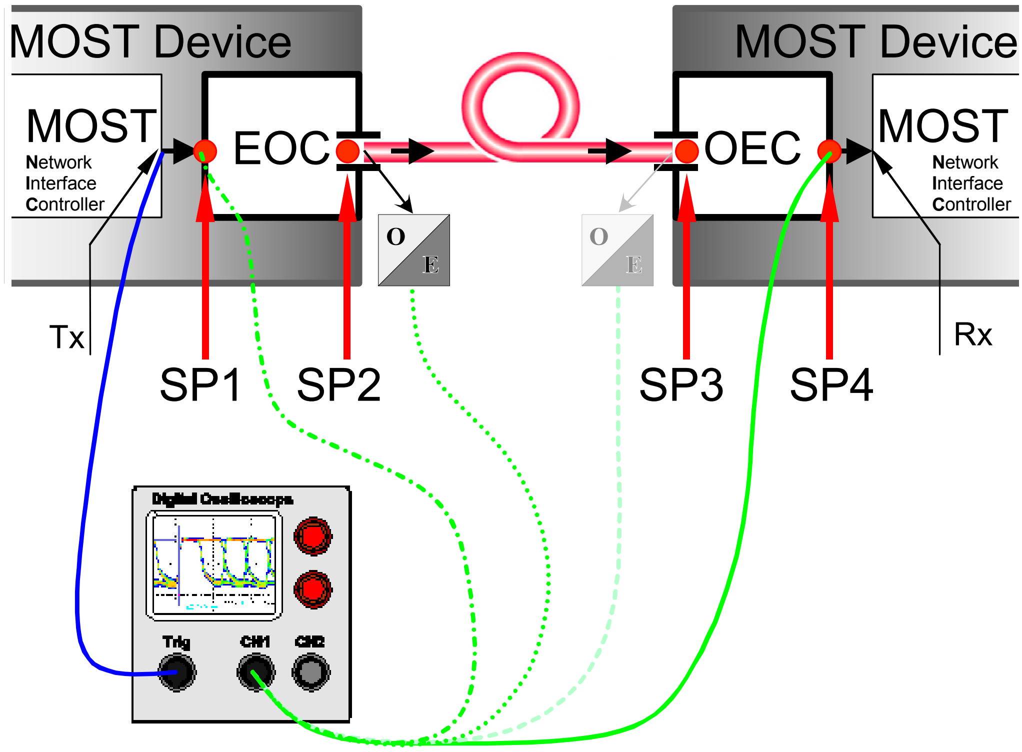


Figure 1-5: Test setup for phase variation measurements for an optical link.

1.1.6.1 Examples for Test Setups Using Real MOST Devices

Test-Setups using real Most devices require a Timing-Master within the test environment in order to generate the required MOST pattern. If the device that contains the SP1- and SP2-interfaces under test is a slave device, the timing master must be placed in front of that slave device (see Figure 1-6 and Figure 1-8 / Figure 1-9). Due to the triggering on TX of the slave device, all Phase Variation from the optical link between Master-node and Slave-node are eliminated from the measurement result. In case SP1 and SP2 for test is included in a Timing Master no additional nodes are needed (see Figure 1-7 and Figure 1-10).

Figure 1-6 shows the setup for a device where the MOST NIC is connected to SP1 is a slave (node x). The test patterns can be routed to the MOST bus either by the timing master or by the test node x itself. Figure 1-8 and Figure 1-9 shows the corresponding setup for measurements on SP4. The measurement setup in Figure 1-8 should be used for link measurements by using two identical slave devices. Figure 1-9 shows the setup for slave nodes using a “known master device” in order to test the behavior from SP3 to SP4 of a slave device.

Figure 1-7 shows the setup for a device were the MOST NIC connected to SP1 is a timing master. The test patterns can only be routed in this MOST NIC. Figure 1-10 shows the corresponding setup for measurement on SP4.

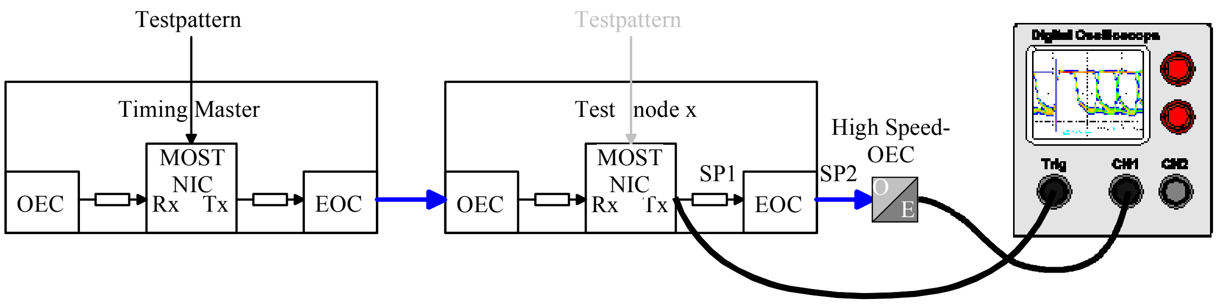


Figure 1-6: Test setup for phase variation measurements at SP2 for slave devices

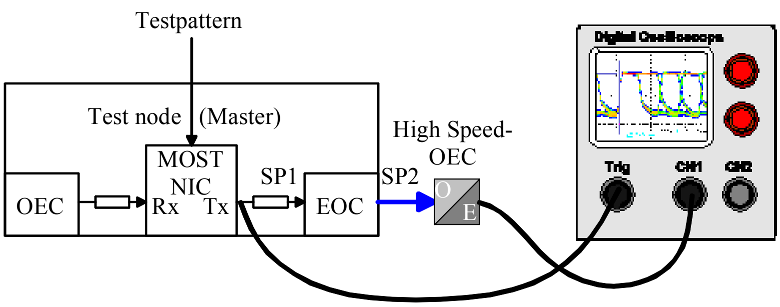


Figure 1-7: Test setup for phase variation measurements at SP2 for master devices

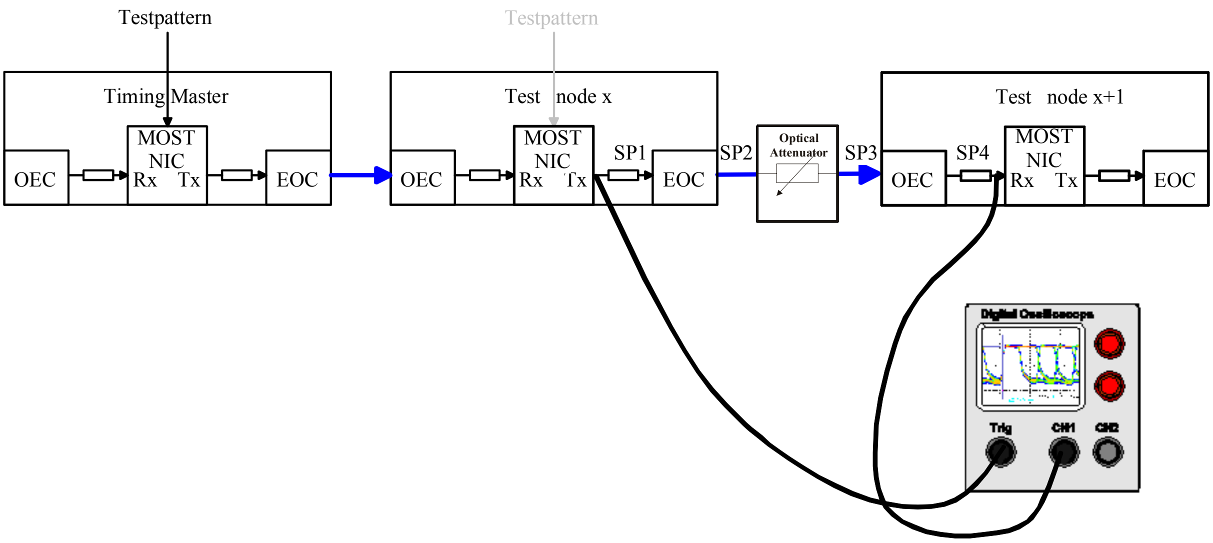


Figure 1-8: Test setup for phase variation measurements at SP4 for slave devices using 1 master and 2 slaves.

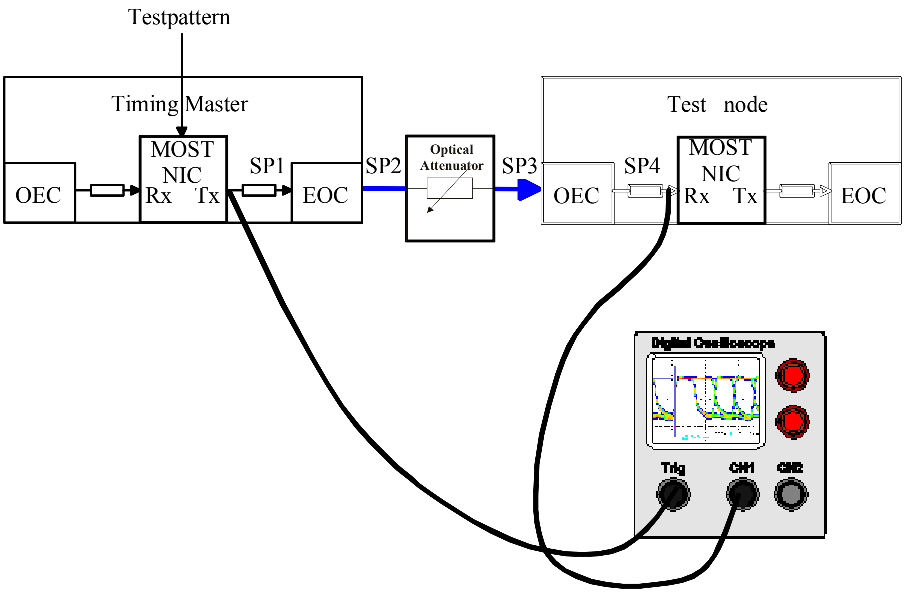


Figure 1-9: Test setup for phase variation measurements at SP4 for slave devices using 1 master and 1 slave.

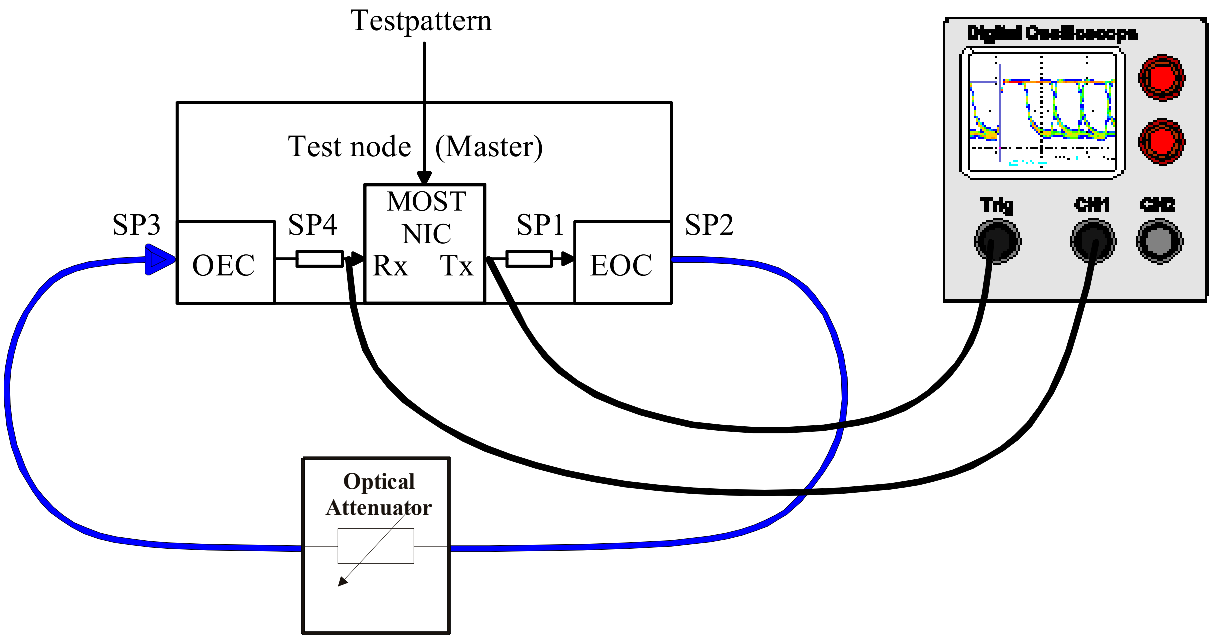


Figure 1-10: Test setup for phase variation measurements at SP4 for master devices

The optical attenuator can be used to adjust the optical input power to the expected level of P_{opt3}.

1.1.6.2 Example for Data Dependent Jitter (Optical Link)

Using a WCDDJ-pattern as test signal like shown in 1.1.4 the histogram measurement shows two humps. Data Dependent Jitter is defined as the distance between the mean-values of that both humps (t_{DDJ}). Figure 1-11 shows an example triggered on Tx(x-1) and measured at SP4(x). A MOST pattern according 1.1.4 (b) was used.

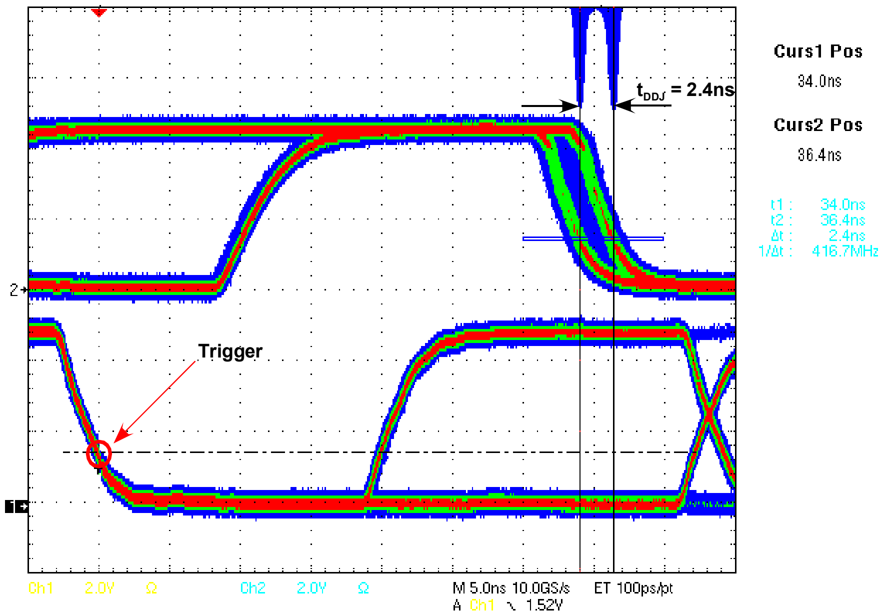


Figure 1-11: Example for data dependent link-jitter @SP4

1.1.6.3 Example for Uncorrelated Jitter (Optical Link)

Using a WCUJ-pattern as test signal like shown in 1.1.4 the histogram measurement shows a single hump. The standard deviation has to be determined. The example Figure 1-12 shows a measurement at SP4 according the definition in the MOST Specification of Physical layer [9]. Figure 1-12 shows an example triggered on Tx(x-1) and measured at SP4(x). A MOST pattern according 1.1.4 (b) was used.

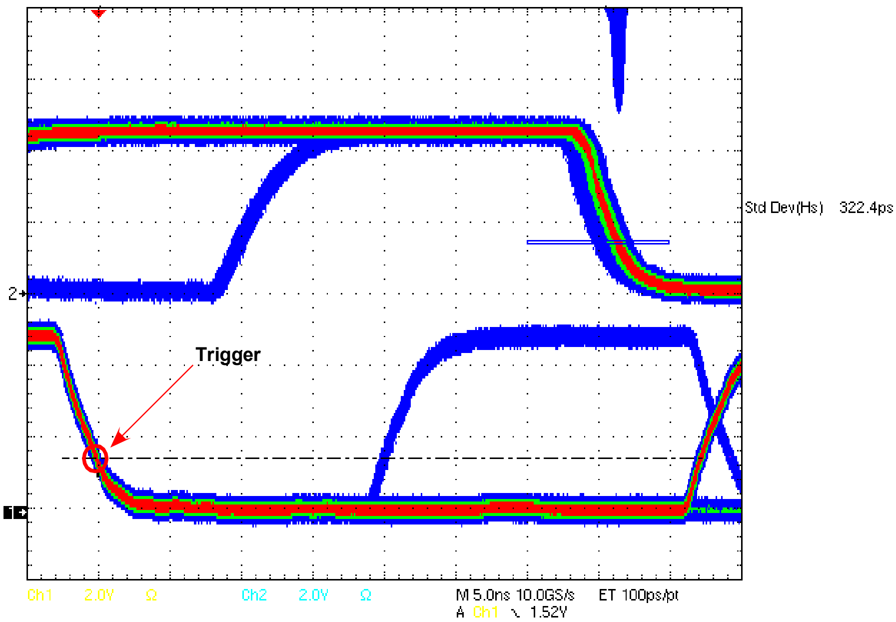


Figure 1-12: Example for uncorrelated link-jitter @SP4

1.1.7 Error Rate

All timing distortion parameters (PWV, APWD, DDJ and UJ for SP1...SP4) of the MOST Specification of Physical Layer [9] are based on a Bit-Error-Rate of 10^{-9}.

1.1.7.1 Pulse-Width-Distortion vs. Error Rate

Pulse-Width-Distortion (PWV and APWD) is defined as a peak-peak value. For a verification of the PWD of a specific pulse-class (1UI, 2UI, 3UI), at least 10^9 pulses have to be acquired. Please note that only one pulse length of the measured pulses is allowed to be outside the specification of PWV or APWD. The required minimum acquisition time depends on the number of elements of the desired pulse class, which are included in a MOST Frame. Due to statistical reasons, actual acquisition time should be longer than the minimum acquisition time.

1.1.7.2 Example for Minimum Acquisition Time

The required minimum acquisition time for each UI is given in Table 1-8, assuming a MOST frame that consists of 50% data bits of value “1” and 50% data bits of value “0” plus one preamble at 44.1kHz FS.

The calculated values are absolute minimum times for the different data elements, when using a measurement method that is able to detect each pulse without any delay between the single acquisitions. Additional delay affected by the measurement-equipment (e.g. the minimum delay of an oscilloscope between two trigger-events) enlarges the total acquisition-time.

Parameters	1UI	2UI	3UI	Unit
Minimum acquisition time	88.6	177.2	22680	s
Minimum acquisition time	1.5	3	378	min

Note:

- A pattern that contains "1" and "0" equally is assumed (a Most frame consists of 512 bits, therefore 256 times “1” and 256 times “0” is transmitted)
- This results in different measurement times for 1UI, 2UI and 3UI
  → 256 times “1” means 256 1UI-elements (high-pulses) / frame
  → 256 times “0” means 128 2UI-elements (high-pulses) / frame
  → 1 preamble means 1 3UI-element (high-pulse) / frame

  The values in the table above correspond to the formula

$$\text{minimum acquistion time} \geq \frac{1}{\left({}^{xUIelement}\!/\!_{frame} \right) \times FS \times ErrorRate}$$

Table 1-8: Table of minimum acquisition time

1.1.7.3 Measurement of PWV vs. Error Rate Using a “Tail Fitting Procedure”

The PWV measurement is specified as a peak-to-peak measurement. Considering the Error Rate requirements this leads to long measurement times (see previous chapter). “Tail fitting” combines histogram-measurement with moderate acquisition time and statistical calculations to achieve a peak-to-peak value for PWV that includes the desired Error Rate.

The histogram in Figure 1-13 is not gaussian, however each edge (left and right) of the histogram can be approximated with a gauss. This is called tail fitting and leads to two gauss functions with two standard deviations and two mean values. A gaussian function is characterized by the standard deviation σ and the mean value *m*. These two parameters characterize the probability density function (PDF), which is well known from the literature.

Theory of Tail fitting
The probability density function (PDF) is given by the formula: $PDF(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(t-m)^2}{2\sigma^2}}$ According to an error rate of >10E-9 this yields to $t \approx m \pm 6\sigma$ Calculation of t_{PWMN} and t_{PWMX}: The mean values m_1 and standard deviation σ_1 of the left gauss yields to $t_{PWMN} = m_1 - 6\sigma_1$ The mean values m_2 and standard deviation σ_2 of the right gauss yields to $t_{PWMX} = m_2 + 6\sigma_2$ $CDF(t) = \int_{-\infty}^{t_{PWMN}} \frac{1}{\sigma_1\sqrt{2\pi}} e^{\frac{-(t-m_1)^2}{2\sigma_1^2}} + \int_{t_{PWMX}}^{+\infty} \frac{1}{\sigma_2\sqrt{2\pi}} e^{\frac{-(t-m_2)^2}{2\sigma_2^2}}$ for a CDF(t) better than 10^{-9}. CDF: Cumulative Density Function

Table 1-9: Theory of tail fitting

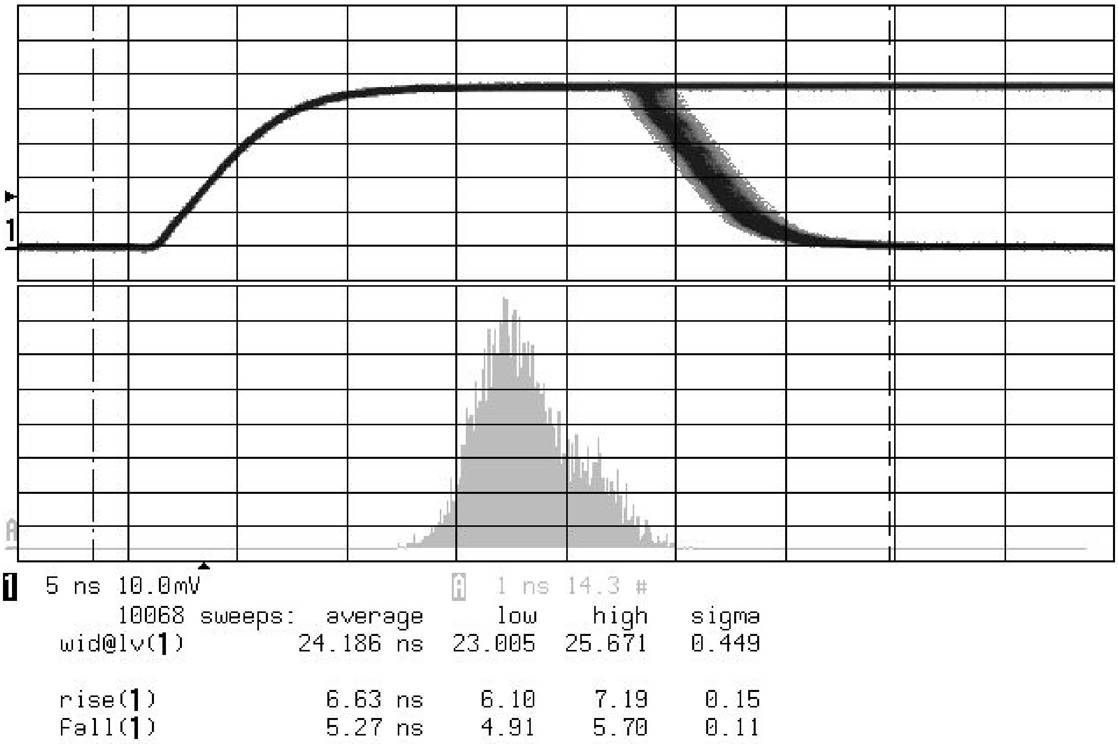


Figure 1-13: PWV histogram measurement

Example:

The plot of the histogram in Figure 1-13 is imported in a computer, which has included a math software with a tail-fitting algorithm. The software determines the two gausses, which approximates the right and the left edge of the histogram and calculated the standard deviations and the mean values. Figure 1-14 shows the original plot in black color, the approximation of the right edge in green color and the approximation of the left edge in orange color.

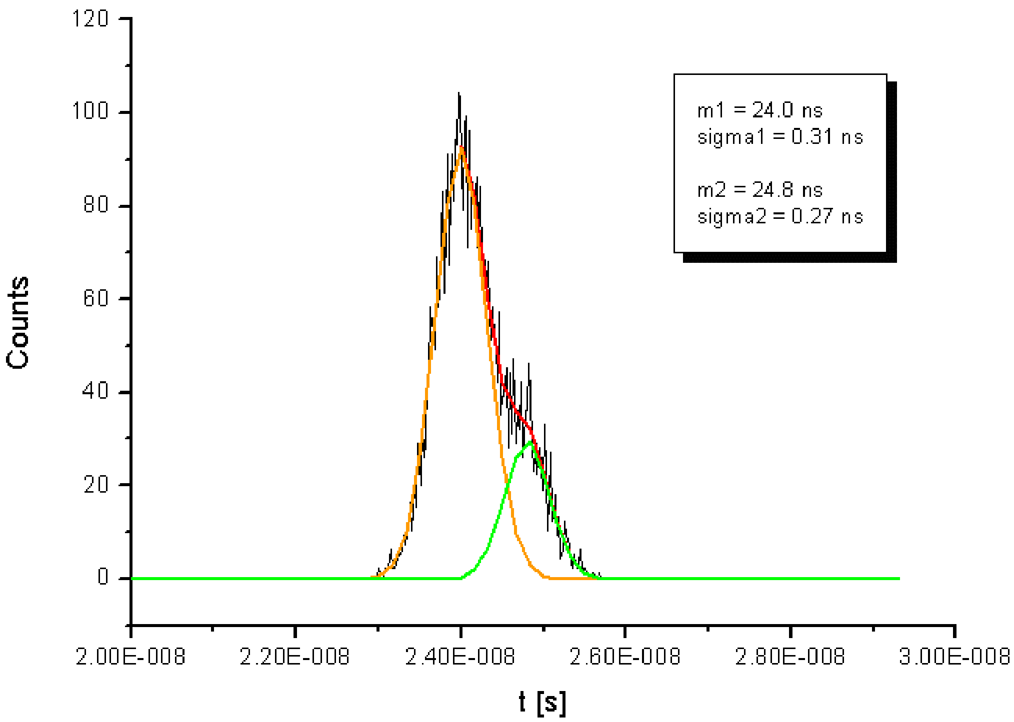


Figure 1-14: PWV histogram

The software calculated for the orange gauss m_1 = *24,0* ns and σ_1 = *0,31* ns. This yields to a t_{PWMN} = *22.14* ns (tpwmn = 24.0ns – 6 x 0.31ns=22.14ns). The software calculated for the green gauss m_2 = *24,8* ns and σ_2 = *0,27* ns. This yields to a t_{PWMX} = *26,42* ns (tpwmx = 24.8ns + 6 x 0.27ns = 26.42ns).

1.2 Measurement Tools

Here are some recommendations that help to select the right measurement tools.

1.2.1 State of the Art Tools

- **Digital oscilloscope:**
  - DSO Type
  - ≥ 2GHz SR
  - BW ≥ 500MHz
  - Fast acquisition time
  - Trigger Jitter: <25ps
  - Gain Accuracy: <2%
  - Histogram function
  - Measurement of Mean Values and Standard Deviation
  - Input filter 200…300MHz (to reduce noise on the High-Speed OEC - signal)
  - Active probe (Cp ≤ 1pF; Rp ≥ 1MOhm)

- **High-speed OEC:**
  - BW: DC to ≥ 250MHz
  - Response flatness: 1dB
    (Constant Gain over BW; linear transfer function over the opt. input range)
  - Wavelength: 650nm
  - Low DC Offset error

- **Optical power meter:**
  - Accuracy: better than +/- 0.25dB
  - Wavelength: 650nm
  - Range: >0dBm ... <-60dBm

- **Ampere meter:**
  - 1µA resolution

- **Function generator:**
  - 0..50kHz rectangle
  - White noise; output level according to the input range of the used ADC

- **Pattern generator if no MOST signal will be used (only for EOC/OEC):**
  - BW 25Mbit
  - PWV/APWD and Jitter requirements according to table Table 2-2 and Table 2-3
  - Generating 1-, 2- and 3-UI signals according to Table 1-2 (a)

- **Optical attenuator:**
  - Attenuation up to 40dB

- **Optical Y – coupler**
  - See chapter 2.3.3

- **Tail fitting SW (option)**
  - See chapter 1.1.7.3

1.2.2 Measurement - Adapter for SP2

The optical power measurement setup is given in Figure 1-15. This measurement adapter allows the test of parameter P_{opt2} under specified requirements (see MOST Specification of Physical Layer [9]).

The optical power at SP2 is transferred by a glass fiber with a numerical aperture of greater than 0.5, a core diameter of 1000 µm and a typical length of 30 mm. An aperture between glass fiber and photo detector confines the transferred beam to the required numerical aperture of 0.5. The size of the aperture is dependant of the distance between glass fiber and the aperture (see Figure 1-16). The accuracy of this measurement setup is at least ±0.3 dB, independent of the Electro Optical Converter (EOC) version. Therefore the end face of the glass fiber must be polished to avoid scattering and a conversion of the beam waist from SP2 to the end of the glass fiber. The glass fiber is mounted into a MOST compatible ferrule, which can be inserted into the MOST device for measuring the optical power at SP2.

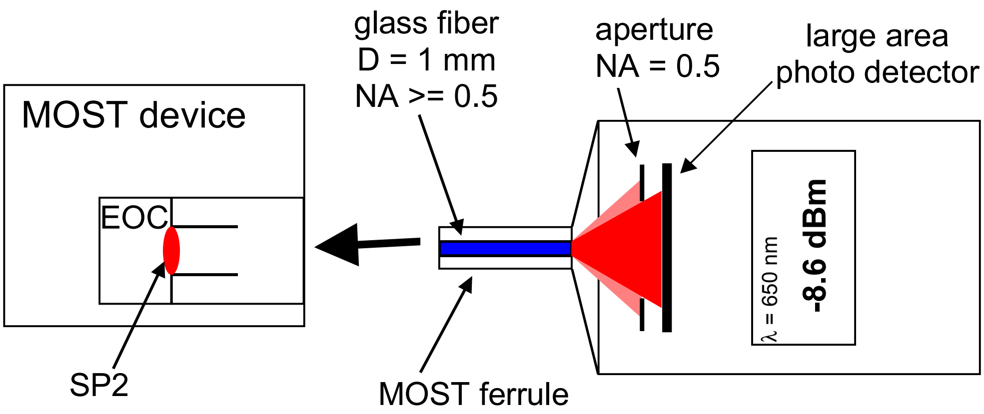


Figure 1-15: Schematic of optical power meter

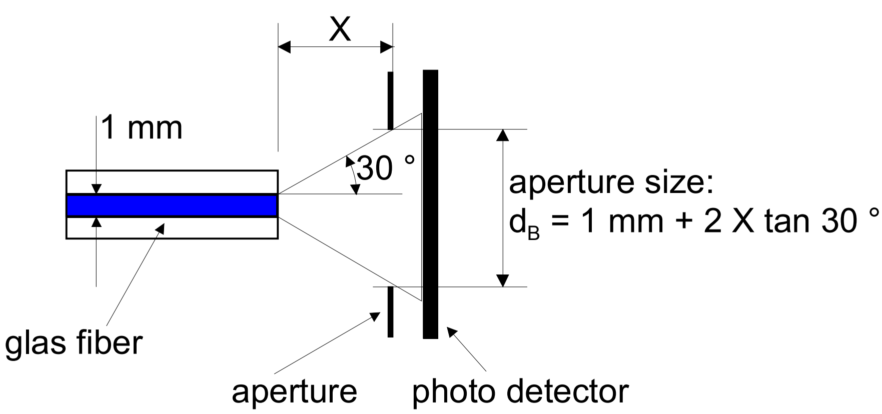


Figure 1-16: Calculation of aperture size d_B

Remark: It should be ensured that the size of the photo detector is big enough to receive all the light after the aperture.

1.2.3 Measurement - Adapter for SP3

The optical power measurement setup is given in Figure 1-17 below. This measurement allows the test of the parameter P_{opt3} under specified requirements (see MOST Specification of Physical Layer [9]).

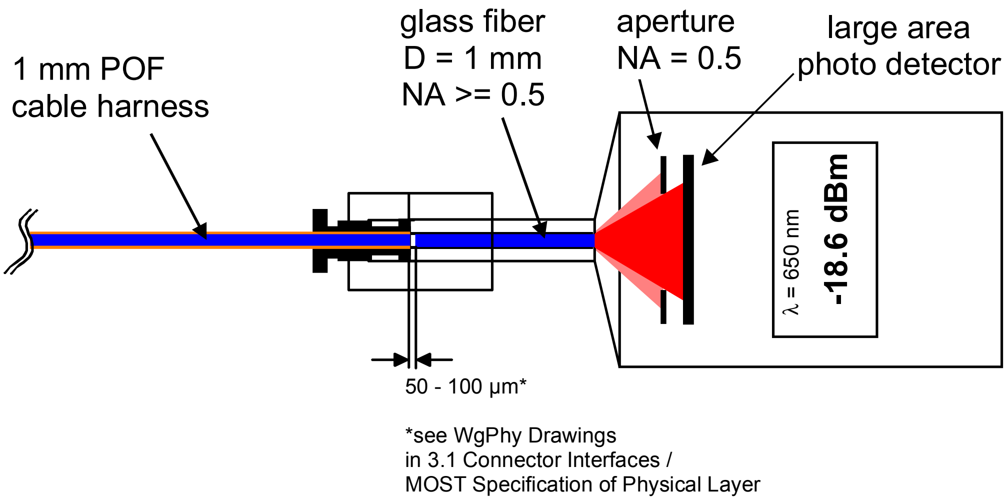


Figure 1-17: Optical power measurement setup for SP3

A glass fiber and an aperture transfer the measured optical power on a large area photo detector (description and aperture calculation see chapter 1.2.2).
In the MOST physical layer specification, P_{opt3} is described as value, when the incoming signal has passed the receiving contact end face. Therefore with the described setup above it is only possible to measure the optical power, which could be ideal coupled in a MOST header. Because of the polished end face of the glass fiber the couple losses are lower compared to the standard used POF (in a MOST header). A designer of a SP3 adapter should take care about this general condition. (Refer also to the MOST Specification of Physical Layer [9], chapter 3.2.2, connector interface loss).
The distance between POF and glass fiber results from the specified WGPhy Drawings.

1.2.4 Additional Measurement Requirements

For slave device - and system measurements a master device is needed where the signals Tx, Rx and RMCK are available.

Timing measurements at SP4 have to be performed considering receivable optical power range for data recovery at SP3.
Therefore a special EOC is required to perform the upper limit of optical input power range. This can be a selected standard EOC, which is able to perform the optical power by keeping the SP2 requirements or a 650nm laser in combination with an attenuator and adequate driving circuits.

2 Parameters of Specification Points

This chapter describes every parameter at every specification point from the standpoint of the MOST compliance that has to be fulfilled by MOST components and MOST devices. Related to each specification point there is a brief introduction of measurement setup and measurement requirements.

Table 2-1 shows all the specified parameters of the MOST physical layer spec. In addition, this table indicates whether the parameters have to be interpreted for inputs, outputs or properties related to hardware components.

Note: Developers of components or modules have to ensure that the outputs of their products fulfill the specification under min/max conditions of their input parameters.

	Parameter to be compliant	MOST NIC	EOC	Optical link	OEC	Device
SP1						
	Bit Rate	Output	Input			
	Logic Levels	Output	Input			
	Fall- / Rise Time	Output	Input			
	Pulse-Width-Variation	Output	Input			
	Average Pulse Width Distortion	Output	Input			
	Data Dependent Link Jitter	Output	Input			
	Uncorrelated Link Jitter	Output	Input			
	Input resistance / -capacitance	1)	Property			
SP2						
	Peak wavelength		Output	Input		Output
	FWHM		Output	Input		Output
	Optical output power		Output	Input		Output
	Optical output power for "light off"		Output	Input		Output
	Extinction ratio		Output	Input		Output
	Fall- / rise-time		Output	Input		Output
	Pulse-Width-Variation		Output	Input		Output
	Average Pulse Width Distortion		Output	Input		Output
	Data Dependent Link Jitter		Output	Input		Output
	Uncorrelated Link Jitter		Output	Input		Output
	Positive /negative overshoot High level signal ripple		Output	Input		Output
SP3						
	Receivable optical power range for data recovery			Output	Input	Input
	Receivable optical power range for switching to "light off state"			Output	Input	Input
	Extinction ratio			Output	Input	Input
	Fall- / rise-time			Output	Input	Input
	Pulse-Width-Variation			Output	Input	Input
	Average Pulse Width Distortion			Output	Input	Input
	Data Dependent Link Jitter			Output	Input	Input
	Uncorrelated Link Jitter			Output	Input	Input
SP4						
	Bit Rate	Input			Output	
	Logic levels	Input			Output	
	Fall- / rise-time	Input			Output	
	Pulse-Width-Variation	Input			Output	
	Average Pulse Width Distortion	Input			Output	
	Data Dependent Link Jitter	Input			Output	
	Uncorrelated Link Jitter	Input			Output	
1) MOST NIC has to drive more than the input capacitance of the EOC						

Table 2-1: Parameters of specification points.

2.1 SP1

For the oscilloscope use an active probe with an input capacitance $C_{Probe} \leq 1pF$ and an input resistance $R_{Probe} \geq 1MOhm$. The ground connection of the probe should be also close to SP1 (GND – pin of EOC).

C_{I1} (10pF max.) and R_{I1} (2kOhm min.) represent the input load of the EOC. The possible capacitance C_{L1} and terminating resistor R_{Term1} of the transmission line between Tx and SP1 depends on the driving capability of Tx.

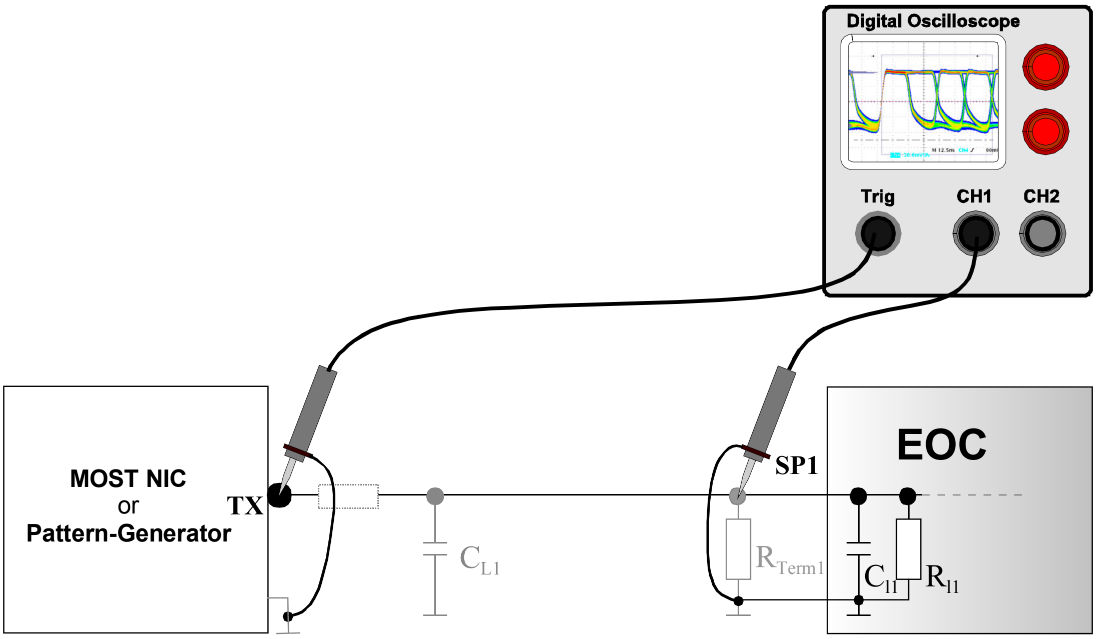


Figure 2-1: Measurement set up for checking the parameters at SP1

Note: Only for the measurement of the phase variation parameters the trigger source is Tx. For all other measurements the trigger source is the signal itself (CH1)!

2.1.1 Bit Rate

It has to be made sure, that all components between SP1 and SP4 are operating reliably within the specified range of bit rate.
Note: Timing parameters have to be ensured only for the nominal Bit rate.

2.1.2 Logic Levels

Belongs to “Low Level Input Voltage V_{IL1}” and “High Level Input Voltage V_{IH1}”. Measurement of this parameters are matter of common knowledge, there is no special recommendation.

2.1.3 Fall and Rise Times

Belongs to “ rise time (10%-90%) t_{r1_10-90}” and “ fall time (90%-10%) t_{f1_90-10}”. Measurement of this parameters are matter of common knowledge, there is no special recommendation. See also note 2 in table 2-1 in MOST Specification of Physical Layer [9].

2.1.4 Pulse-Width-Variation and Average Pulse Width Distortion

Belongs to “Pulse-Width-Variation” tpwv1 and “Average Pulse-Width-Distortion” tapwd1.

Parameters	Symbol	Min.	Max.	Unit
Pulse Width Variation	t_{pwv1}	0.955	1.045	UI
Average Pulse Width Distortion	t_{apwd1}	-0.023	0.023	UI
1UI = 22,14 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv1}	21.15	23.14	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	21.63	22.65	ns
1UI = 20.35 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv1}	19.43	21.26	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	19.88	20.81	ns
2UI = 44,29 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv1}	43.29	45.29	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	43.78	44.80	ns
2UI = 40,69 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv1}	39.77	41.61	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	40.22	41.16	ns
3UI = 66,43 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv1}	65.44	67.43	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	65.92	66.94	ns
3UI = 61,04 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv1}	60.12	61.95	ns
Average Pulse Width Distortion	$t_{apwd1\sim}$	60.57	61.50	ns
Note: All measurements at 1,5 Volt based on ERROR RATE requirements (see 1.1.7 Error Rate). $t_{apwd1\sim} = t_{apwd} + n*UI$				

Table 2-2: Pulse width distortion values at SP1

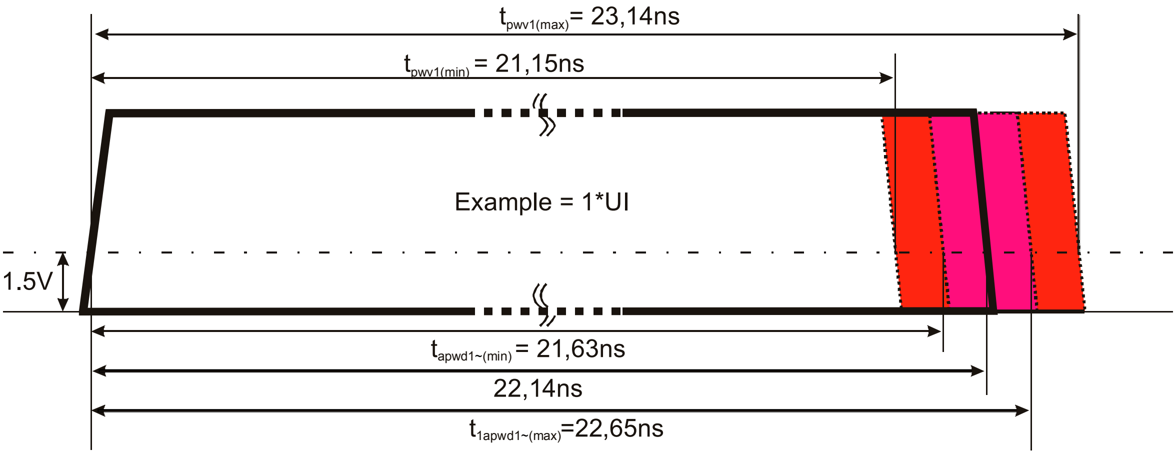


Figure 2-2: Sketch regarding signal distortion parameters at SP1 based on FS=44.1 kHz

2.1.5 Data Dependent Jitter and Uncorrelated Jitter

These measurements can be relinquished if there are no components between the Tx output of the MOST NIC and SP1, high-speed design rules are obeyed and if the requirements of 2.1.2, 2.1.3 and 2.1.4 for SP1 are met.

In practice the signals for Tx and SP1 are identical regarding jitter. However, a general measurement setup is given in chapter 1.1.6.

Parameters	Symbol	Min.	Max.	Unit
Data Dependent Link Jitter	t_{DDJ1}	-	0.01	UI
Uncorrelated Link Jitter	t_{UJ1}	-	0.0045	UI
@ FS 44.1 kHz				
Data Dependent Link Jitter	t_{DDJ1}	-	0.22	ns
Uncorrelated Link Jitter	t_{UJ1}	-	0.10	ns
@ FS 48.0 kHz				
Data Dependent Link Jitter	t_{DDJ1}	-	0.20	ns
Uncorrelated Link Jitter	t_{UJ1}	-	0.09	ns

Table 2-3: Phase variation limits at SP1

2.1.6 Input Resistance and Input Capacitance

Belongs to “Input resistance R_{I1}” and “Input capacitance C_{I1}”. These are properties of SP1 that have to be guaranteed by the EOC supplier.

Measurement of input capacitance CI1:

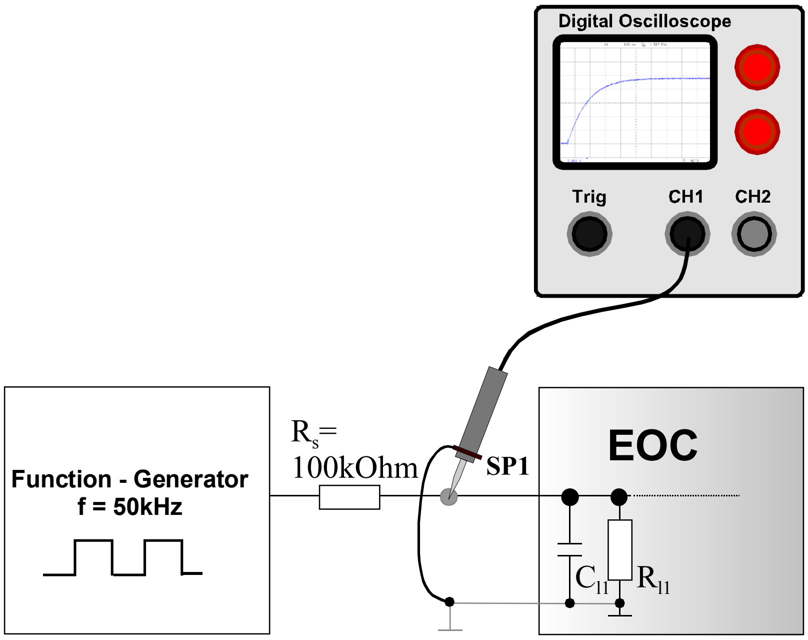


Figure 2-3: Measurement setup for input capacitance C_{I1}

The pins GND, Vcc and Rext should have the recommended operating voltages.

The data pin is connected to the function generator in series with a 100kOhm resistor. The used signal of the function generator has a frequency of 50 kHz and has a square waveform. The high and low level input voltage should have the recommended operating voltage. The rise and fall time of the signal has to be smaller than 1 ns and the capacity of the active probe has to be smaller than 1pF. The digital oscilloscope shows the saturation curve of C_{I1}.

The saturation curve yields to the time constant τ. τ is the difference of t1 and t0. t0 is at the start of the curve and t1 is the time when the curve has reached a value of 63% of the end value. The following screen shot shows τ.

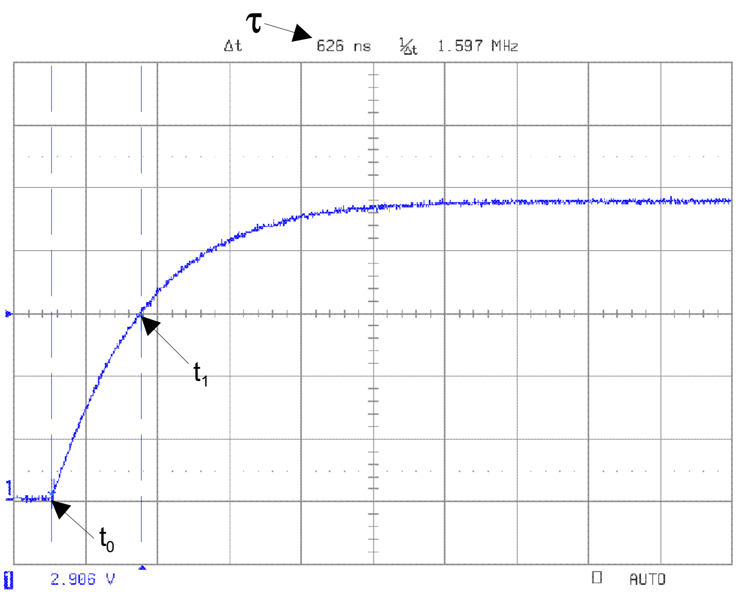


Figure 2-4: typical charge characteristic of C_{I1}

Then the following formula yields to the capacitance C_{I1}.

$$C_{I1} = \frac{\tau}{R}$$

The example above yields to C_{I1} = 6.6 pF.

Measurement of R_{I1}:

The input resistance is measured at 0V and VDD of the EOC as input voltage divided by the leakage current (by using a high-sensitive ampere meter according to Figure 2-5.)

$R_{I1} = VCC/I_{leak1} - Ri_{amp}$

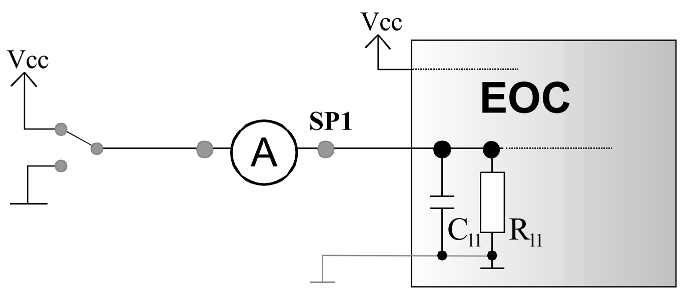


Figure 2-5: Measurement setup for input resistance of R_{I1}

2.2 SP2

To measure the timing characteristics on SP2 a high-speed optical-electrical converter is needed. The setup and its requirements are shown in Figure 2-6. The passive optical components (fiber, connectors) for measuring the dynamic parameters should have low attenuation based on the requirements of the used High-Speed OEC.
To measure the optical output power an optical power meter is required. The setup and its requirements are shown in Figure 2-7.

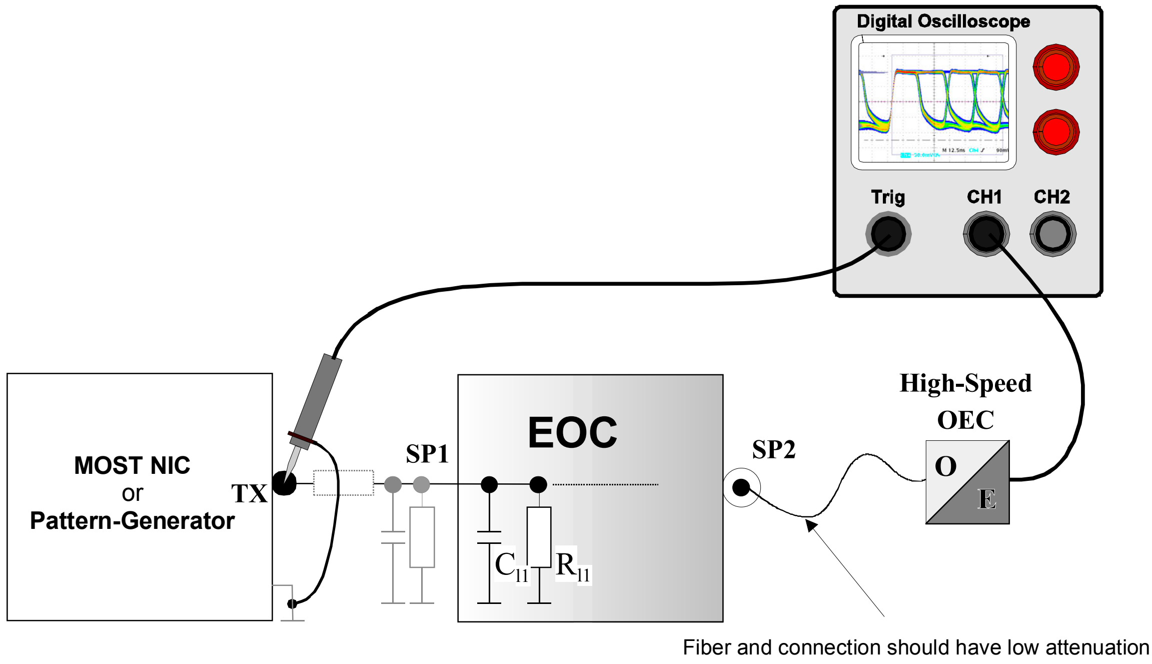


Figure 2-6: Measurement setup for dynamic parameters at SP2

Note: Only for the measurement of the phase variation parameters the trigger source is Tx. For all other measurements the trigger source is the signal itself (CH1)!
Please note also that High-Speed OECs itself generate noise that causes random jitter. For jitter measurements the jitter due to the High-Speed OEC should be subtracted.

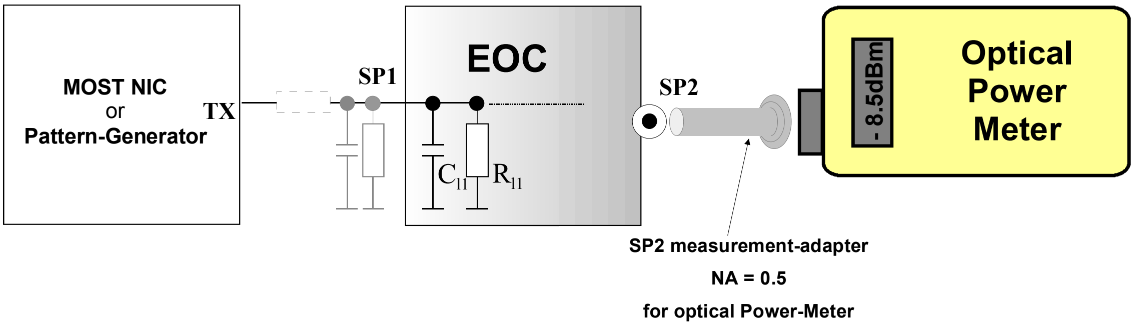


Figure 2-7: Measurement setup for optical power parameters at SP2

2.2.1 Bit Rate

It has to be made sure, that all components between SP1 and SP4 are operating reliably within the specified range of bit rate.
Note: Timing parameters have to be ensured only for the nominal Bit rate.

2.2.2 Peak Wavelength

Belongs to "Peak Wavelength λ_2". Measurement of this parameter is matter of common knowledge for suppliers of optical components and therefore has to be guaranteed by the EOC supplier.

2.2.3 Full Width at Half Maximum (FWHM)

Belongs to "FWHM $\Delta\lambda_2$". Measurement of this parameter is matter of common knowledge for suppliers of optical components and therefore has to be guaranteed by the EOC supplier.

2.2.4 Optical Output Power

Belongs to " Optical output power P_{opt2}". The measurement setup is given in Figure 2-7. In addition refer to 1.2.2 for the measurement adapter. In combination with an optical power meter, this adapter allows the measurement of P_{opt2} under specified requirements (see MOST Specification of Physical Layer [9] Table 2-2).

2.2.5 Optical Output Power for "Light Off"

Belongs to " Optical output power 'Light Off' P_{OFF2}". Measurement setup is given in Figure 2-7. In addition refer to 1.2.2 for the measurement adapter. In combination with an optical power meter, this adapter allows the measurement of P_{opt2} under specified requirements (see MOST Specification of Physical Layer [9] Table 2-2).

2.2.6 Extinction Ratio

Belongs to "Extinction Ratio r_{e2}". Measurement setup is given in Figure 2-6. Extinction ratio is calculated based on "Optical High Level b1" and "Optical Low Level b0" as described in Figure 2-8

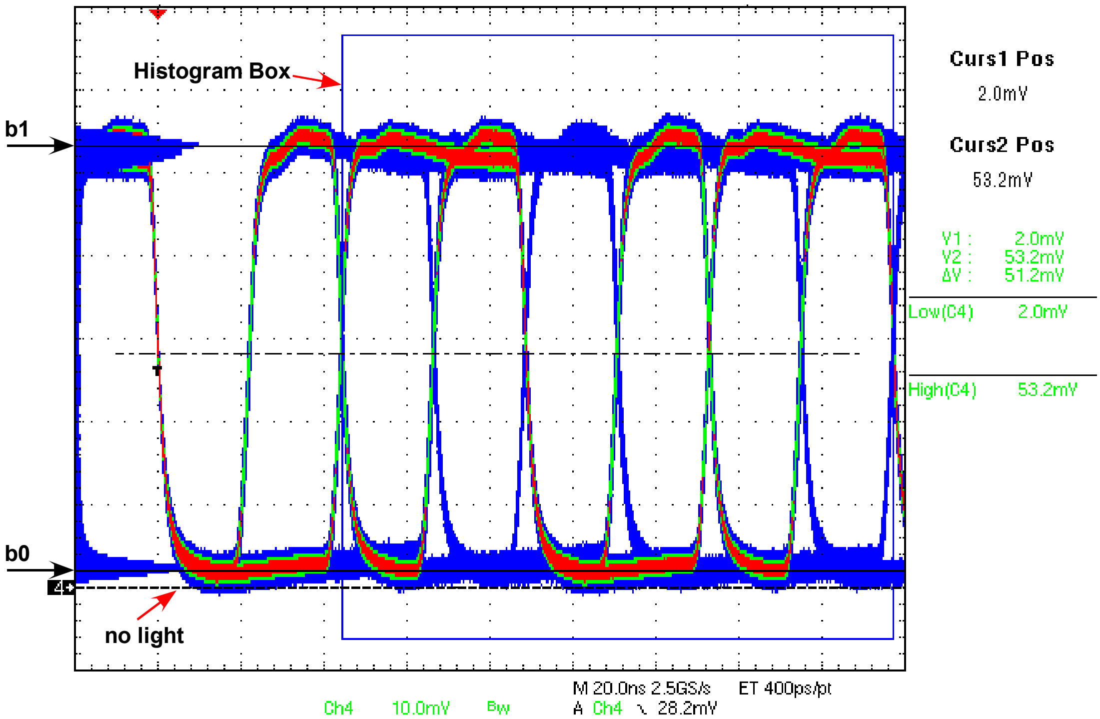
	Symbol	Relations	Remarks
1	r_{e2}	= 10 log (b1/b0)	Extinction Ratio
2	b0		Optical Low Level, see Figure 2-8
3	b1		Optical High Level, see Figure 2-8
Note: All Parameters described in EN/IEC 61280-2-2			

Table 2-4: Parameter for extinction ratio

For evaluation of b0 and b1 use a vertical histogram as shown in Figure 2-8 and described in EN/IEC 61280-2-2.

A WCPWV-pattern has to be used in order to determine the Extinction Ratio. The measurement of b1 and b0 is triggered off an edge of the measured signal itself. The setting of the oscilloscopes time-scale has to assure that at least 3UI are considered. The Histogram box in Figure 2-8 shows an example containing 6UIs.

Note: Detection of the acquired levels (especially b0) requires high accuracy; otherwise parameters derived from b1-/b0-levels will get inaccurate. This measurement assumes using very low DC offset O/E converter with unity gain over the specified BW (DC to ≥250MHz) or relative measurement minimizing DC offset errors.



r_e = 10 * log(b1/b0)
r_e = 10 * log(53.2mV/2mV)
r_e = 14.25dB

Figure 2-8: Example for vertical histogram to evaluate b1 and b0

2.2.7 Fall and Rise Times

Belongs to " rise time (20%-80%) t_{r2_20-80}" and " fall time (80%-20%) t_{f2_80-20}". The fall and rise time is referenced to 20% / 80% of the real optical amplitude (b1-b0). Measurement setup is given in Figure 2-6.

2.2.8 Pulse-Width-Variation and Average Pulse Width Distortion

Belongs to "Pulse-Width-Variation" t_{pwv2} and "Average Pulse-Width-Distortion" t_{apwd2}. Measurement setup is given in Figure 2-6.

Parameters	Symbol	Min.	Max.	Unit
Pulse Width Variation	t_{pwv2}	0.903	1.097	UI
Average Pulse Width Distortion	t_{apwd2}	-0.063	+0.063	UI
1UI = 22,14 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv2}	20.00	24.29	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	20.75	23.54	ns
1UI = 20.35 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv2}	18.37	22.32	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	19.06	21.63	ns
2UI = 44,29 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv2}	42.14	46.44	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	42.89	45.68	ns
2UI = 40,69 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv2}	38.72	42.66	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	39.41	41.97	ns
3UI = 66,43 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv2}	64.28	68.58	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	65.04	67.83	ns
3UI = 61,04 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv2}	59.06	63.01	ns
Average Pulse Width Distortion	$t_{apwd2\sim}$	59.75	62.32	ns
Note: All measurements at 50% of signal amplitude based on ERROR RATE requirements (see 1.1.7 Error Rate). $t_{apwd1\sim} = t_{apwd} + n*UI$				

Table 2-5: Pulse width distortion values at SP2

2.2.9 Data Dependent Jitter and Uncorrelated Jitter

Belongs to “Data Dependent Jitter” t_{DDJ2} and “Uncorrelated Jitter” t_{UJ2}. Measurement setup is given in Figure 2-6. The both parameters have to be measured using the dedicated test pattern as defined in chapter 1.1.4. A description of the measurement procedure is given in chapter 1.1.6.

Parameters	Symbol	Min.	Max.	Unit
Data Dependent Link Jitter	t_{DDJ2}	-	0.035	UI
Uncorrelated Link Jitter	t_{UJ2}	-	0.015	UI
@ FS 44.1 kHz				
Data Dependent Link Jitter	t_{DDJ2}	-	0.78	ns
Uncorrelated Link Jitter	t_{UJ2}	-	0.33	ns
@ FS 48.0 kHz				
Data Dependent Link Jitter	t_{DDJ2}	-	0.71	ns
Uncorrelated Link Jitter	t_{UJ2}	-	0.31	ns

Table 2-6: Phase variation limits at SP2.

2.2.10 Positive and Negative Overshoot

The positive Overshoot occurs at the rising edge of the signal. Negative Overshoot occurs at the falling edge of the signal. The value in percent of the positive / negative overshoot is related to the difference of the signal amplitudes b1-b0. The absolute location of the positive and negative overshoot is related to the absolute location of the levels b1 and b0 (see Figure 2-9)

Measurement setup is given in Figure 2-6. For evaluation of b0 and b1 use a vertical histogram as shown in Figure 2-8 and described in EN/IEC 61280-2-2.

2.2.11 High Level Signal Ripple

The High-level signal ripple is defined in the range of 2/3UI and 3/4UI. The value in percent of the High-level signal ripple is related to the difference of the signal amplitudes b1-b0. The absolute location of the High-level signal ripple is related to the absolute location of the level b1 (see Figure 2-9)

Measurement setup is given in Figure 2-6. For evaluation of b0 and b1 use a vertical histogram as shown in Figure 2-8 and described in EN/IEC 61280-2-2.

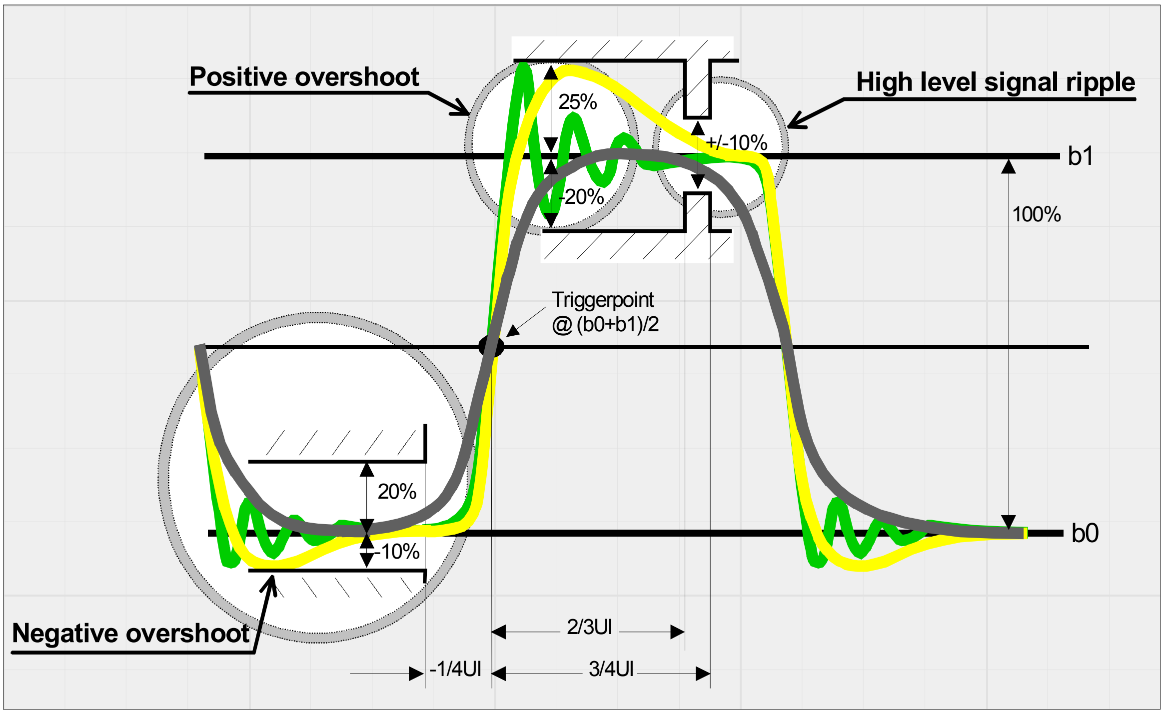


Figure 2-9: Schematics of optical pulses at specification point 2.

2.3 SP3

The measurement of the dynamic parameters at SP3 at low optical input power is associated with big effort. However, the dynamic parameters of SP3 are very similar to SP2 and will not change significantly when using an optical link (harness). In general, optical links are passive linear systems and should be well-known regarding their bandwidth-length product. Therefore, it is sufficient to measure dynamic parameters at SP2. In addition to system considerations of the optical link, the values at SP3 can be calculated.

The measurement of the optical power at SP3 is mandatory. Figure 2-10 shows the measurement setup for measuring the optical power at SP3.

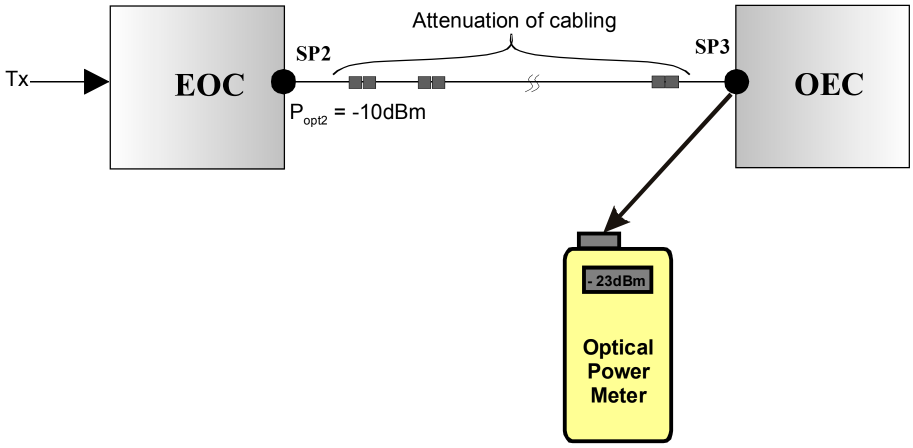


Figure 2-10: Measurement setup for optical power parameters at SP3

2.3.1 Bit Rate

It has to be made sure, that all components between SP1 and SP4 are operating reliably within the specified range of bit rate.
Note: Timing parameters have to be ensured only for the nominal Bit rate.

2.3.2 Receivable Optical Power Range for Data Recovery

Belongs to "Receivable optical power range for data recovery P_{opt3}". The adapter of the Optical Power Meter has to look like a (female) MOST connector. The measurements in 2.4.4 and 2.4.5 take care for this parameter.

2.3.3 Receivable Optical Power Range for Switching to "Light Off State"

Belongs to “Receivable optical power range for switching to “light off state” P_{OFF3}”. The measurement setup has to be configured in the same manner as a MOST connector at SP3. This influences the design of the adapter between harness and an Optical Power Meter.
Figure 2-11 shows the sketch of the measurement setup. EOC 1 and EOC 2 are MOST compliant EOCs, which transmit a modulated biphase code signal. The Source can be switched either to EOC1 or to EOC2. An Optical Summing Unit (Y – Coupler) sums the optical signals of EOC1 and EOC2 to SP3.
If the source is switched to EOC1 the optical power at the end of the fiber (SP3) should be attenuated by the optical attenuator 1 down to P_{opt3} min (-23dBm).
The optical power of EOC 2 at the end of the fiber (SP3) can be varied by the optical attenuator 2. If the source is switched to EOC2 then the power on SP3 has to be P_{Off3} min (-40 dBm). The test is fulfilled if the OEC (DUT) switches to low power mode when the source is switched to EOC2 and switches ON when the source is switched to EOC 1.
The ON/OFF - status can be measured on the /STATUS output of the OEC.

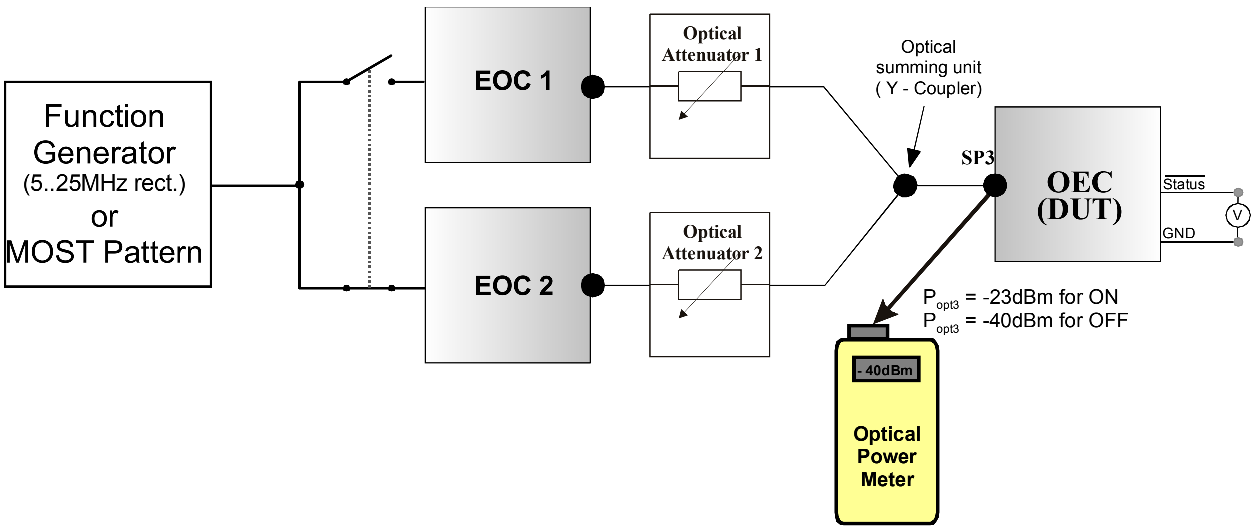


Figure 2-11: Measurement setup for optical output power for light off.

2.3.4 Extinction Ratio

Belongs to “Extinction Ratio r_{e3}”. Extinction ratio is calculated based on “Optical High Level b1” and “Optical Low Level b0” as described in Table 2-4. There is no difference between r_{e2} on SP2 and r_{e3} on SP3, because the influence of the attenuation is linear to all optical amplitudes.

2.3.5 Rise and Fall Time

Due to the limited bandwidth of optical links, rise- and fall-time may increase. Therefore, there is a difference in the values of rise- and fall-time between SP2 and SP3.

The bandwidth-length-product of selected materials must be taken into consideration by developers of optical harnesses. This helps to avoid an increase of the rise and fall-times larger than the difference between SP2 and SP3.

Developers of OECs have to ensure the performance of their product under worst-case input parameters, in detail rise- and fall-time of SP3.

2.3.6 Pulse-Width-Variation and Average Pulse Width Distortion

Belongs to “Pulse-Width-Variation” t_{pwv3} and “Average Pulse-Width-Distortion” t_{apwd3}. There are no differences between SP2 and SP3 regarding PWV and APWD.

Parameters	Symbol	Min.	Max.	Unit
Pulse Width Variation	t_{pwv3}	0.903	1.097	UI
Average Pulse Width Distortion	t_{apwd3}	-0.063	+0.063	UI
1UI = 22,14 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv3}	20.00	24.29	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	20.75	23.54	ns
1UI = 20.35 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv3}	18.37	22.32	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	19.06	21.63	ns
2UI = 44,29 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv3}	42.14	46.44	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	42.89	45.68	ns
2UI = 40,69 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv3}	38.72	42.66	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	39.41	41.97	ns
3UI = 66,43 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv3}	64.28	68.58	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	65.04	67.83	ns
3UI = 61,04 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv3}	59.06	63.01	ns
Average Pulse Width Distortion	$t_{apwd3\sim}$	59.75	62.32	ns
Note: All measurements at 50% of signal amplitude based on ERROR RATE requirements (see 1.1.7 Error Rate). $t_{apwd1\sim} = t_{apwd} + n*UI$				

Table 2-7: Phase variation limits at SP3.

2.3.7 Data Dependent Jitter and Uncorrelated Jitter

Belongs to “Data Dependent Jitter” t_{DDJ3} and “Uncorrelated Jitter” t_{UJ3}. DDJ does not change from SP2 to SP3 since the optical bandwidth is very high. It is very difficult to measure jitter at low optical input power, since High-Speed OECs itself generate lots of random noise at low optical input power. Therefore the measurement of DDJ and UJ on SP2 takes care also for SP3. A separate measurement is not necessary.

Parameters	Symbol	Min.	Max.	Unit
Data Dependent Link Jitter	t_{DDJ3}	-	0.035	UI
Uncorrelated Link Jitter	t_{UJ3}	-	0.015	UI
@ FS 44.1 kHz				
Data Dependent Link Jitter	t_{DDJ3}	-	0.78	ns
Uncorrelated Link Jitter	t_{UJ3}	-	0.33	ns
@ FS 48.0 kHz				
Data Dependent Link Jitter	t_{DDJ3}	-	0.71	ns
Uncorrelated Link Jitter	t_{UJ3}	-	0.31	ns

Table 2-8: Phase variation limits at SP3.

2.4 SP4

The signal performance at SP4 mainly depends on the optical input power at SP3. Therefore the limits on SP4 must be guaranteed over the optical input range on SP3. Figure 2-12 shows the required test setup for SP4. The load given by C_L=10pF (max. value) and R_L = 50kOhm (min. value) includes the input load of the MOST NIC and the load of the wiring on the PCB.

For the oscilloscope use an active probe with an input capacitance $C_{Probe} \leq$ 1pF and an input resistance $R_{Probe} \geq$ 1MOhm. The ground connection of the probe should be also close to SP4 (ground of C_L and R_L).

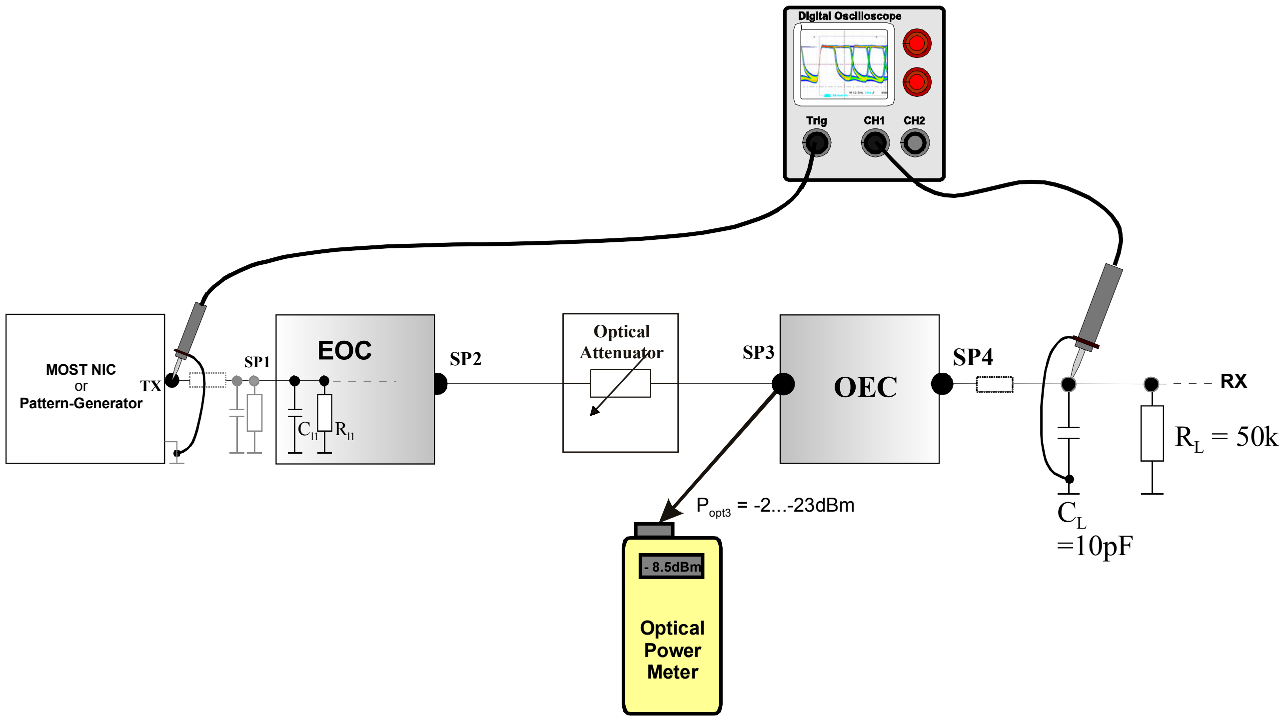


Figure 2-12: Measurement setup for optical output power for light off.

Note: Only for the measurement of the Jitter parameters the trigger source is Tx. For all other measurements the trigger source is the signal itself (CH1)!

Note: The SP4 is defined as the output of the OEC, but in reality other parameters like trace impedance, trace length, or signal termination can affect the signal condition that has to be taken into consideration for the measurement!

2.4.1 Bit Rate

It has to be made sure, that all components between SP1 and SP4 are operating reliably within the specified range of bit rate.
Note: Timing parameters have to be ensured only for the nominal Bit rate.

2.4.2 Logic Levels

Belongs to "Low Level Input Voltage V_{IL4}" and "High Level Input Voltage V_{IH4}". Measurement of this parameters are matter of common knowledge, there is no special recommendation.

2.4.3 Rise / Fall Time

Belongs to " Rise time (10%-90%) $t_{r4\_10\text{-}90}$" and " fall time (90%-10%) $t_{f4\_90\text{-}10}$". Measurement of these parameters is a matter of common knowledge; there is no special recommendation. See also note 2 in table 2-4 in MOST Specification of Physical Layer [9].

2.4.4 Pulse-Width-Variation and Average Pulse Width Distortion

Belongs to "Pulse-Width-Variation" t_{pwv4} and "Average Pulse-Width-Distortion" t_{apwd4}. The parameters have to be within the specified limits over the receivable optical power range P_{opt3} specified in SP3.

Parameters	Symbol	Min.	Max.	Unit
Pulse Width Variation	T_{pwv4}	0.743	1.40	UI
Average Pulse Width Distortion	t_{apwd4}	-0.15	0.316	UI
1UI = 22,14 ns @ FS 44.1 kHz				
Pulse Width Variation	T_{pwv4}	16.45	31.00	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	18.82	29.14	ns
1UI = 20.35 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv4}	15.12	28.48	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	17.29	26.77	ns
2UI = 44,29 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv4}	38.60	53.15	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	40.97	51.29	ns
2UI = 40,69 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv4}	35.46	48.83	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	37.64	47.12	ns
3UI = 66,43 ns @ FS 44.1 kHz				
Pulse Width Variation	t_{pwv4}	60.74	75.29	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	63.11	73.43	ns
3UI = 61,04 ns @ FS 48 kHz				
Pulse Width Variation	t_{pwv4}	55.81	69.17	ns
Average Pulse Width Distortion	$t_{apwd4\sim}$	57.98	67.46	ns
Note: All measurements at 1,5 Volt based on ERROR RATE requirements (see 1.1.7 Error Rate). $t_{apwd1\sim} = t_{apwd} + n{*}UI$				

Table 2-9: Phase variation limits at SP4.

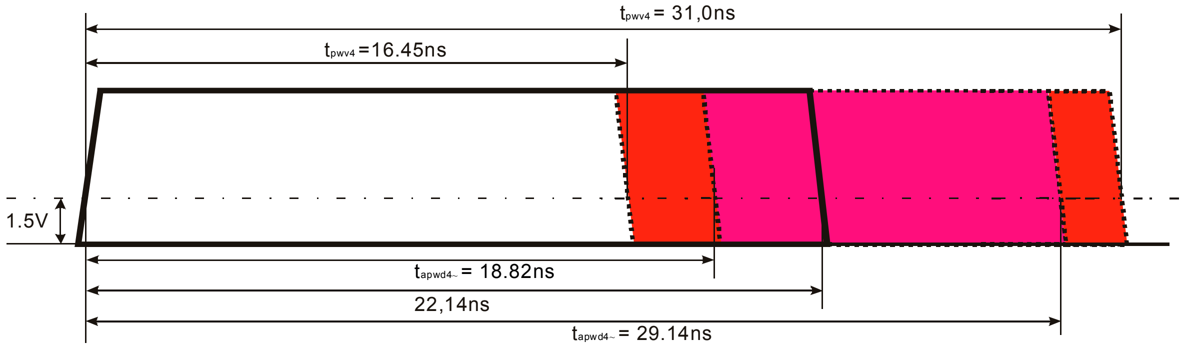


Figure 2-13: Sketch regarding signal distortion parameters at SP4 based on FS=44.1 kHz.

2.4.5 Data Dependent Jitter and Uncorrelated Jitter

Belongs to “Data Dependent Jitter” t_{DDJ4} and “Uncorrelated Jitter” t_{UJ4}. Measurement setup is given in Figure 1-8 and Figure 1-10. The both parameters have to be measured using the dedicated test pattern as defined in chapter 1.1.4. A description of the measurement procedure is given in chapter 1.1.6.

Parameters	Symbol	Min.	Max.	Unit
Data Dependent Link Jitter	t_{DDJ4}	-	0.15	UI
Uncorrelated Link Jitter	t_{UJ4}	-	0.045	UI
@ FS 44.1 kHz				
Data Dependent Link Jitter	t_{DDJ4}	-	3.32	ns
Uncorrelated Link Jitter	t_{UJ4}	-	1.00	ns
@ FS 48.0 kHz				
Data Dependent Link Jitter	t_{DDJ4}	-	3.05	ns
Uncorrelated Link Jitter	t_{UJ4}	-	0.92	ns

Table 2-10: Phase variation limits at SP4.

3 Accumulated Jitter

In order to achieve system integrity according to paragraph 2.6 of the MOST Specification of Physical Layer [9] the following formula must be kept from a system.

Master-Jitter-Tolerance
The requirements for the system-design are combined in the formula below:
$$\text{M-Jitter-Tol.} \geq \sum_{n=1}^{m} t_W(n) + \sum_{n=1}^{m-1} t_{DDJacc}(n) + \sum_{n=1}^{m-1} t_{UJacc}(n) + t_{DDJ}(m) + t_{UJ}(m)$$
M – Jitter – Tol.*:* Jitter Tolerance of the NIC in the master device ***m:*** Number of nodes/optical links in a Ring **$t_W(n)$:** Wander (Phase Drift) per node and optical link **$t_{DDJacc}(n)$:** Accumulated Data Dependent Jitter per node to node (Tx(n-1)→Tx(n) **$t_{UJacc}(n)$:** Accumulated part of Uncorrelated Jitter per node to node (Tx(n-1)→Tx(n) **$t_{DDJ}(m)$:** Data Dependent Jitter of the last link **$t_{UJ}(m)$:** Uncorrelated Jitter of the last link
The sum of $t_{DDJ}(m)$ and $t_{UJ}(m)$ is the Link-Jitter between last Slave TX and SP4 of the Timing-Master.

Table 3-1: Relationship of system jitter parameters

The Master – Jitter tolerance is a property of the used MOST NIC in the master device and has to be depicted in the corresponding data sheet.

3.1 Additional Test Signals and Requirements

In addition to the test patterns mentioned in 1.1.4 some more test patterns/signals needs to be defined for tests on system level:

TSW: Test Signal For Wander
The TSW should exist by only one frequency in order to suppress data dependent effects as much as possible. Therefore it could be identical with WCUJ described in 1.1.4.3.

RMCKm: RMCK @ Master
The RMCK at the master is needed for jitter measurements for big rings and has to be set to typically 64FS (→ 2.8224MHz). By using this signal the measurable accumulated jitter is about 170ns @ 44.1kHz * FS.

RMCKls: RMCK @ last Slave
The RMCK at the last slave is also needed for big ring measurements and has to be set to typically 64FS (→ 2.8224MHz). By using this signal the measurable accumulated jitter is about 170ns @ 44.1kHz * FS.

The Timing Master device must be prepared that the Tx/Rx signal and the RMCKm signal can be measured. The last slave must be prepared to measure Tx and RMCKls.

Important: It has to be taken into consideration that the measurements will require special modes of test software in the timing master device and the last slave device especially to support the required signals above!

3.2 System Measurements

There are several ways to evaluate phase variations on system level. The following chapters describe examples of possible measurement methods in order to clarify the meaning of the specified parameters.

3.2.1 Measurement of System Wander

According to formula term: $\left[\sum_{n=1}^{m} W(n)\right]$

Wander is mainly caused by temperature drift of the used components in the chain of the MOST signal. Additional effects like drift of the power supply of the components can cause additional wander. Figure 3-1 shows the measurement setup for measuring wander.

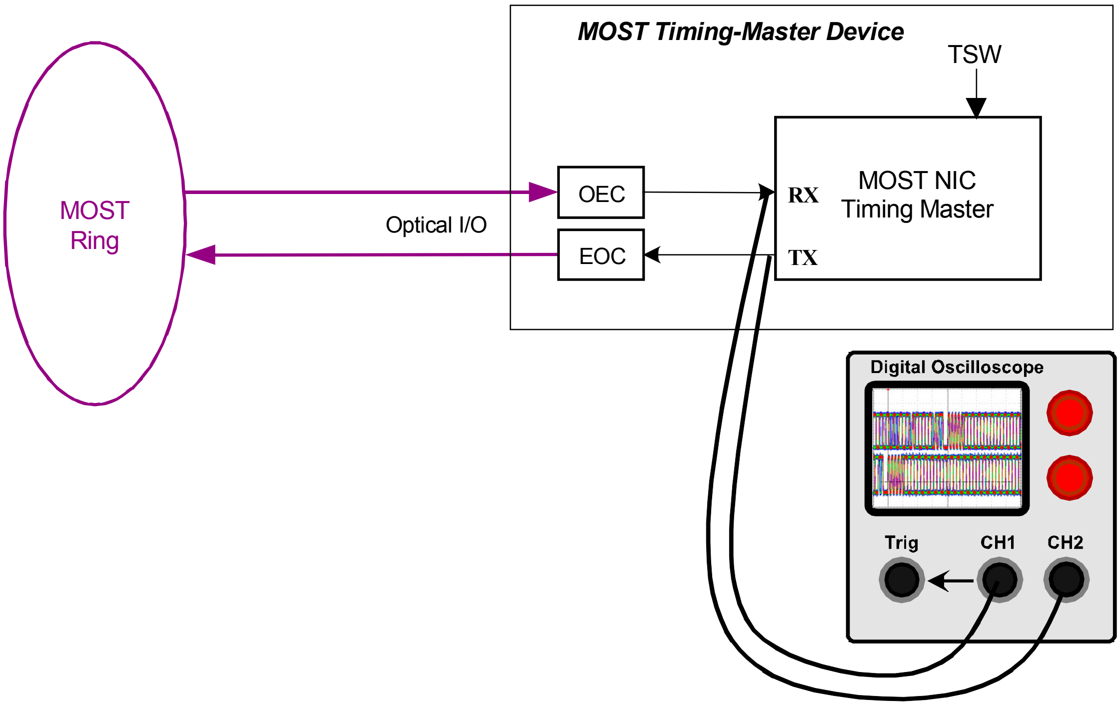


Figure 3-1: Measurement setup for wander

The steps to measure wander are the follows:

1. Put all the devices into a climatic chamber and connect the ring. The network should be structured as close as possible to the real system (e.g. power budget, sequence of devices).
2. Connect probes on the timing master according to Figure 3-1
3. Trigger on a preamble of Tx. Triggering on a preamble can be achieved by triggering on high- or low-pulses of >60ns, because only preambles contain 3UI-elements (3 * 22.14ns = 66.42ns @ 44.1kHz FS).
4. Cool down to lower border of the specified temperature range
5. Start system by using the TSW for the MOST signal
6. Measure delay from Tx to Rx preamble according to Figure 3-2
7. Increase temperature stepwise (e.g. 10 degree steps).
8. The delay between RX and TX will change. Measure the new delay from TX- to RX-preamble at each temperature step.
9. Wander is the difference between initial delay (step 6) and current delay (see Figure 3-3).
10. Repeat step 7 to 9 until the upper temperature limit is reached.
11. Determine the maximum wander from all measurements.

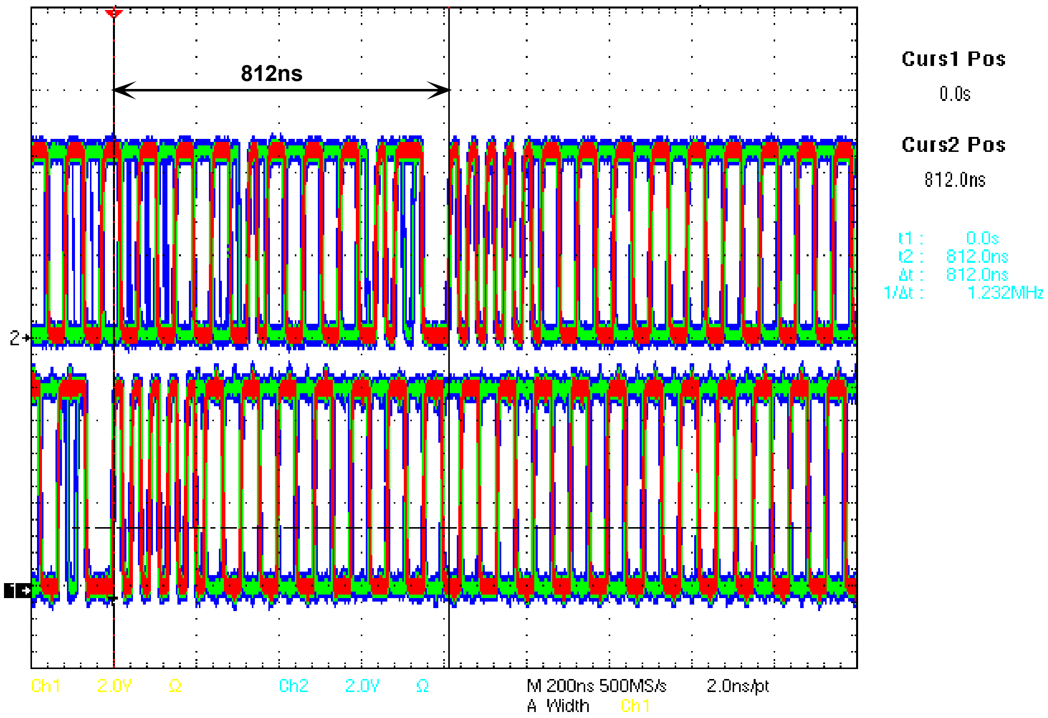


Figure 3-2: Delay at start of measurement

Measuring Delay: Trigger on a preamble-element (3UI high-pulse or 3UI low-pulse) of Tx (channel 1 in Figure 3-2) and place one cursor to a preamble of the Rx signal (channel 2).
After this Preamble has reached it's new position place the 2nd cursor to that position and measure the difference of the two positions (see Figure 3-3).

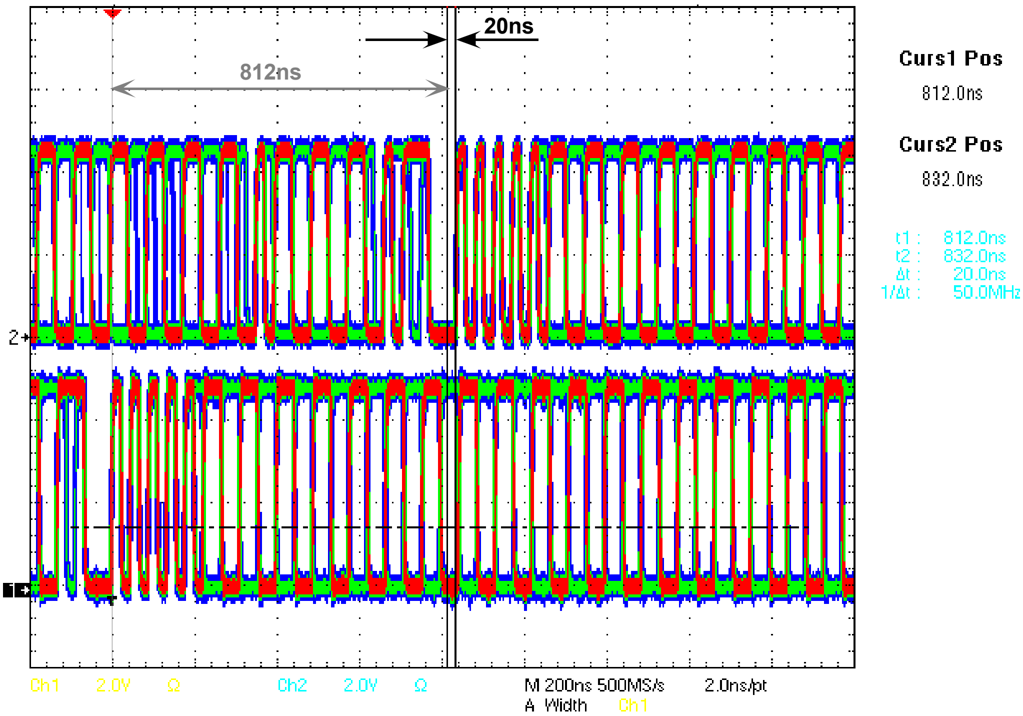


Figure 3-3 Delay at end of measurement

Note: The phase of the preamble can change if unlocks occur during measurement!

3.2.2 Measurement of Total DDJ and UJ

Jitter up to about 0.75UI (16.5ns @ 44.1kHz FS) can be measured directly at Rx triggered off Tx of the timing master, because the eye-diagram on Rx is still open. Therefore this kind of measurement can be used only for systems were system jitter is expected to be small. The setup is the same as shown in Figure 3-1. Instead of TSW use the corresponding test signals for UJ and DDJ.

The sum of DDJ and UJ corresponds to the term:

$$\sum_{n=1}^{m-1} t_{DDJacc}(n) \;+\; \sum_{n=1}^{m-1} t_{UJacc}(n) \;+\; t_{DDJ}(m) \;+\; t_{UJ}(m).$$

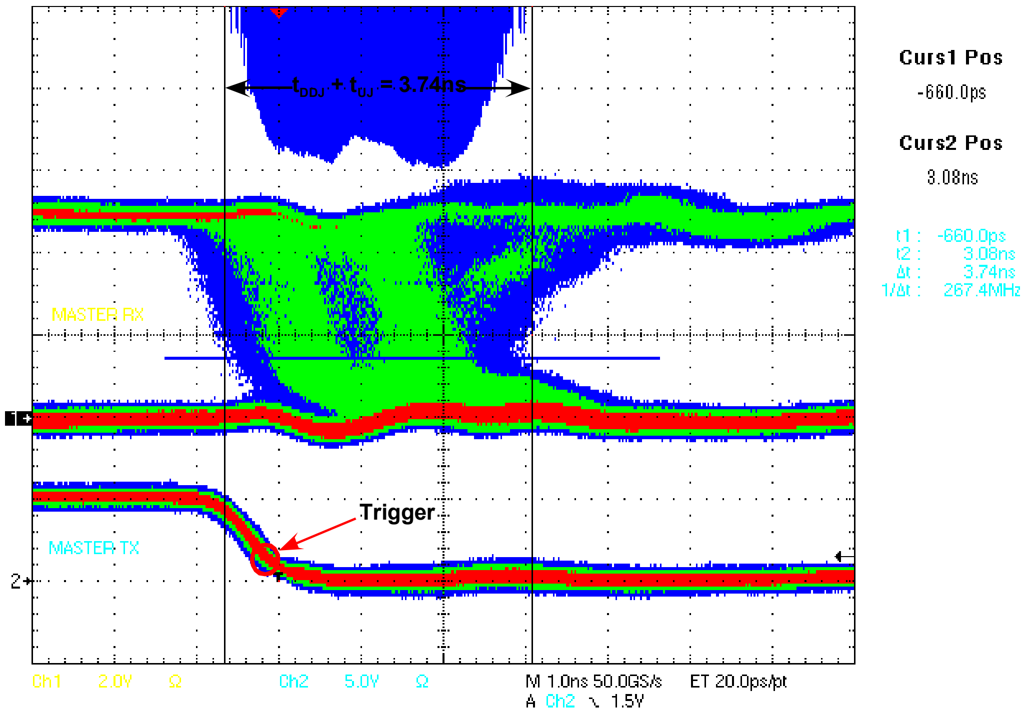


Figure 3-4: Measurement of Tx-to-Rx peak-to-peak jitter at the timing master

Due to overlaid rising and falling edges it is not easy to determine the exact amount of jitter. In addition it is nearly impossible to distinguish between data-dependent jitter of the rising and falling edges. Therefore this measurement is suited for quick results in a laboratory environment.
However, if this measurement already shows that the amount of system jitter doesn't exceed the master-jitter tolerance the complex measurements shown in chapter 3.2.3 do not need to be done.

3.2.3 Split Measurement of Accumulated DDJ and UJ

Jitter beyond 0.75UI (16.5ns @ 44.1kHz FS) can be determined indirectly by measuring the accumulated part up to the last slave node and add the measured jitter of the last link.

3.2.3.1 Worst-Case Measurement of DDJ+UJ up to the Last Slave Node

As illustrated in Figure 3-5 the scope is triggered off the RMCK from the MOST timing-master device (RMCKm) and the peak-to-peak jitter on the RMCK of the last timing-slave (RMCKls) is observed. RMCK signals can be used for all jitter measurements. The RMCK has the same phase variation properties like Tx, because they both originate from the same PLL clock. RMCKm and RMCKls must be set to the same frequency (64*FS to 512*FS).

The sum of DDJ and UJ corresponds to the term:

$$\sum_{n=1}^{m-1} t_{DDJacc}(n) \quad + \quad \sum_{n=1}^{m-1} t_{UJacc}\ (n)$$

of the formula in Table 3-1 and is measured as follows:

1. Put all the devices into a climatic chamber and connect the ring. The network should be structured as close as possible to the real system (e.g. power budget, sequence of devices).
2. Prepare the timing master according to Figure 3-5.
3. Heat-up the devices to the upper limit of the specified temperature range (this is usually the worst-case for jitter). Wait until new temperature has settled and there is no influence due to Wander.
4. Start system by using the WCDDJ pattern for the MOST signal.
5. Measure the peak-to-peak jitter of RMCKls according to Figure 3-6. The acquisition time for the measurement has to consider the BER requirement!

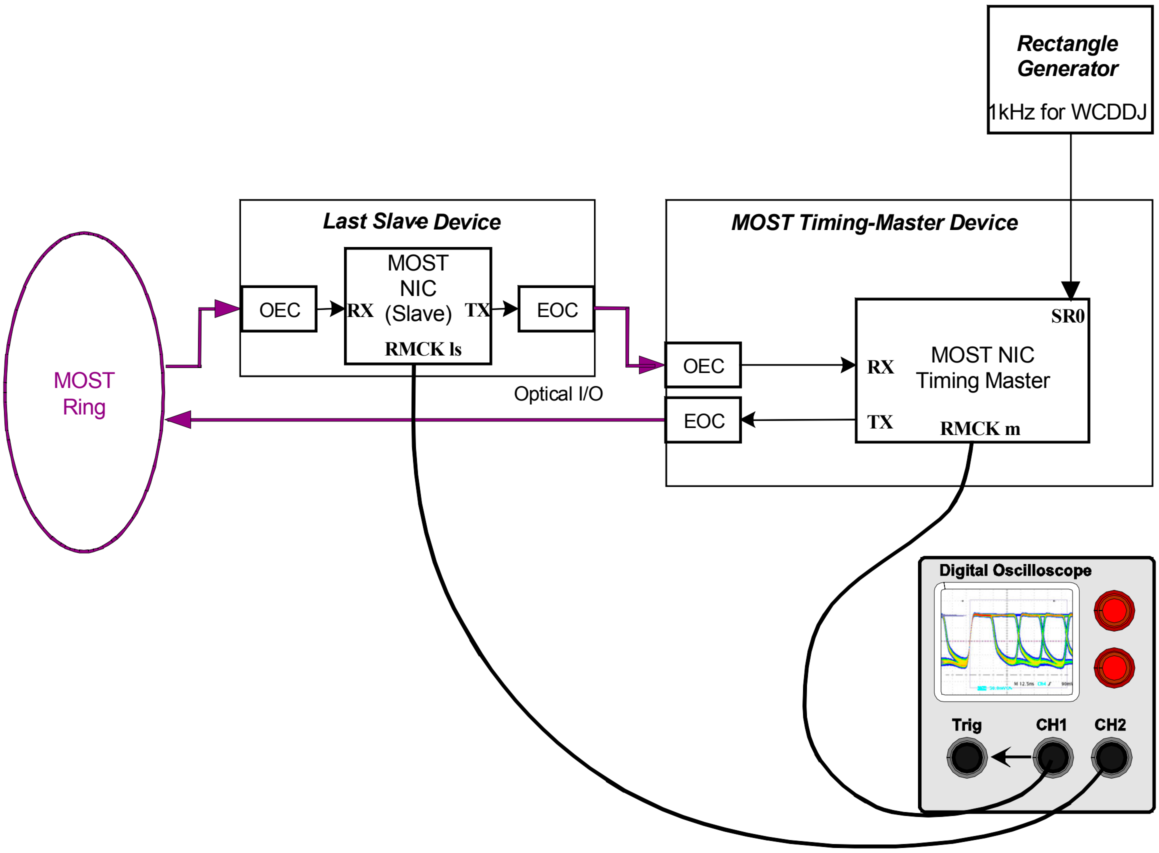


Figure 3-5: Measurement setup for accumulated DDJ and UJ

Figure 3-6 illustrates the measurement of the sum of accumulated DDJ and UJ up to Tx of the last slave node. Channel 1 is the (edge) trigger source of the RMCK of the master (RMCKm). Channel 2 is the signal RMCKls. The histogram shows the peak-to-peak value of the accumulated jitter up to the last slave.

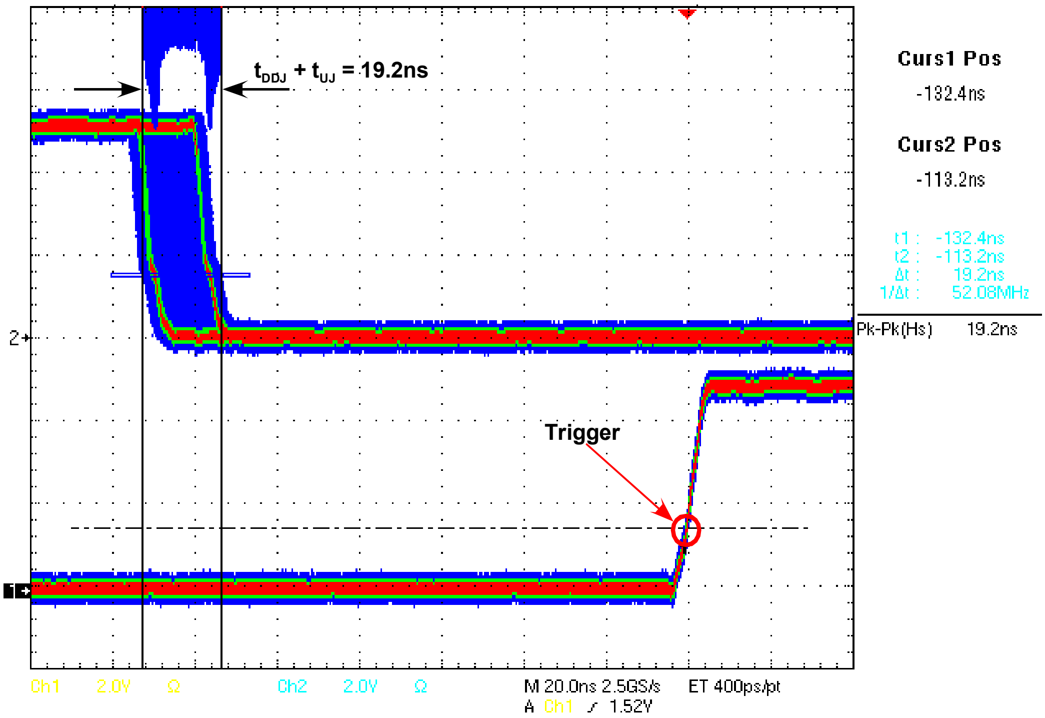


Figure 3-6: Measurement of DDJ plus UJ (peak-to-peak)

3.2.3.2 Measurement of Link Jitter Between Last Slave and Master

According to formula term:

$$DDJ\ (m)\ +\ UJ\ (m)$$

the measurement of the last link jitter is identical with the measurements which have to be done for SP4 based on Tx of the device before. The measurement has to be done at the last link. See also chapter 1.1.6.1.

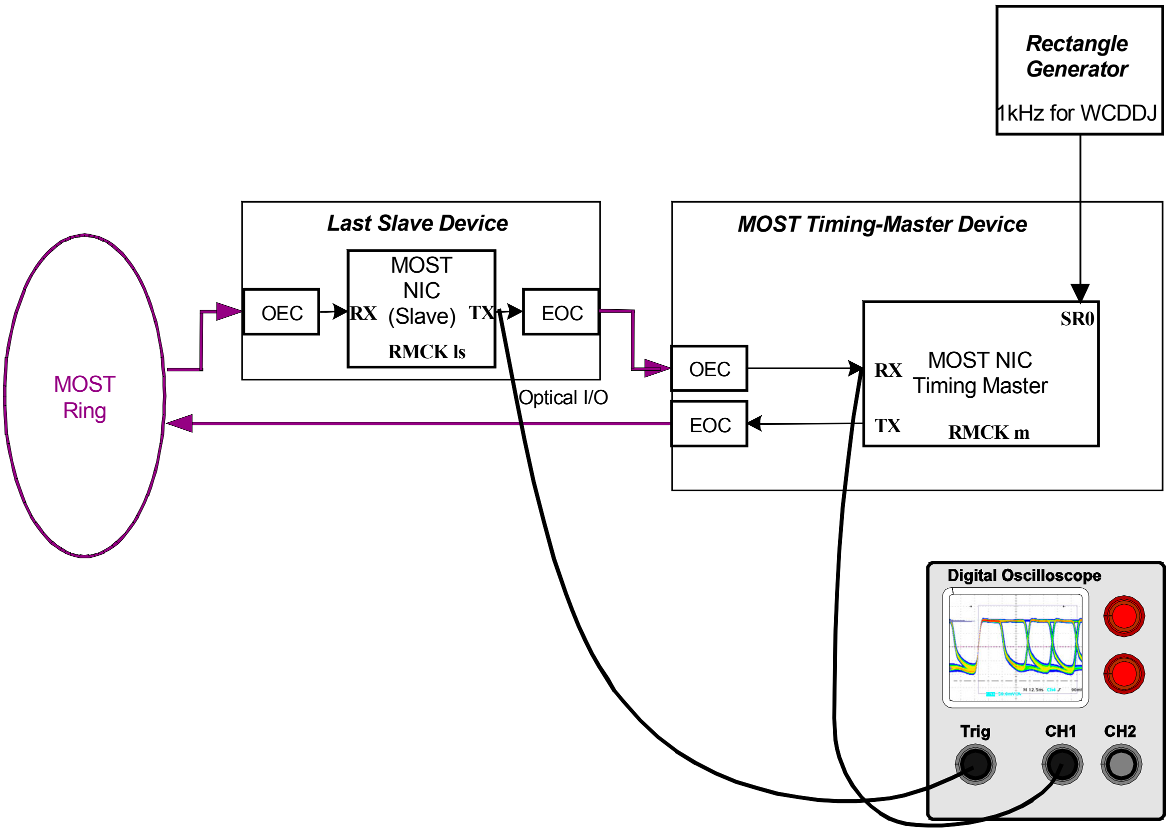


Figure 3-7: Measurement setup for DDJ and UJ of the last link

3.2.4 Measurement of Application Specific DDJ+UJ

The measurement shown above reflects the absolute worst-case of phase variations that normally does not occur in real systems. The test patterns for Phase Variation were created to separate DDJ and UJ on optical links. The patterns will also produce absolute worst-case Phase Variation on system level. However, in real systems no synchronous or asynchronous data will be 0xFF on all bytes especially over several frames. Therefore the test method using worst-case patterns may be oversized on system level. A different method can be used which leads also in assured results, but requires very good knowledge what kind of data are transmitted over the MOST bus. This method is oriented on structures of the target system.

In general the measurement is done in the same manner as described above, but the test pattern on the frame is adapted to the real condition of the target system. To create such a test pattern the frame is divided into three sections:

- Synchronous data area used by the target system (green area in Figure 3-8)
- Synchronous data area unused by the target system (yellow area in Figure 3-8)
- Asynchronous data area (red area in Figure 3-8)

Each of these areas is filled with their corresponding worst-case patterns.

Workflow how to get a application specific worst-case pattern:

1. Determine the SBC value of the target system.
   Size of synchronous area = SBC value * 4 (Bytes)
   Size of asynchronous area = (0x0F – SBC value) * 4 (Bytes)
2. Determine the max. number of synchronous bytes, which will be used at the same time.
3. In order to route specific test patterns to all channels of the frame set the SBC value at the master to 0x0F.
4. Route the signal (according to chapter 1.1.4.2) to the channels in the frame that correspond to the asynchronous area in the frame.
   Refer to Figure 3-9, SR0 is routed to asynchronous area (red area in Figure 3-8).
5. Route random data to all the channels that are used for synchronous data.
   Refer to Figure 3-9, SR1 is routed to synchronous area (green area in Figure 3-8).
   In addition the data stream on SR1 is gated by the test signal on SR0. This causes the synchronous channels to switch between 00H and random data (corresponds to a pause between two CD – tracks).
6. Route 0x00 to all unused synchronous channels (yellow area in Figure 3-8).

Figure 3-9 shows the measurement setup using an application specific pattern.

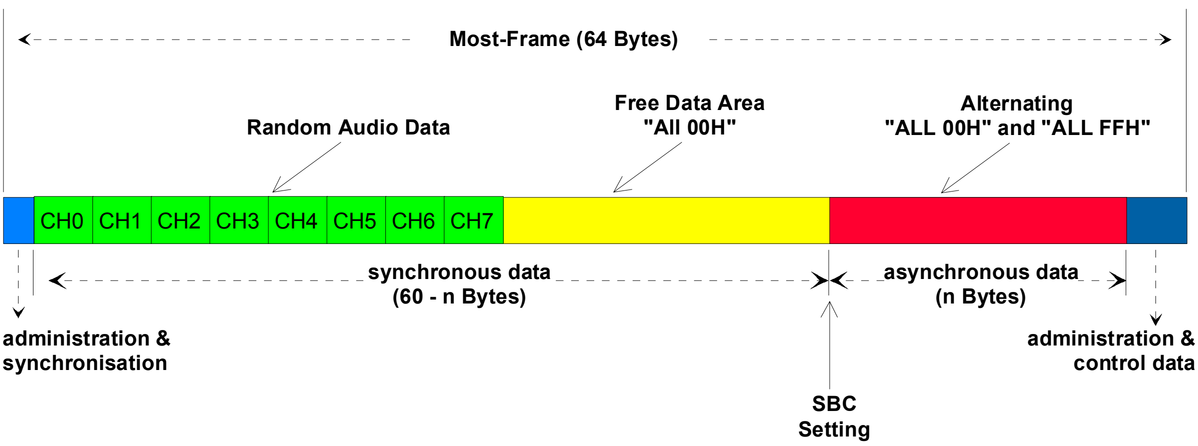


Figure 3-8: Example of an application specific test pattern

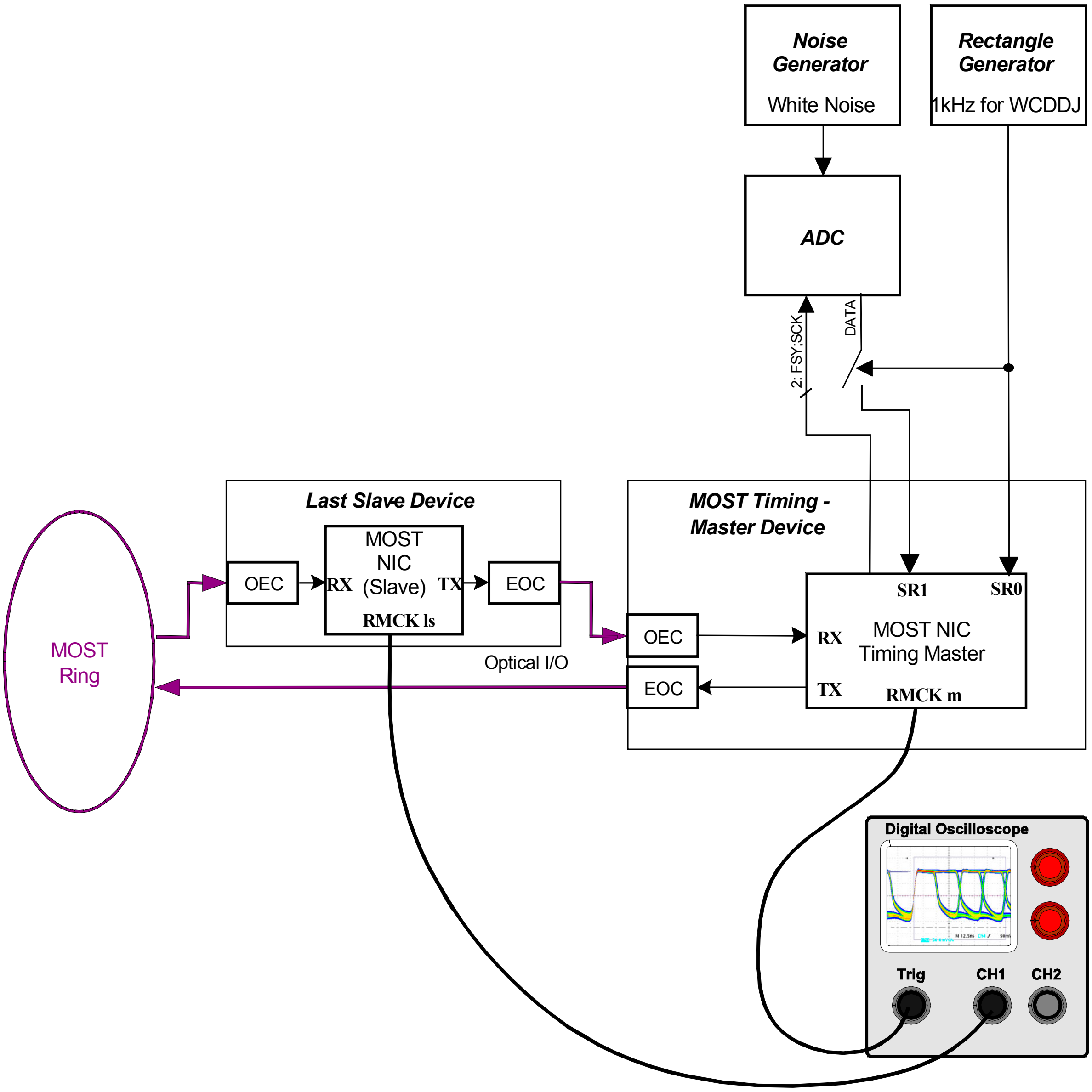


Figure 3-9: Measurement setup for accumulated DDJ and UJ with system related WCDDJ signal

Appendix A: List of Figures

Figure 1-1: Location of specification points along a MOST point-to-point-link 10
Figure 1-2: Structure of the MOST frame. 11
Figure 1-3: Sketch regarding signal distortion (typical signal of SP4 @ FS = 44.1kHz). 16
Figure 1-4: Tolerance-scheme for SP1 to SP4 regarding signal distortion @ 44.1kHz FS. 17
Figure 1-5: Test setup for phase variation measurements for an optical link. 19
Figure 1-6: Test setup for phase variation measurements at SP2 for slave devices 20
Figure 1-7: Test setup for phase variation measurements at SP2 for master devices 20
Figure 1-8: Test setup for phase variation measurements at SP4 for slave devices using 1 master and 2 slaves. 21
Figure 1-9: Test setup for phase variation measurements at SP4 for slave devices using 1 master and 1 slave. 21
Figure 1-10: Test setup for phase variation measurements at SP4 for master devices 22
Figure 1-11: Example for data dependent link-jitter @SP4 23
Figure 1-12: Example for uncorrelated link-jitter @SP4 23
Figure 1-13: PWV histogram measurement 26
Figure 1-14: PWV histogram 27
Figure 1-15: Schematic of optical power meter 29
Figure 1-16: Calculation of aperture size d_B 29
Figure 1-17: Optical power measurement setup for SP3 30
Figure 2-1: Measurement set up for checking the parameters at SP1 32
Figure 2-2: Sketch regarding signal distortion parameters at SP1 based on FS=44.1 kHz 34
Figure 2-3: Measurement setup for input capacitance C_{I1} 35
Figure 2-4: typical charge characteristic of C_{I1} 36
Figure 2-5: Measurement setup for input resistance of R_{I1} 36
Figure 2-6: Measurement setup for dynamic parameters at SP2 37
Figure 2-7: Measurement setup for optical power parameters at SP2 38
Figure 2-8: Example for vertical histogram to evaluate b1 and b0 40
Figure 2-9: Schematics of optical pulses at specification point 2. 43
Figure 2-10: Measurement setup for optical power parameters at SP3 44
Figure 2-11: Measurement setup for optical output power for light off. 45
Figure 2-12: Measurement setup for optical output power for light off. 48
Figure 2-13: Sketch regarding signal distortion parameters at SP4 based on FS=44.1 kHz 51
Figure 3-1: Measurement setup for wander 54
Figure 3-2: Delay at start of measurement 55
Figure 3-3 Delay at end of measurement 56
Figure 3-4: Measurement of Tx-to-Rx peak-to-peak jitter at the timing master 57
Figure 3-5: Measurement setup for accumulated DDJ and UJ 59
Figure 3-6: Measurement of DDJ plus UJ (peak-to-peak) 60
Figure 3-7: Measurement setup for DDJ and UJ of the last link 61
Figure 3-8: Example of an application specific test pattern 62
Figure 3-9: Measurement setup for accumulated DDJ and UJ with system related WCDDJ signal 63

Appendix B: List of Tables

Table 1-1: Description of specification points. 10
Table 1-2: Table of worst-case pattern for pulse width variation 12
Table 1-3: Table of worst-case pattern for data dependent jitter. 13
Table 1-4: Table of worst-case pattern for uncorrelated jitter. 14
Table 1-5: Table of abbreviations regarding signal distortion. 15
Table 1-6: Table of example, measured values based on Figure 1-3 16
Table 1-7: Summary phase variations 18
Table 1-8: Table of minimum acquisition time 24
Table 1-9: Theory of tail fitting 25
Table 2-1: Parameters of specification points. 31
Table 2-2: Pulse width distortion values at SP1 33
Table 2-3: Phase variation limits at SP1 34
Table 2-4: Parameter for extinction ratio 39
Table 2-5: Pulse width distortion values at SP2 41
Table 2-6: Phase variation limits at SP2. 42
Table 2-7: Phase variation limits at SP3. 46
Table 2-8: Phase variation limits at SP3. 47
Table 2-9: Phase variation limits at SP4. 50
Table 2-10: Phase variation limits at SP4. 51
Table 3-1: Relationship of system jitter parameters 52

Appendix C: Abbreviations

ADC	Analog to Digital Converter
APWD	Average Pulse Width Distortion
APWD~	APWD~ is the APWD related to the relevant pulse width (1UI, 2UI, 3UI)
BER	Bit Error Rate
EOC	Electrical Optical Converter
CDF	Cumulative Density Function
DDJ	Data Dependent Jitter
DUT	Device under Test
FS	Frame Sync per second (System sample frequency)
FWHM	Full Width at Half Maximum
NA	Numerical Aperture
NIC	Network Interface Controller
OEC	Optical Electrical Converter
PDF	Probability Density Function
PWV	Pulse Width Variation
RMCK	Received Master Clock
Rx	MOST NIC Input
SBC	Synchronous Boundary Control Register
SPn	Specification Point No. n (n= 1 … 4)
SR0 / SR1	Source Data Inputs of NIC
Ta	Ambient Temperature
TSW	Test Signal For Wander
Tx	MOST NIC Output
UI	Unit Interval
UJ	Uncorrelated Jitter
WCDDJ	Worst-Case Pattern for Data Dependent Jitter
WCPWV	Worst-Case Pattern for Pulse Width Variation
WCUJ	Worst-Case Pattern for Uncorrelated Jitter

Notes: