MOST

Media **O**riented **S**ystems **T**ransport

Multimedia and Control Networking Technology

MOST Electrical Physical Layer Specification

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For more information on the MOST technology, please contact:

MOST Cooperation
Administration
Bannwaldallee 48
D-76185 Karlsruhe
Germany

Tel: (+49) (0) 721 966 50 00
Fax:(+49) (0) 721 966 50 01
E-mail: contact@mostcooperation.com
Web: www.mostcooperation.com

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Contents

Document Structure

All documents this MOST document is referring to are listed here with the actual revision.

Document	Revision
MOST Electrical Physical Layer Compliance Specification	1V0_00

Document History

Initial Release: 02/2004

First version 0.9-00

Change Ref.	Section	Changes
0V9_00	-	First issue

Changes version 0.9-00 to 1.0-00

Change Ref.	Section	Changes
1V0_00	2	Decided the one electrical physical Layer solution
-	APPENDIX B.1	Added wire harness and connector conditions
-	APPENDIX B.2	Added System evaluation
-	APPENDIX B.3	Added Interoperability
-	3.2	Added EMC regulation B

Changes version 1.0-00 to 1.1-00

Change Ref.	Section	Changes
1V1_00	-	Reviewed the whole structure for separating Compliance Specification from ePHY Specification
-	3.1.1, 3.1.2, 3.1.3, 3.1.4	Filled the detail parameter

1 Introduction

The Electrical Physical Layer Specification is part of the specifications of the MOST® (Multimedia Oriented System Transport) system. The Electrical Physical Layer of the MOST network supports electrical transmission of the bit stream between MOST devices. This document, the "MOST Specification of Electrical Physical Layer", describes and defines Specification Points (SP's) and pass/fail criteria of SP's and noise tests.

1.1 General Description

The ePHY system is a method of serial data communication between two or more MOST50 compatible nodes using twisted pair (TP) wire instead of optical fiber. As such, an ePHY link can be more susceptible to electrical noise than an optical link and can also emit more electrical noise than an optical link. A simplified block diagram of a two-node ePHY connection is shown below. A large portion of the circuitry is designed for the purpose of reducing electrical emissions and increasing the overall system immunity to EMI.

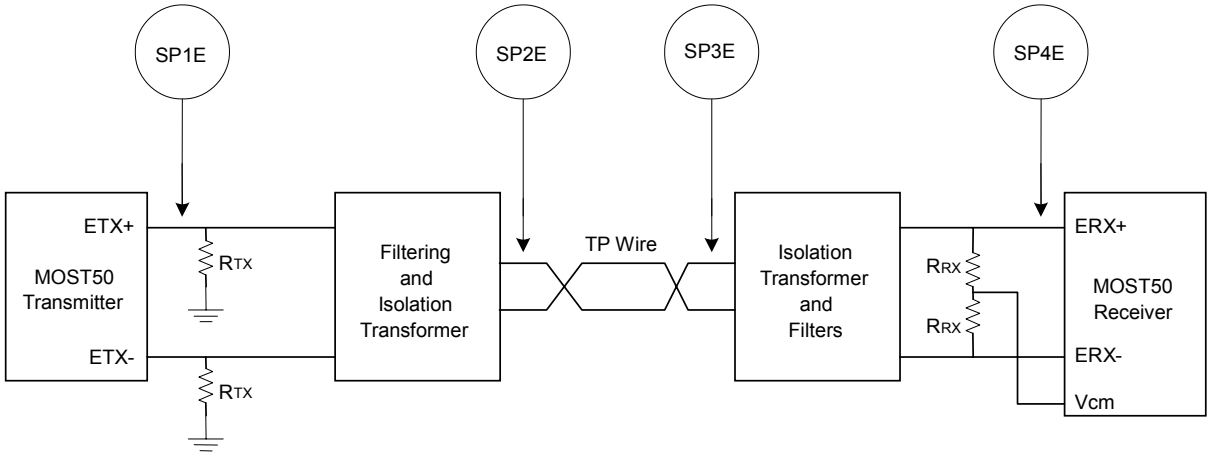


Figure 1-1: Block Diagram of ePHY Physical Layer

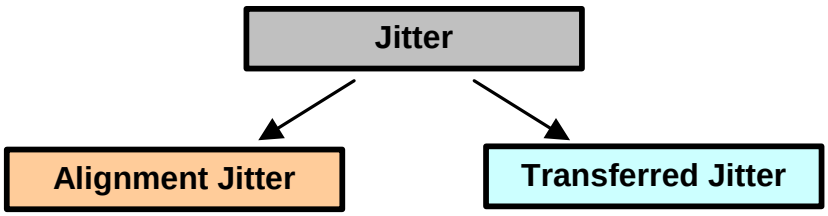
Note: There is no relationship between the optical specification points SP1...SP4 and the ePHY specification points SP1E...SP4E. The "E" suffix has been added to differentiate the ePHY specifications from the optical specifications.

There are four primary measurement points – SP1E, SP2E, SP3E and SP4E – in an ePHY system. These points are illustrated in
Figure 1-1. All of the tests listed in this specification refer to one of these four points to indicate the point in the system from which data should be collected.
The MOST50 transmitter output, ETX+ and ETX-, is a differential signal generated by a DAC. The DAC creates a low-pass filtered version of the MOST data at SP1E. This signal is sent through a low pass analog filter to further filter the DAC output and is then sent to an isolation transformer that drives the TP cable at SP2E. The transformer increases the noise immunity of the receive-side circuitry by providing a high level of common mode noise rejection. Both the transmit and receive-side circuits should be terminated to match the cable impedance.

At the receiver end, SP3E, the signal is applied to an isolation transformer that feeds into a low-pass filter before being applied to the receiver's ERX+ and ERX- inputs at SP4E as a fully differential signal. The resistors at the receiver inputs serve to terminate the line in its characteristic impedance and are also used to form a center tap for providing the proper common mode voltage to the differential receiver. All signals from SP1E to SP4E are differential and should be measured with a differential oscilloscope probe.

2 Monitoring Methodology

For reliable data transmission over a wide range of operating conditions, including high electrical noise environments, the signals at all points along the transmission path need to be kept as noise free as possible, and signal distortion due to jitter and pulse width variation must be minimized. As an aid to designing and verifying an acceptable signal path, the four specification/test points SP1E, SP2E, SP3E, and SP4E have been selected for detailed definition and standardization. Eye Mask Templates are provided for pass-fail testing. Eye patterns that pass the template tests should result in a link with a Bit Error Ratio that is better than 10e-9.
Since all the signals at the specification points are differential, a high-quality differential oscilloscope probe must be used to take the measurements.
It should be also noted that there are two kinds of jitter that appear on a MOST50 signal; high frequency jitter and low frequency jitter.
The high frequency jitter is called “Alignment Jitter” and affects the ability to recover data in a NIC. “Alignment Jitter” is controlled by Eye-pattern measurements, and thus the limit is defined in eye masks. For the detection of Eye-diagrams, a clock-signal needs to be recovered from the data stream. (see chapter 2.1 for details)
The low frequency jitter is called “Transferred Jitter” and affects accumulation of system jitter over a network. For detection of “Transferred Jitter” a Jitter Filter is required. Limits for “Transferred Jitter” are defined in RMS. (for details see chapter 2.2)



2.1 Eye Patterns and Masks

This specification utilizes eye pattern diagrams and mask templates to validate the serial data link. A properly acquired eye pattern simultaneously tests signal amplitude, rise/fall time, pulse width variation (PWV), average pulse width distortion (APWD) and alignment jitter.
A high-quality signal with low jitter and distortion will show a large eye opening, which can be compared to a standardized mask, placed in the center of the eye for comparison (a diamond shape in the center of the eye). The mask is designed such that a good signal will not touch the mask at any locations. A pattern that touches the mask can be recorded as a failure and logged by the test equipment automatically. Signals with slow rise times, low amplitudes, jitter, or pulse width variations will show up as closures in the eye pattern. Signals with excessively high amplitudes will touch the horizontal bars above and below the eye diagram and also cause a failure to be recorded.
An eye diagram is formed inside of the oscilloscope using a serial data analysis tool (SDA). The tool performs clock recovery (clock @ UI-rate) with a specified model on the data stream and will show an eye diagram. The PLL model used for forming the eye diagram contains a single pole with a bandwidth of 125 kHz (Please refer to Figure 2-2: Filter Transfer Function and Table 2-1: PLL Filter Response).
The formation of an eye pattern starts by capturing the network signal. The data from each UI is then overlaid on top of the other to from an eye pattern. The eye pattern causes any differences in pulse shape or timing to become apparent. The eye pattern is then overlaid onto an eye mask. If any part of the signal trace touches the mask, then the signal is considered out-of-spec.
The basic Eye Mask Template for MOST50 ePHY is illustrated in Figure 2-1. The values for Points A to D and Levels 1 to 2 are defined in a table for each Specification Point.

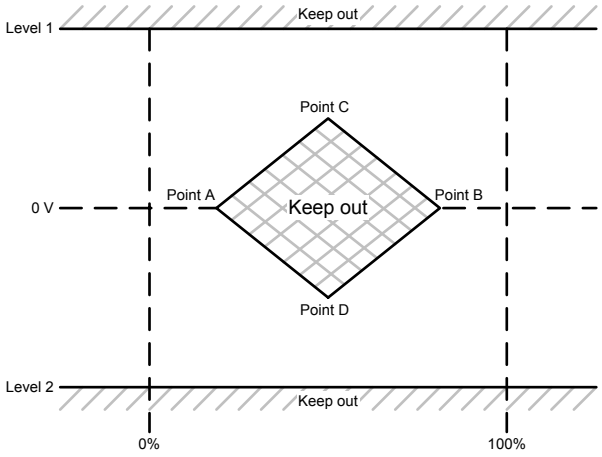


Figure 2-1: Eye Mask Template

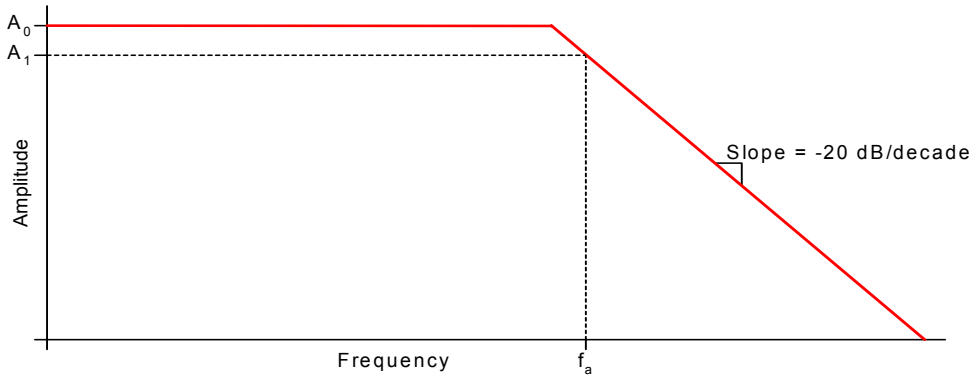


Figure 2-2: Filter Transfer Function

Parameter	Value	Unit
A_0	0	dB
A_1	-3	dB
f_a	125	kHz

Table 2-1: PLL Filter Response

2.2 Transferred Jitter

All Jitter that can be tracked by a PLL will be transferred to the output data stream of a NIC. Jitter below the PLL loop bandwidth will be transferred and therefore accumulated within the ring. Jitter above the loop bandwidth will be attenuated. Therefore the detection of Transferred Jitter requires a Jitter Filter, the characteristics of that filter are given in Table 2-2 and Figure 2-3. This filter can be modeled in software and is used in combination with serial data analysis tools. Transferred jitter is measured as the filtered root mean square of the skew of the data edges compared to their ideal locations.

Parameter	Value	Unit
A_0	0	dB
A_1	-3	dB
A_2	-20	dB
f_a	10	kHz
f_b	500	kHz
f_c	5000	kHz

Table 2-2: Transferred Jitter Filter Characteristics

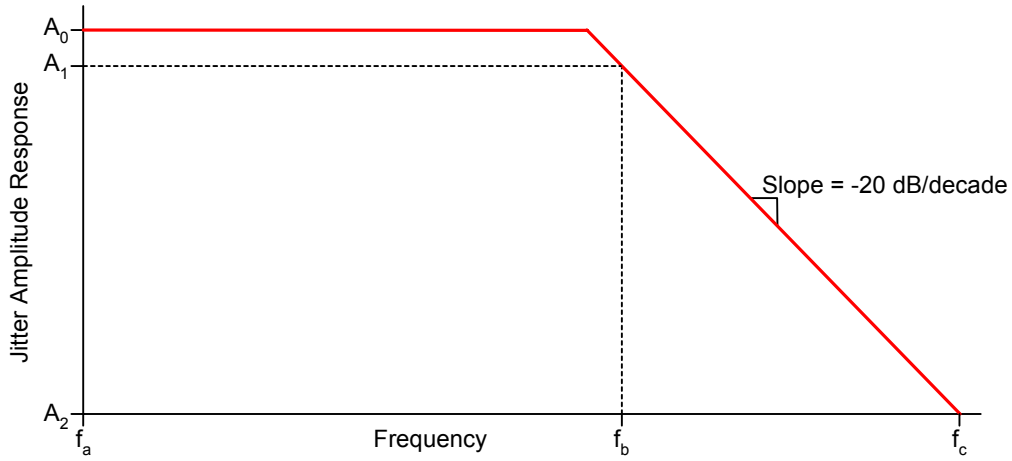


Figure 2-3: Filter Transfer Function for Transferred Jitter Measurement

3 Requirements

3.1 Signal Requirements

3.1.1 SP1E (NIC Transmission)

3.1.1.1 Transmission Quality

Transmission Quality is measured at SP1E using an eye mask as defined in Section 2.1.
The test mask defines a minimum transmit eye opening area and a maximum transmit signal amplitude for the NIC under test. (Please see the Appendix C for more information.) The waveform should not intrude on any of the keep-out areas. The Eye Mask for SP1E is defined in Table 3-1. See Figure 2-1 for the Eye Mask Template.

Parameter	Voltage (V)	Time (%UI)
Point A	0.00	11.7
Point B	0.00	88.3
Point C	0.20	50.0
Point D	-0.20	50.0
Level 1	1.25	N/A
Level 2	-1.25	N/A

Table 3-1: SP1E Eye Mask Parameters

3.1.1.2 Transferred Jitter

NIC Transferred Jitter must be less than 140 ps_{RMS} when measured at SP1E.

3.1.2 SP2E (Device Transmission)

3.1.2.1 Transmission Quality

Transmission Quality is measured at SP2E using an eye mask as defined in Section 2.1.
The test mask defines a minimum transmit eye opening area and a maximum transmit signal amplitude for the node under test. (Please see the Appendix C for more information.) The waveform should not intrude on any of the keep-out areas. The Eye Mask for SP2E is defined in Table 3-2. See Figure 2-1 for the Eye Mask Template.

Parameter	Voltage (V)	Time (%UI)
Point A	0.00	15.6
Point B	0.00	84.4
Point C	0.30	50.0
Point D	-0.30	50.0
Level 1	1.25	N/A
Level 2	-1.25	N/A

Table 3-2: SP2E Eye Mask Parameters

3.1.2.2 Transferred Jitter

Device Transferred Jitter must be less than 150 ps_{RMS} when measured at SP2E.

3.1.3 SP3E (Device Receiver Tolerance)

Receiver Tolerance, measured at SP3E, defines the minimum and maximum limits for the eye pattern which the receiving device must be able to recover.
The test mask defines the minimum and maximum limits for the eye pattern which the receiving node must be able to recover. (Please see the Appendix C for more information.) The waveform should not intrude on any of the keep-out areas. The Eye Mask for SP3E is defined in Table 3-3. See Figure 2-1 for the Eye Mask Template.

Parameter	Voltage (V)	Time (%UI)
Point A	0	23.5
Point B	0	76.5
Point C	0.15	50
Point D	-0.15	50
Level 1	1.25	N/A
Level 2	-1.25	N/A

Table 3-3: SP3E Eye Mask Parameters

3.1.4 SP4E (NIC Receiver Tolerance)

Receiver Tolerance, measured at SP4E, defines the minimum and maximum limits for the eye pattern which the receiving NIC must be able to recover.
The test mask defines the minimum and maximum limits for the eye pattern which the receiving node must be able to recover. (Please see the Appendix C for more information.) The waveform should not

intrude on any of the keep-out areas. The Eye Mask for SP4E is defined in Table 3-4. See Figure 2-1 for the Eye Mask Template.

Parameter	Voltage (V)	Time (%UI)
Point A	0.00	23.5
Point B	0.00	76.5
Point C	0.15	50
Point D	-0.15	50
Level 1	1.25	N/A
Level 2	-1.25	N/A

Table 3-4: SP4E Eye Mask Parameters

3.1.5 Receiver Tolerance Consideration

When designing the ePHY network system as shown in Figure 3-1, it is recommended to measure the Receiver Tolerance of all nodes in the entire system in order to ensure a reliable and robust network. When measuring the Receiver Tolerance, all nodes in the network shall meet the SP4E Receiver Tolerance requirements defined in 3.1.4 SP4E (NIC Receiver Tolerance).

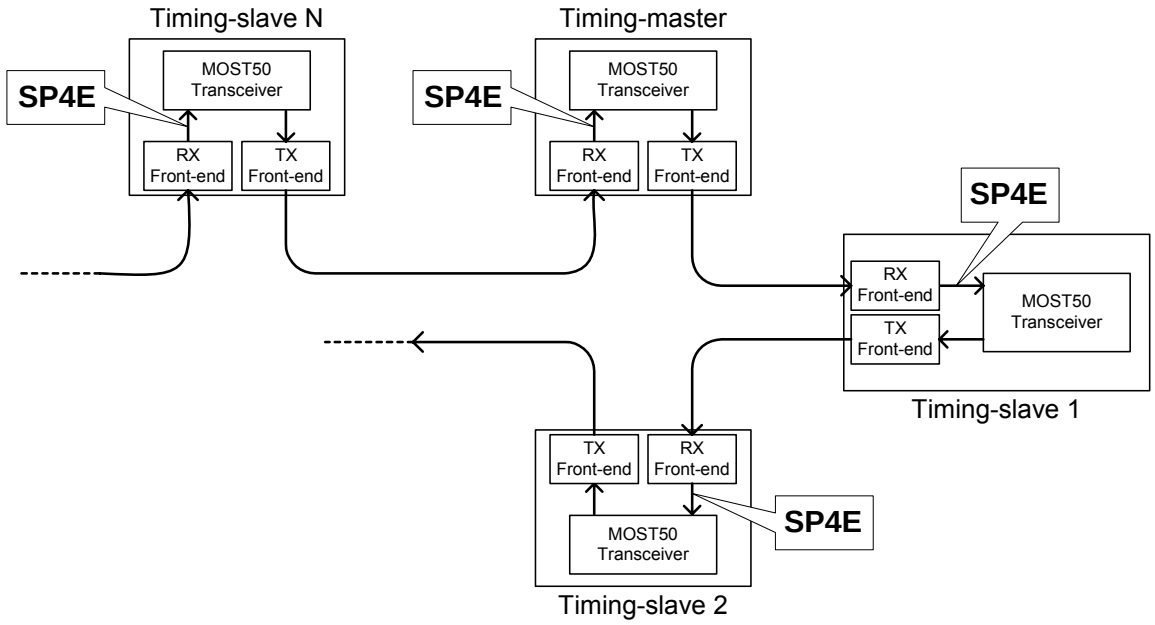


Figure 3-1: MOST50 ePHY network system with N timing-slave nodes

3.2 Electromagnetic Requirements

EMC should be considered by all device makers during the design process. Refer to the OEM's specifications for exact EMC requirements.

Appendix A. Acronyms

- ePHY: Electrical Physical Layer
- SP: Specification Point
- SPnE: Specification Point for ePHY (n=1 to 4. The suffix 'E' denotes Electrical Physical Layer)
- PWV: Pulse Width Variation
- APWD: Average Pulse Width Distortion
- SDA: Serial Data Analysis
- NIC: Network Interface Controller
- UI: Unit Interval
- EMC: Electromagnetic Compatibility
- WG: Working Group

Appendix B. ePHY WG Early Investigation Information

This appendix presents additional information that the ePHY WG used when investigating the validity of the ePHY system during the early stages of development.
The information about Device Front End circuitry, the wire harness and connectors, which were used during the system evaluation are given in the following sections.
The contents described in this appendix are just information and NOT a mandatory specification of ePHY.

B.1 Device Front End

B.1.1 Front End Circuitry

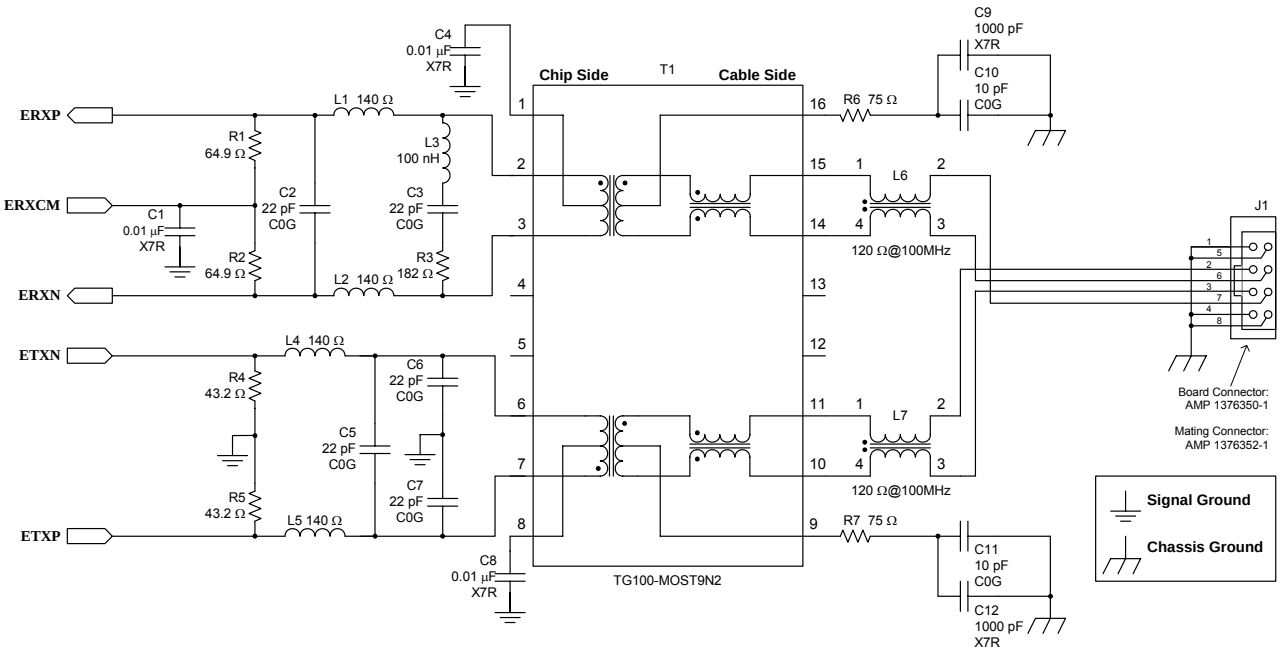


Figure B-1: Front end circuitry

NOTE: The most up-to-date Front End circuitry can always be found in the latest NIC data sheet from the IC vendor.

B.1.2 Front End Components

The table below shows the components used the Front End Circuitry;

Qty	Reference	Part Number	Manufacturer	Description
5	C2,C3, C5, C6, C7			CAP, 22 pF, COG, 50 V, 5 %
3	C1, C4, C8			CAP, 0.01 uF, X7R, 50 V, 10 %
2	C9, C12			CAP, 1000 pF, X7R, 50 V, 5 %
2	C10, C11			CAP, 10 pF, COG, 50 V, 5 %
1	J1	1376350-2	TYCO/AMP	8-Pin 2x4 Right Angle connector
4	L1, L2, L4, L5	BLM18BB141SN1	MURATA	Ferrite Bead, 140 Ω @ 100 MHz, 200 mA, 0603
1	L3	LQW18ANR10J00	MURATA	High Freq Chip Coil, 100 nH, 5%, 220 mA, 0603
2	L6, L7	DLP31SN121SL2	MURATA	COMMON-MODE CHOKE COIL, 16V, 100 mA, 120 Ω @ 100 MHz, SMD
2	R1, R2			RES, 64.9 Ω, 0603, 1/10 W, 1 %, 200 ppm
1	R3			RES, 182 Ω, 0603, 1/10 W, 1 %, 200 ppm
2	R4, R5			RES, 43.2 Ω, 0603, 1/10 W, 1 %, 200 ppm
2	R6, R7			RES, 75.0 Ω, 1210, 1/2 W, 1 %, 200 ppm
1	T1	TG100-MOST9N2	HALO	MOST Transformer, SMD

Table B-1: Front End Components

The table below shows the recommended transformer specifications;

Parameter	Value	Units	Notes
Open Circuit Inductance	200	µH	100 kHz, 0.1 Vrms
Insertion Loss	-1	dB	Max., 100 kHz to 50 MHz
Isolation Voltage	1500	Vrms	Min.
DC Winding Resistance	0.6	Ω	Max.
Winding to winding Capacitance	18	pF	Max.
Turns Ratio (windings	1:1 ±3% 1:1.5 ±3%		RX TX
Common-mode Rejection (Note 1)	-40	dB	Min., 100 kHz to 100 MHz
Common to Diff Rejection (Note 2)	-40	dB	Min., 100 kHz to 100 MHz
Diff to Common Rejection (Note 3)	-50	dB	Min., 100 kHz to 100 MHz
100Ω Return Loss	-12	dB	Min., at 50 MHz
Operating Temperature	-40 / +85	°C	

Notes:

1. Common-mode Rejection is measured for both TX and RX halves of the transformer module. For the TX half, it is measured from the chip-side to the wire-side. For the RX half, it is measured from the wire-side to the chip-side.
2. Common-mode to Differential Rejection is measured on the RX half of the transformer module from the wire-side to the chip-side.
3. Differential to Common-mode Rejection is measured on the TX half of the transformer module from the chip-side to the wire-side.

Table B-2: Transformer Specification

B.2 Wire Harness

Cable	Unshielded twisted pair cable
Gauge	0.22 mm^2
Twist length	Less than 45 mm
Untwisted wire length	Less than 10 cm
Characteristic Impedance	130Ω +10/-30

Table B-3: Wire Harness

B.3 Connectors

Maker	Tyco Electronics AMP
Product Number	1376350-2, 1376352-1

Table B-4: Connector

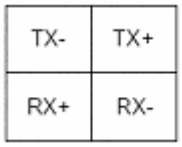


Figure B-2: Pin orientation

B.4 System Evaluation

At the early stage of ePHY development, the ePHY WG conducted the system evaluation in order to investigate the electrical characteristic assuming basic vehicle environments.
The system evaluation included the following tests and the ePHY WG confirmed the validity of the method described in this specification.

No	Content	Condition
1	Max number of nodes	64 nodes (Functional testing) 30 nodes (Actual testing)
2	Max number of connector between the nodes	8 connectors
3	Max length of wire harness between the nodes	10 m
4	Worst case of system / connection pattern	Combination of 1, 2, 3 and 4

Table B-5: System evaluation

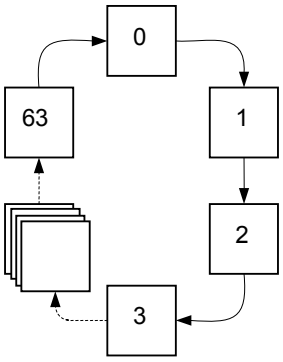


Figure B-4: Max Number of Nodes

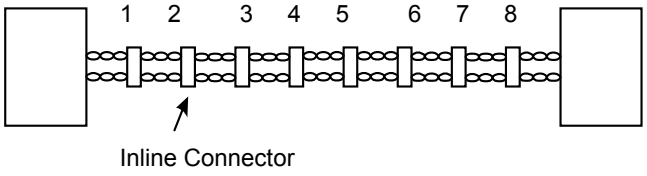


Figure B-3: Max Number of Connector Between the Nodes

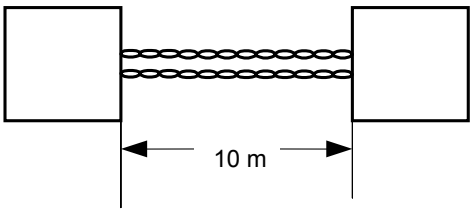


Figure B-5: Max Length of Wire Harness Between the Nodes

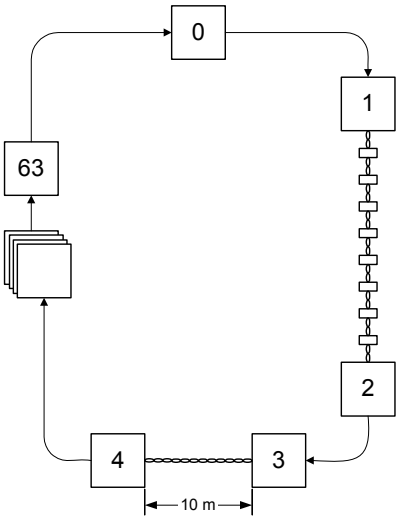


Figure B-6: Worst Case of System / Connection Pattern

Appendix C. Eye Pattern Diagram Information

This appendix is provided only for better understanding of the relationship between eye pattern and eye mask parameters (min., typ., and max. values), and is out of the scope of this specification.
The diagram below shows a few important points of an eye pattern, which is the collection of waveforms, to be looked at:

- WF Typ: represents the typical value of the wave pattern
- WF Max: represents the maximum value of the wave pattern
- WF Min: represents the minimum value of the wave pattern

* Please note that the parts of waveforms drawn in the diagram are schematic waveforms and differ from actual waveforms

Therefore, the point A of the eye mask parameter specifies the maximum limit for eye pattern, while the point B of the eye mask parameter specifies the minimum limit for the eye pattern.

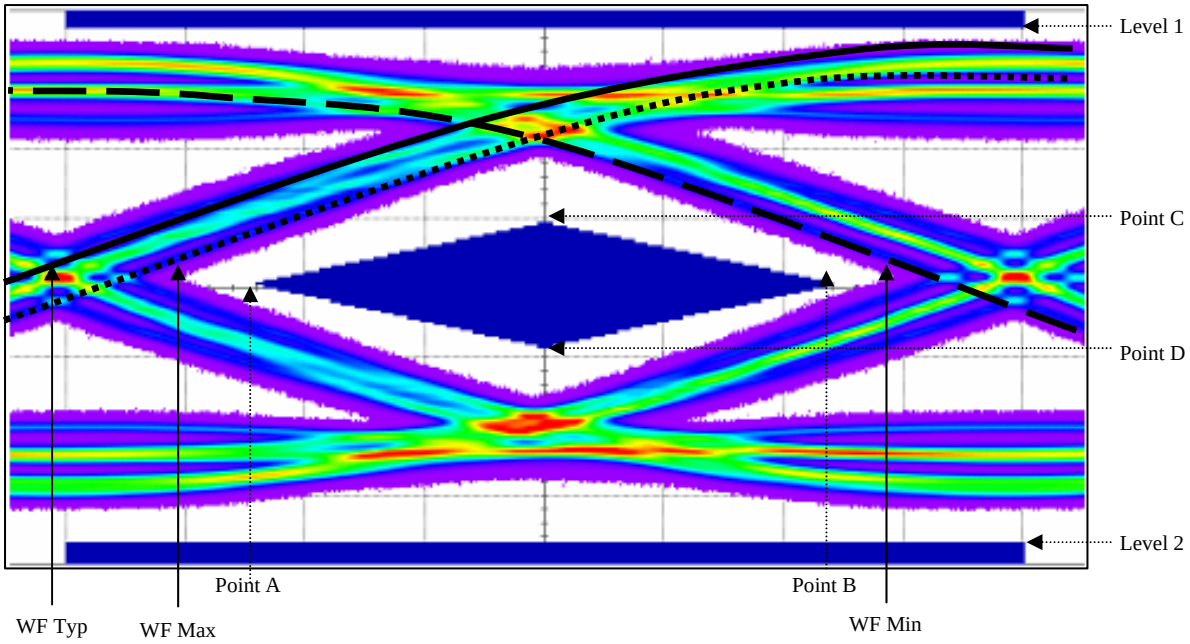


Figure C-1: An Eye Mask and Eye Pattern

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