MOST

Media **O**riented **S**ystems **T**ransport

Multimedia and Control
Networking Technology

MOST Specification of Physical Layer
Rev 1.1
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Version 1.1-00

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Contents

Bibliography

Number/ Keyword	MOST related Documents
[1]	MOST Specification Framework
[2]	MOST Specification
[3]	MOST High Protocol Specification
[8]	MOST FunctionCatalog
[9]	MOST Specification Of Physical Layer
[10]	MOST Compliance Test Of Physical Layer

Number/ Keyword	Other Documents
-	IEC958
-	EN/IEC 61280-2-2
-	IEC 60825-1/-2

Document History

Initial Release Date: 2001-02-16

First version 1.0-00

Change Ref.	Section	Changes
-	-	- First version, no changes

Changes revision 1.0-00 to revision 1.1-00

Change Ref.	Section	Changes
-	Bibliography	- Corrected numbers in table, remove Netservices documents, other documents added which are not related to MOST but mentioned within this document
	1	- Changed “MOST Network transceiver unit” to “MOST NIC” in Figure 1-1 and text - Added table which describes location of SPs
	2.2 – 2.5	- Corrected reference from Figure 1-2 to Figure1-1 in all tables of SP1…SP4
	2.1	Totally revised This was necessary since in addition to the point-to-point requirements there are also system-relevant parameters which were not handled in version V1.0. - Added tolerance for FS to be +/- 0.1% according to “normal accuracy mode” stated in IEC958 - Added chapter 2.1.1, Timing-Distortion, which describes the differences of pulse-width-distortion and phase-variation. This was necessary since the influence of phase-variation in a MOST system was not handled adequate in version V1.0 - Added chapter 2.1.1.1, Pulse-Width-Distortion This is the same as the remaining part of 2.1 general remarks of version V1.0. No changes were done as far as the content is concerned. - Added chapter 2.1.1.2, Phase-Variation This chapter describes in detail the influence of Wander, uncorrelated jitter and data dependent jitter - Added chapter 2.1.1.3, Overview Timing-Distortion This chapter summarizes all kind of timing-distortion and divides the timing-distortion into device-relevant aspects and system-relevant aspects. - Added chapter 2.1.2, Logic Levels at SP1 and SP4 Version V1.0 is based on TTL-Logic. The electrical interfaces SP1 & SP4 can also be realized with alternative logic families. This chapter gives some notes to take into consideration.
	2.2	- Added values for data dependent jitter and uncorrelated jitter. - Added note that all values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements. - Changed note 1) Range of VDD +/- 5% - Added note 5) Trigger signal for UJ- and DDJ-measurement is TX - Added note 6) R_{I1} and C_{I1} are parameters of the input of the EOC.

Change Ref.	Section	Changes
	2.3	- Added bit rate parameter - Changed pulse-width-variation to 0.903 - 1.097UI - Changed average pulse-width-distortion to -0.063 - +0.063UI - Added values for data dependent jitter and uncorrelated jitter. - Added note that all values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements. Components or modules have to fulfill the specified output parameters considering min/max conditions on the input parameters. - Changed note 2 to “Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0mm”. - Added to note 7 “The limits for positive/negative overshot must be kept after the rising edge (respectively falling edge) passed b1 (respectively b0).” - Added note 8) Trigger signal for UJ- and DDJ-measurement is TX. - Added note 9) The designations of IEC 60825-1/-2 'safety of optical fiber communication' have to be taken into account - Removed “No Light” – line from Figure 2-2 which could cause confusion.
	2.4	- Added parameter “bit rate”, “Peak wavelength of input signal” and “FWHM of input signal” - Changed Pulse Width Variation to 0.903 - 1.097UI - Changed average pulse-width-distortion to -0.063 - +0.063UI - Added values for data dependent jitter and uncorrelated jitter. - Added note that all values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements. - Changed note 1 to “Average values, when receiving modulated light. Tolerance ranges for timing and amplitude specified for SP3 (r_{e3}, t_{r3}, t_{f3}, t_{pwv3}, t_{apwd3}) have to be fulfilled.” - Changed note 3 to “Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0mm”. - Changed note 4 to “Average values, when receiving modulated light or stray light.” - Added note 9) Trigger signal for UJ- and DDJ-measurement is TX. - Added note 10) an attenuation of >0.5dB between SP2 and SP3 is assumed.
	2.5	- Added low level output voltage “min” – value. - Added high level output voltage “max” – value - Changed pulse-width-variation to 0.743 - 1.47UI - Changed average pulse-width-distortion to -0.15 - +0.316UI - Added values for data dependent jitter and uncorrelated jitter. - Added note that all values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements. Components or modules have to fulfill the specified output parameters considering min/max conditions on the input parameters. - Added note 5) Trigger signal for UJ- and DDJ-measurement is TX.
	2.6	- This chapter was totally revised since the system relevant parameters and their influence to the system were not explicit handled in version V1.0. Especially the influence of Wander, data dependent jitter and uncorrelated jitter on system level and how to calculate this system jitter is described in this section.
	2-3	- Assimilation of all indices to “unit $_{\text{parameter SP}}$“ (e.g. t_{pwv2})
	3.1	- Removed [ϕ=1,0 mm] in table 3-1
	6	- Abbreviations updated
		-
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1 Introduction

The Physical Layer of a MOST Network supports the optical transmission of the bit stream between MOST devices. This document describes and defines the "*MOST Specification of Physical Layer*".

The physical connection of two MOST devices is called "*point-to-point-link*". The "*MOST Specification of Physical Layer*" is organized in four specification points along an individual "*point-to-point-link*". The location of the specification points is shown in Figure 1-1.

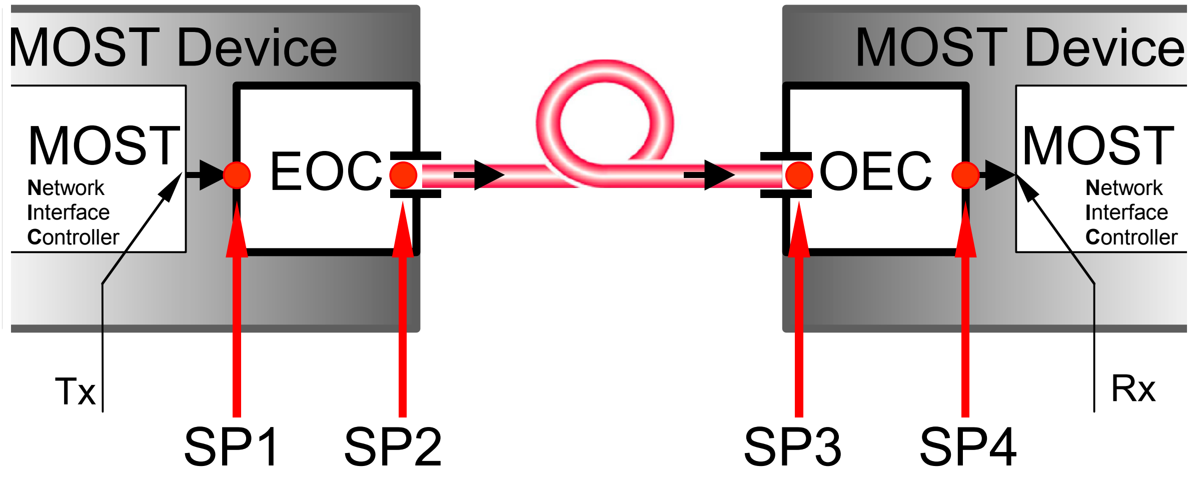

Figure 1-1: Location of specification points along a MOST point-to-point-link.

	Signal at SP	Location of SP
SP1	Electrical input signal	Data Input Pin of EOC
SP2	Radiated optical output signal	End face of the optical contact of the EOC (see also connector interface drawings)
SP3	Coupled optical input signal	Light input behind the end face of the optical contact of the OEC (see also connector interface drawings)
SP4	Electrical output signal	Data Output Pin of OEC, including a defined load

Table 1-1: Description of specification points.

Specification point No.1 and specification point No. 4 are pure electrical interfaces. They define the electrical signal requirements between a MOST NIC (**N**etwork **I**nterface **C**ontroller) with its input (Rx) and output (Tx) and an optical ⇔ electrical converter (e.g. electrical signal timings, electrical signal levels, electrical signal distortion).

Specification point No. 2 and specification point No. 3 define the optical and mechanical properties of the interfaces between a MOST device and a wiring harness (e.g. wavelength, optical signal timing, optical power budget, optical signal distortion, connector interface drawings). All parameters and definitions required for individual specification points are summarized in tables that are referenced in Table 1-2.

Individual MOST devices that fulfill the "*MOST Specification of Physical Layer*" are basically compatible to each other. Due to several point-to-point-links within a MOST Network, system network functionality is only ensured, when "*MOST Specification of Physical Layer*" is fulfilled by every individual point-to-point-link and the special requirements of section 2.6 are considered. The number of MOST devices is equal to the number of point-to-point-links.

There are special tests defined to check the physical layer compliance of MOST devices. These tests are part of the general MOST Compliance Test (see references in Table 1-2).

	References within this document	**References to other documents / URL**
SP 1: Electrical signal definitions	Table 2-1	
SP 2: Optical signal definitions Connector interface drawings	Table 2-2 Table 3-1, Table 3-2 Figure 3-1	www.mostcooperation.com
SP 3: Optical signal definitions Connector interface drawings	Table 2-3 Table 3-1, Table 3-2 Figure 3-1	www.mostcooperation.com
SP 4: Electrical signal definitions	Table 2-4	
Additional Requirements for system Design	Chapter 2.6	
Compliance Test of Specification Points		www.mostcooperation.com
Commercial Products and proprietary Specifications		www.mostcooperation.com

Table 1-2: Content and references of MOST Specification of Physical Layer.

2 Electrical and Optical Parameters

2.1 General Remarks

A MOST frame consists of 512 bits. The bit rate B of the MOST system can be calculated as:

B = 512bit * FS

Where FS is a particular sampling rate (FS = Frame Sync). Due to biphase mark coding, the smallest pulse length is given as:

UI = 1/(2B)

Where UI stands for Unit Interval. The FS has to stay within a tolerance of +/- 0.1% of the used sample frequency (e.g. 44.1kHz +/- 44.1Hz). This corresponds to the “normal accuracy mode” stated in IEC958.

Within a MOST pattern, only three different pulse lengths can occur. They are called UI, 2UI and 3UI. If FS is equal to 44.1kHz, the Bit Rate B and the Unit Interval UI are:

B = 22.5792 MBit/s

UI = 22.14ns.

The points Tx and Rx represent the interfaces of the used MOST Network Interface Controller (NIC). They are not specified here. However, they have to fulfill the requirements of SP1 and SP4. This includes possible worsening due to the transmission between the NIC and the respective EOC and OEC.

2.1.1 Timing-Distortion

All deviations from ideal signal timing are called timing-distortion. In principle timing-distortion can be divided up in two different subcategories. As a criterion for the distinction into the subcategories the consequences of the distortion type is used.

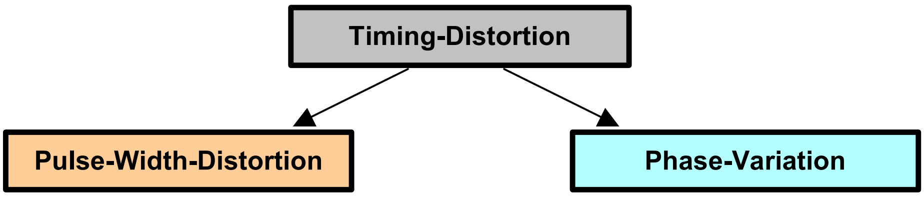

Figure 2-1: Classification of timing-distortion.

Please note: For the timing-distortion parameters an error rate of better than 10^{-9} is required!

Pulse-Width-Distortion:
Pulse-width-distortion is relevant for the data recovery on a single node in the network. Having passed an active MOST node all pulse-width-distortion will be removed from the data signal. Therefore there is no accumulation of pulse-width-distortion around the ring.

Phase-Variation:
Phase-variation describes the variation in delay of transitions in the data signal related to a reference signal. Phase-variations may accumulate around the ring due to the ability of PLLs to track on delay variations of the transitions in the data stream. The rules for the accumulation depend on the frequency characteristic of the variation and on the PLL's transfer function.

Phase-variation that appears on a single point to point link is called "link jitter". It is related to the TX-signal of the preceding node. "Link jitter " covers all parts of phase-variations that were generated at an individual link.

The total amount of phase variation at a particular position within the network is called "system jitter". It is always related to the TX-data signal of the timing master. "System jitter" includes all accumulated parts of phase-variations up to the point of observation.

All accumulated parts of phase-variation up to the last slave node in the ring (e.g. measured @TX of the last slave) plus the phase-variation generated by the last optical link between last slave (Tx) and timing master (SP4) determine the master jitter tolerance of the timing master and vice versa (see chapter 2.6).

2.1.1.1 Pulse-Width-Distortion

The definition of pulse-width-distortion includes two parameters called “pulse-width-variation” and “average pulse-width-distortion”.

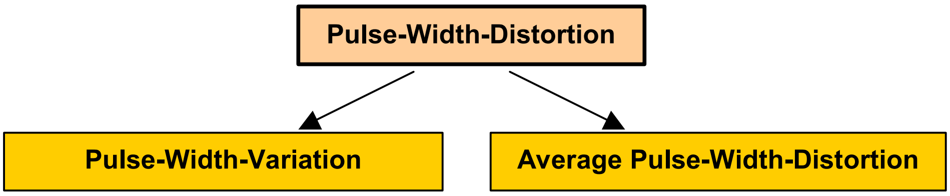

Figure 2-2: Classification of pulse-width-distortion.

Please Note: Pulse-width-distortion is specified for high pulses

The pulse width variation (t_{pwv}) is defined as the sum of the average pulse-width-distortion plus high-frequency jitter (see Figure 2-3). The limits for the pulse width variation are valid for all data elements (Length of high pulse = n*UI; n=1,2,3). Absolute pulse width has to be within the limits

$n*UI – (UI-t_{pwv(min)})$ and $n*UI + (t_{pwv(max)}–UI)$

$t_{pwv(min)}$, $t_{pwv(max)}$ are the specified parameters for PWV assuming an error rate of better than 10^{-9}.

The average pulse-width-distortion, defined as $t_{apwd} = (t_{pwmx} + t_{pwmn} – 2*n*UI)/2$, is illustrated in Figure 2-3. The measured values t_{pwmx} and t_{pwmn} are maximum and minimum values, so that pulses with a width of less than $t_{pwv(min)}$ or more than $t_{pwv(max)}$ occur with a probability of less than 10^{-9}. The example of Figure 2-3 shows the limit of $t_{pwmx} = t_{pwv(max)}$ and $t_{pwmn} = t_{pwv(min)}$.

The limits for the average pulse-width-distortion are valid for all data elements (Length of high pulse = n*UI; n=1,2,3).

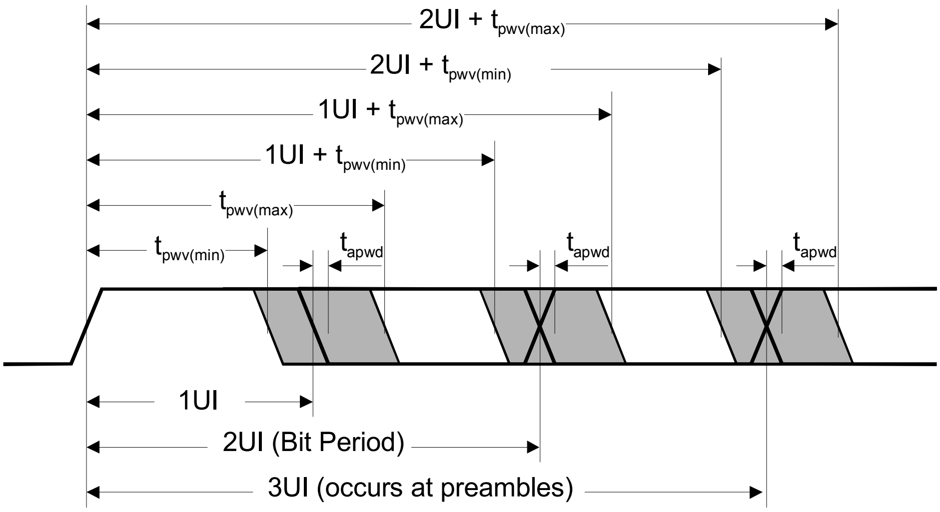

Figure 2-3: Pulse-width-variation and average pulse-width-distortion.

2.1.1.2 Phase-Variation

Phase-variation is always related to a reference signal. Due to the basic causes of phase-variations and their impact on accumulation around the ring, a division in subcategories can be achieved:

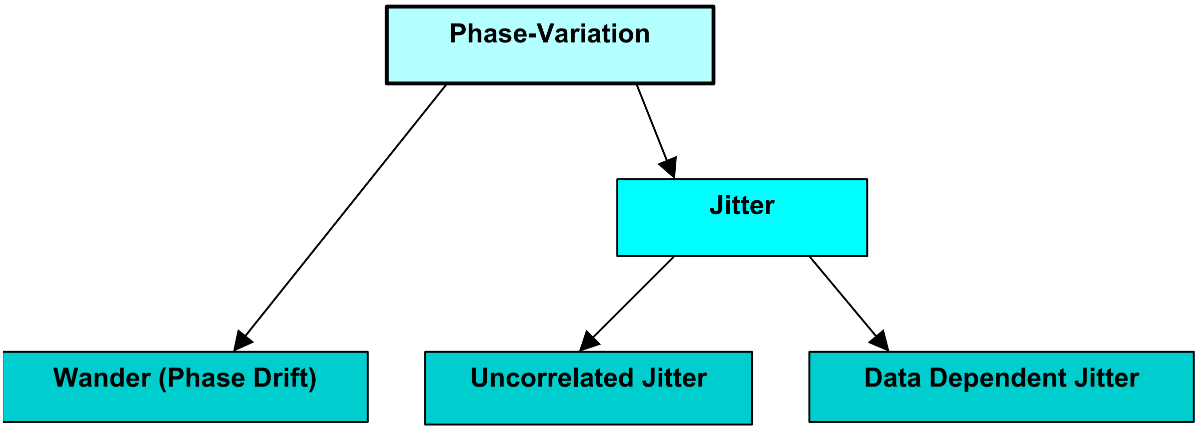

Figure 2-4: Classification of phase-variation.

Wander (Phase Drift):
Wander describes a very low frequency drift (< 1Hz) of transitions in the MOST signal over single components or as an accumulation of component drifts over the whole network. Wander is mainly caused by variations in temperature. All active components between SP1 and SP4 as well as components between SP4 and SP1 will create Wander. All slave PLLs are able to track this kind of Phase-variation, so all parts of Wander are accumulated around the ring.

The Wander must be determined by using constant data content in the MOST frame (e.g. all data channels in the MOST frame are set to 0x00h). A measurement on a whole network typically results in a Wander behavior as shown in Figure 2-5. The hatched line shows the initial phase of the signal. After a certain time period with variation in temperature, the hump is moved. This system wide Wander can be divided up into the particular parts of Wander that are generated by single components, links or nodes.

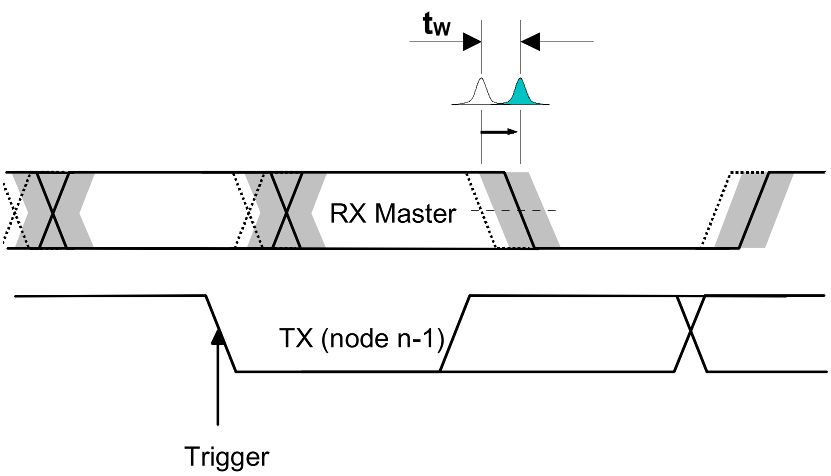

Figure 2-5: Example for Wander of Rx master related to Tx master.

Data Dependent Jitter:
Data dependent jitter (DDJ) is generated by components that have limitations in bandwidth (e.g. EOCs or OECs) along the signal path. The mechanism of accumulation is determined by those PLLs that are part of each slave node. Phase-variations due to changes in the data structure in a low frequency manner accumulates around the ring while high frequency variations are attenuated by the PLLs.

In general the DDJ must be determined by using a transmission signal which alternates from lower border to higher border of the specified bandwidth (all data channels in the MOST frame are set to 0xFFh and to 0x00H for a certain time). In an optical link or a network were DDJ does occur, a histogram measurement shows two humps. Data dependent jitter is defined as the distance between the mean-values of that both humps (t_{DDJ}).
Figure 2-6 shows an example on how to get the data dependent jitter on SP4. The accumulated part of DDJ can also be measured at the Tx of node “n”.

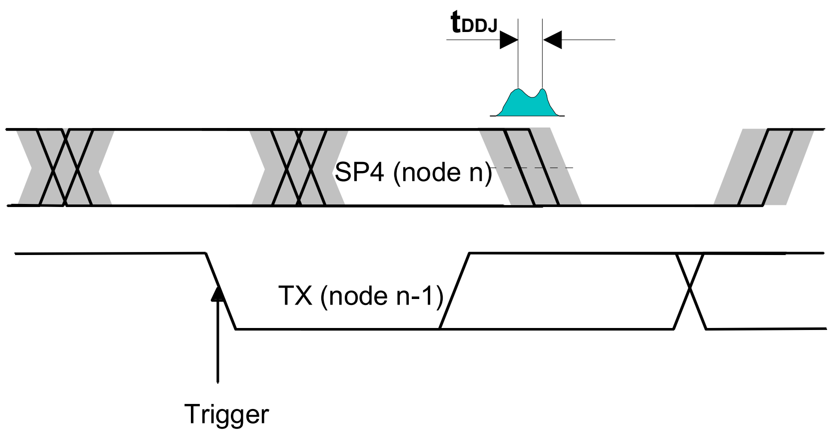

Figure 2-6: Data dependent jitter at SP4 of an optical link.

Please note: The value of t_{DDJ} has to correspond to that edge of the Rx signal, the PLL driven by SP4 does locks to. The value of t_{DDJ} may be different on the rising and the falling edge. That means, the transition that is used by the MOST NIC chip for clock recovery, has to be taken into consideration. Therefore the “active edge” has to be defined in the MOST NIC’s data sheet.

Uncorrelated Jitter (UJ):
All categories of jitter that are not caused by data dependencies are defined as “uncorrelated jitter”. This includes random jitter caused by (white) noise in the electrical stages, power supply noise injection into the electrical components of a link and jitter due to electrical or optical crosstalk.

In general the UJ must be determined by using a transmission signal, which contains a single frequency (e. g. all data channels in the MOST frame are set to 0xFFh). All data dependent effects must be removed. In a histogram measurement, UJ is displayed as a single hump. The distribution ideally is gaussian (Non-gaussian distribution is an indication of bad design, crosstalk, etc.). UJ is determined by the standard deviation. It can be measured on a single optical link as shown in Figure 2-7.

The UJ above the cut-off frequency of the PLL is attenuated while UJ below the cut-off frequency will be accumulated in the ring. The accumulated part of UJ can be measured at the Tx of node n.

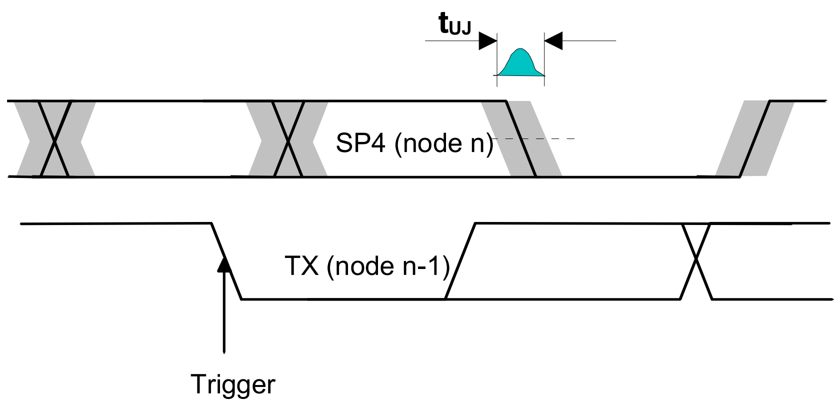

Figure 2-7: Example of uncorrelated jitter at SP4 of an optical link.

Please note: The value of t_{UJ} has to correspond to that edge of the Rx signal, the PLL driven by SP4 locks to. The value of t_{UJ} may be different on the rising and the falling edge. The transition that is used by the MOST NIC for clock recovery has to be taken into consideration. Therefore the "active edge" has to be defined in the MOST NIC's data sheet.

Data Dependent Jitter & Uncorrelated Jitter (UJ):

The combination of DDJ and UJ leads to the total amount of jitter that is created over an optical link (see Figure 2-8).

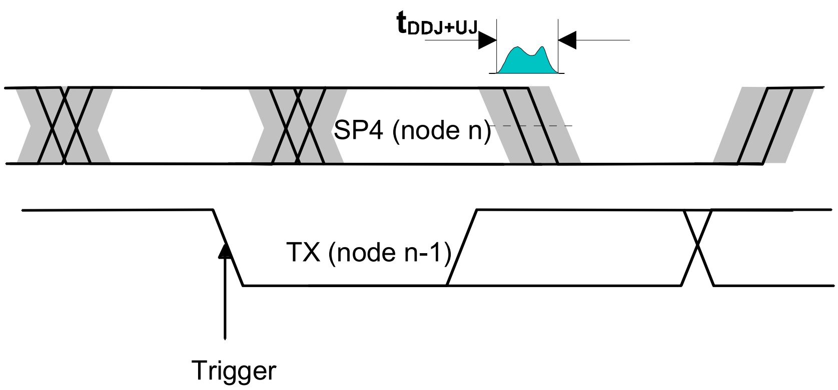

Figure 2-8: Example DDJ and UJ at SP4 of an optical link.

In principle phase-variations can be seen as signal distortion on a single point-to-point link ("link jitter") or from system point of view as the accumulation of all phase-variations around the ring ("system jitter"). In the following tables for SP1 up to SP4, the maximum tolerances for "link jitter " (DDJ and UJ) are shown. The specified limits for SP1 up to SP4 are based on the requirements of MOST NIC chips to attain an appropriate clock recovery. Based on system requirements, phase-variation should be kept as small as possible. Chapter 2.6describes how "system jitter" can be derived using the parameters DDJ, UJ and Wander.

2.1.1.3 Overview Timing-Distortion

The definitions for the different types of timing-distortion given in chapters 2.1.1.1 and 2.1.1.2 are summarized in Figure 2-9.

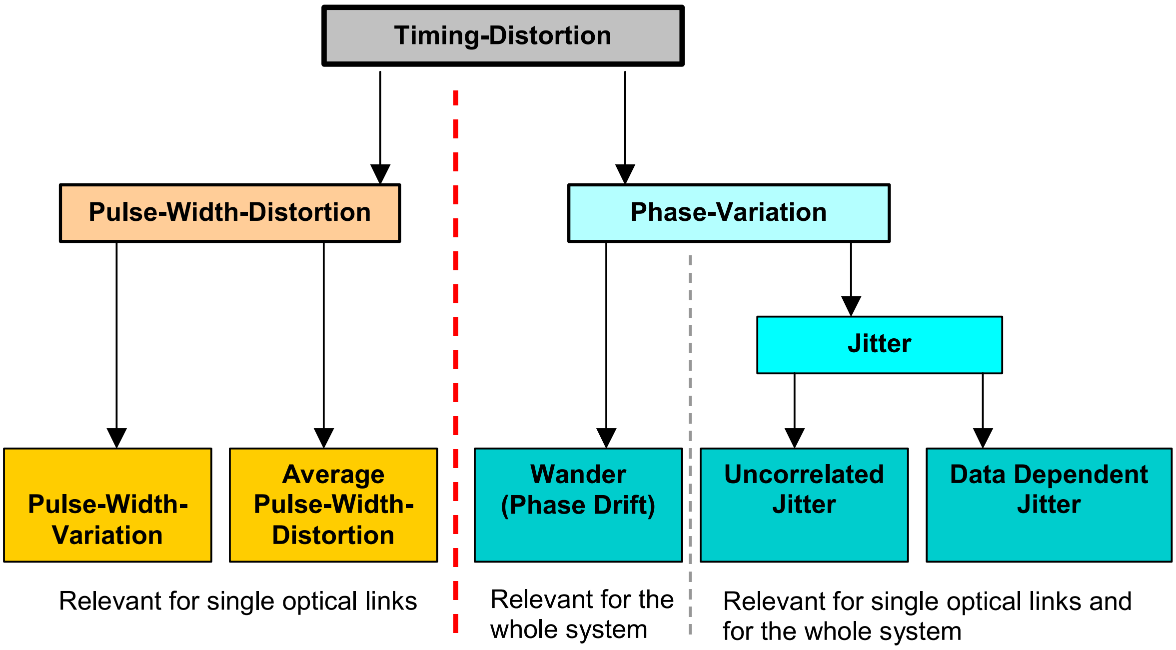

Figure 2-9: Summary of timing-distortion.

Pulse-width-distortion that stays within the specified limits, will be eliminated by the following node. Phase-variation within the specified limits will lead to a proper clock and data recovery on the following node, however parts of the phase-variation will be transferred over the node.

2.1.2 Logic Levels at SP1 and SP4

The specified logic levels at SP1/4 are based on TTL and the timing requirements are related to the corresponding trigger point (see note 3 in Table 2-1 and Table 2-4). Mixing different logic families may cause deviations in the signal timing.

Exception:
When the timing parameters **and** logic levels of both sides of the specification point are compatible to each other, the deviations might be negligible. Since the trigger points are very close to each other, this could be the possible for e.g. a 3V CMOS output driving a TTL input.

As a matter of course, the timing requirements of SP1/4 must be met in any case, especially if other logic families are used than those specified in this document (e.g. CMOS, LVDS, ECL, PECL, etc.).

2.2 Specification Point SP1

	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit rate		Bi-phase mark	4	22.6	25	MBit/s
Low level input voltage	V_{IL1}	1), 6)	-0.3	-	0.8	V
High level input voltage	V_{IH1}	1), 6)	2.0	-	VDD+0.3	V
Rise time (10%-90%)	$t_{r1\_10\text{-}90}$	2)	-	-	0.23	UI
Fall time (90%-10%)	$t_{f1\_90\text{-}10}$	2)	-	-	0.23	UI
Pulse-width-variation	t_{pwv1}	3), 4)	0.955	-	1.045	UI
Average pulse-width-distortion	t_{apwd1}	3), 4)	-0.023	-	+0.023	UI
Data dependent link jitter	t_{DDJ1}	3), 4), 5)	-	-	0.01	UI
Uncorrelated link jitter	t_{UJ1}	3), 4), 5)	-	-	0.0045	UI
Input resistance	R_{I1}	6)	2	-	-	kOhm
Input capacitance	C_{I1}	6)	-	-	10	pF

Note:
This table describes the electrical input signal parameters of an electrical optical converter (see Figure 1-1). All values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements (e.g.: Ta = –40°C ... +85°C, humidity, vibration and shock, resistance against chemical agencies, EMC/EMI, lifetime, etc.)

1) Range of VDD +/- 5%
2) In case of using 20 % - 80 % measurement $t_{r1\_20\text{-}80}$, $t_{f1\_80\text{-}20}$ has to be 0.18 UI
3) Measured at 1.5 V
4) For more information please refer to chapter 2.1, General Remarks
5) Triggered of Tx
6) Input EOC

Table 2-1: Signal parameters of specification point 1.

2.3 Specification Point SP2

	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit rate		Bi-phase mark	4	22.6	25	MBit/s
Peak wavelength	λ_2		630	650	685	nm
FWHM	$\Delta\lambda_2$		-	-	30	nm
Optical output power	P_{opt2}	1), 2), 9)	-10	-	-1.5	dBm
Optical output power “Light off”	P_{OFF2}	2), 3)	-	-	-50	dBm
Extinction ratio	r_{e2}	4)	10	-	-	dB
Rise time (20%-80%)	t_{r2}		-	-	0.27	UI
Fall time (80%-20%)	t_{f2}		-	-	0.27	UI
Pulse-width-variation	t_{pwv2}	5), 6)	0.903	-	1.097	UI
Average pulse-width-distortion	t_{apwd2}	5), 6)	-0.063	-	+0.063	UI
Data dependent link jitter	t_{DDJ2}	5), 6), 8)	-	-	0.035	UI
Uncorrelated link jitter	t_{UJ2}	5), 6), 8)	-	-	0.015	UI
Positive overshoot within 0UI…….2/3UI		7)	-20	-	+25	%
Negative overshoot within -1UI….-1/4UI		7)	-10	-	+20	%
High level signal ripple between 2/3UI and 3/4U		7)	-10	-	+10	%

Note:
This table describes the optical output signal parameters of an electrical optical converter (Figure 1-1). All values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements (e.g.: Ta = –40°C ... +85°C, humidity, vibration and shock, resistance against chemical agencies, EMC/EMI, lifetime, etc.). Components or modules have to fulfill the specified output parameters considering min/max conditions on the input parameters.

1) Average values, when transmitting modulated light @ MOST frame @ signal timing parameters as defined in next chapter
2) Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0mm
3) Average value, when MOST Network off
4) r_{e2}=10*log(b1/b0) average see EN/IEC 61280-2-2
5) Values at 50% of signal amplitude (b1-b0)
6) For more information please refer to chapter 2.1, General Remarks
7) The positive/negative overshot and the signal ripple is related to the signal amplitude b1-b0. The limits for positive/negative overshot must be kept after the rising edge (respectively falling edge) passed b1 (respectively b0). For more detail refer to Figure 2-10
8) Triggered of Tx
9) The designations of IEC 60825-1/-2 'safety of optical fiber communication' have to be taken into account

Table 2-2: Signal parameters of specification point 2.

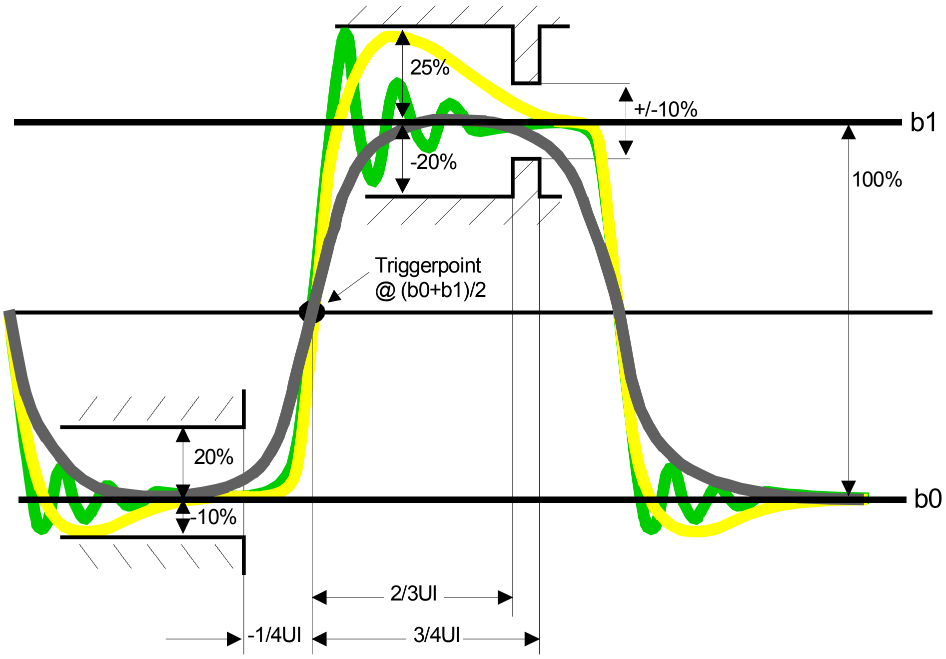

Figure 2-10: Schematic of optical pulses at specification point 2.

2.4 Specification Point SP3

	Symbol	Condition	min.	typ.	max.	Unit
Bit rate		Bi-phase mark	4	22.6	25	MBit/s
Peak wavelength of input signal	λ_3		630	650	685	nm
FWHM of input signal	$\Delta\lambda_3$		-	-	30	nm
Receivable optical power range for data recovery	P_{opt3}	1), 2), 3), 10).	-23	-	-2	dBm
Receivable optical power range for switching to "Light off state"	P_{OFF3}	2), 3), 4), 5)	-40	-	-23	dBm
Extinction ratio	r_{e3}	6)	10	-	-	dB
Rise time (20%-80%)	t_{r3}		-	-	0.31	UI
Fall time (80%-20%)	t_{f3}		-	-	0.31	UI
Pulse-width-variation	t_{pwv3}	7), 8)	0.903	-	1.097	UI
Average pulse-width-distortion	t_{apwd3}	7), 8)	-0.063	-	+0.063	UI
Data dependent link jitter	t_{DDJ3}	7), 8), 9)	-	-	0.035	UI
Uncorrelated link jitter	t_{UJ3}	7), 8), 9)	-	-	0.015	UI
Positive overshoot within 0UI..2/3UI		11)	-20	-	+25	%
Negative overshoot within –1UI..–1/4UI		11)	-10	-	+20	%
High level signal ripple between 2/3UI and 3/4U		11)	-10	-	+10	%

Note:
This table describes the optical input signal parameters of an optical electrical converter (Figure 1-1). All values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements (e.g.: Ta = –40°C ... +85°C, humidity, vibration and shock, resistance against chemical agencies, EMC/EMI, lifetime, etc.)

1) Average values, when receiving modulated light. Tolerance ranges for timing and amplitude specified for SP3 (r_{e3}, t_{r3}, t_{f3}, t_{pwv3}, t_{apwd3}) have to be fulfilled.
2) Value, when incoming signal has passed the receiving contact end face
3) Power within a far field angle of 30° (NA = 0.5) and a diameter of 1.0mm
4) Average values, when receiving modulated light or stray light
5) Value helpful to create a low-current sleep mode operation, meaning of "Light off" see [2] MOST Specification, section 4.2, Optical Interface Area
6) r_{e3}=10*log(b1/b0) average see EN/IEC 61280-2-2
7) Values at 50% of signal amplitude
8) For more information please refer to chapter 2.1, General Remarks
9) Triggered of Tx
10) Assumption of an attenuation of >0.5dB between SP2 and SP3
11) The positive/negative overshoot and the signal ripple is related to the signal amplitude b1-b0. The limits for positive/negative overshoot must be kept after the rising edge (respectively falling edge) passed b1 (respectively b0). For more details refer to Figure 2-10

Table 2-3: Signal parameters of specification point 3.

2.5 Specification Point SP4

	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit rate		Bi-phase mark	4	22.6	25	MBit/s
Low level output voltage	V_{OL4}	1)	0	-	0.4	V
High level output voltage	V_{OH4}	1)	2.5	-	VDD+0.3	V
Rise time (10%-90%)	t_{r4_10-90}	1), 2)	-	-	0.45	UI
Fall time (90%-10%)	t_{f4_90-10}	1), 2)	-	-	0.45	UI
Pulse-width-variation	t_{pwv4}	1), 3), 4)	0.743	-	1.40	UI
Average pulse-width-distortion	t_{apwd4}	1), 3), 4)	-0,15	-	0.316	UI
Data dependent link jitter	t_{DDJ4}	3), 4), 5)	-	-	0.15	UI
Uncorrelated link jitter	t_{UJ4}	3), 4), 5)	-	-	0.045	UI

Note:
This table describes the optical output signal parameters of an optical electrical converter (Figure 1-1). All values have to be guaranteed under automotive worst-case conditions, which have to be considered as OEM specific requirements (e.g.: Ta = –40°C ... +85°C, humidity, vibration and shock, resistance against chemical agencies, EMC/EMI, lifetime, etc.). Components or modules have to fulfill the specified output parameters considering min/max conditions on the input parameters.

1) Assuming a load of 50 kOhm / 10 pF
2) In case of using 20 % - 80 % measurement t_{r4_20-80}, $t_{f4\ 80-20}$ has to be 0.34 UI
3) Measured at 1.5 V
4) For more information please refer to chapter 2.1, General Remarks
5) Triggered of Tx

Table 2-4: Signal parameters of specification point 4.

2.6 Additional Requirements for System Design

In the previous chapters all timing parameters were well discussed, with the main focus on single optical links. The specified parameters in SP1 up to SP4 are the base for an accurate point-to-point link. However, some parameters have been detected which influence the entire system behavior of a MOST Network due to their ability to accumulate around the ring.

All the accumulating effects are covered by the expression “phase-variation”. The subcategories of phase-variation were defined as Wander, uncorrelated jitter and data dependent jitter. From the system perspective, a limiting of parameters on system-level is required, based on the parameters specified in SP1 up to SP4.

The limitation for network stability on system level is determined by the ability of the master node to tolerate phase-variations. The maximum amount of phase-variation for a MOST NIC in timing master mode is called master-jitter-tolerance. It represents the allowed system jitter, which is relevant for system-related examination. This parameter has to be defined in the data sheet of each MOST Network Interface Controller.

Jitter accumulation is determined by the characteristic of the PLLs that are implemented in each slave node. The mechanism how phase-variations are transferred over a slave node is a function of frequency. Phase-variation with low frequency characteristic will be transferred completely due to the ability of PLLs to track such kind of phase deviation. Variations in phase delay that change in high frequency manner will be attenuated since the PLL cannot track that kind of deviation.

Table 2-5 shows the overall formula determining the minimum value for the master-jitter-tolerance. The relevance of the different types of phase-variation on the jitter accumulation is shown in Table 2-6.

Master-Jitter-Tolerance

The requirements for the system-design are combined in the formula below:

$$\text{M-Jitter-Tol.} \geq \sum_{n=1}^{m} t_W(n) + \sum_{n=1}^{m-1} t_{DDJacc}(n) + \sum_{n=1}^{m-1} t_{UJacc}(n) + t_{DDJ}(m) + t_{UJ}(m)$$

m:	Number of nodes/optical links in a ring
$t_W(n)$:	Wander (Phase Drift) per node and optical link
$t_{DDJacc}(n)$:	Accumulated data dependent jitter per node to node [Tx(n-1)→Tx(n)]
$t_{UJacc}(n)$:	Accumulated part of uncorrelated jitter per node to node [Tx(n-1)→Tx(n)]
$t_{DDJ}(m)$:	Data dependent jitter of the last link
$t_{UJ}(m)$:	Uncorrelated jitter of the last link

The sum of $t_{DDJ}(m)$ and $t_{UJ}(m)$ is the link jitter between last Slave TX and SP4 of the timing master.

Table 2-5: Relationship of system jitter parameters.

Phase-Variation	Formula	Consequence on Jitter Accumulation
Accumulation of Wander	$\sum_{n=1}^{m} t_W(n)$	Due to the low frequency characteristic of Wander, that kind of phase-variation is transferred completely over a PLL. Wander is generated by all active components of the optical link and by the MOST NIC. Wander is caused by variations in temperature. It has to be specified in the data sheet of each active component. Each part of Wander that occurs somehow in the network has impact on the master-jitter-tolerance.
Accumulation of data dependent jitter	$\sum_{n=1}^{m-1} t_{DDJacc}(n)$	Bandwidth limitations in components along an optical link in combination with a data signal that consists of different frequencies affect the phase delay of the transitions in the data stream related to the reference signal. Due to the bi-phase coding, in principle two different frequencies are transferred, 256*FS for 2UI elements and 512*FS for the 1UI-elements. The 3UI-elements appears only once per MOST frame and has no impact on jitter accumulation. At the input of the PLL (driven by SP4), a specific delay position for each frequency can be found. Variation between both frequencies causes phase shifts. So the phase relation depends on the data content. The response of a PLL on such phase shifts has a low pass characteristic. Phase shifts that occur in a frequency higher than the cut off frequency will be attenuated. Phase shifts that occur in a frequency lower than the cut off frequency will be tracked and therefore transferred through the PLL. The frequency of phase shifts is determined by the maximum length of such data segments that contain constant data (0x00h or 0xFFh respectively). Only the accumulated part of t_{DDJ} has to be taken into consideration.
Accumulation of uncorrelated jitter	$\sum_{n=1}^{m-1} t_{UJacc}(n)$	In principle UJ is a kind of random distortion, so all potential frequencies may occur (wide band). UJ in a frequency range below the cut-off-frequency will be tracked, UJ above the cut-off-frequency UJ will be attenuated. Only the accumulated part of t_{UJ} has to be taken into consideration.
Link jitter between last slave TX and SP4 of the timing master	$DDJ\,(m) + UJ\,(m)$	The timing master node has no PLL within its input stage, therefore the full amount of jitter (DDJ plus UJ, both peak-peak) of the last link has to be added to the accumulated part of jitter plus Wander present at the Tx of the last slave.

Table 2-6: System jitter parameters.

A MOST system that complies with the above formula, will guarantee system stability under all conditions. If there is a gap between master-jitter-tolerance and the calculated system jitter, a more detailed investigation of the particular system is required.

Please Note: The measurement method for DDJ and UJ is defined under worst-case conditions to achieve precise and separated information about the specific types of phase-variation. Especially DDJ is determined using specific data patterns that will not appear in real systems.

Remarks for a detailed system design and analysis:

- The master-jitter-tolerance parameter is different for individual versions of the NIC chips. Different solutions with different tolerances are available.
- The amount of phase-variation at Rx of the timing master depends on the number of nodes and optical links.
- DDJ and UJ mainly are generated within the OECs. The grade of jitter due to OECs depends on parameters like temperature and especially optical input power. The values for jitter (DDJ and UJ) stated in the data sheet are specified for worst-case conditions. For instance a rough estimation of the expected input power at each device within a real network will show that probably not all inputs will be driven at the same input power range. So a comparison between the expected range of optical input power and the maximum jitter in that input power range will lead to reduced values for DDJ and UJ.
- The accumulation of DDJ depends on maximum length of the data segment within the MOST frame that may contain constant data (0x00H or 0xFFh). Very often, this data segment is defined by the area for packet data transportation. This area should be reduced to the minimum size that is required for the designed packet data rate.

3 Device Connection

3.1 Connector Interfaces

Table 3-1 summarizes the five specified hybrid connector interfaces.

Please Note: The optical contacts located at SP2 and SP3 are combined in a single duplex connector.

"Nick name"	Number of optical contacts	Number of electrical contacts		
		PIN = 0,63 mm	PIN = 1,5 mm	PIN = 2,8 mm
2+0	2	-	-	-
2+4	2	4	-	-
2+12	2	12	-	-
2+20	2	18	2	-
4+40	2 x 2	2 x 12	-	2 x 8

Table 3-1: Connector family.

The following table indicates the drawing codes and the file names of the specified connector interfaces.

"Nick name"	Drawing code	TIFF file	Drawing date
2+0	MOST-CON-2-0	MOST-CON-2-0.TIF	6.02.2001
2+4	MOST-CON-2-4	MOST-CON-2-4.TIF	6.02.2001
2+12	MOST-CON-2-12	MOST-CON-2-12.TIF	6.02.2001
2+20	MOST-CON-2-20	MOST-CON-2-20.TIF	6.02.2001
4+40	MOST-CON-4-40	MOST-CON-4-40.TIF	6.02.2001
Fiber module interface	MOST-FM-I	MOST-FM-I.TIF	6.02.2001
Test connector	MOST-CON-T	MOST-CON-T.TIF	6.02.2001
LWL collar	MOST-FM-C	MOST-FM-C.TIF	6.02.2001
		TIFF files available on www.mostcooperation.com	

Table 3-2: Drawing codes and file names of connector interfaces.

3.2 Connector Interface Loss

Figure 3-1 shows details of the connector insertion loss D_{con} between devices and cabling:

- The attenuation of optical power may not exceed $D_{conmax2}$ = 2.5 dB, when optical signal transits from SP2 into the cabling fiber.
- The attenuation of optical power may not exceed $D_{conmax3}$ = 2.5 dB, when optical signal transits from the cabling fiber into SP3.

Please Note: The maximum connector attenuation is a part of the "*MOST Specification of Physical Layer*".

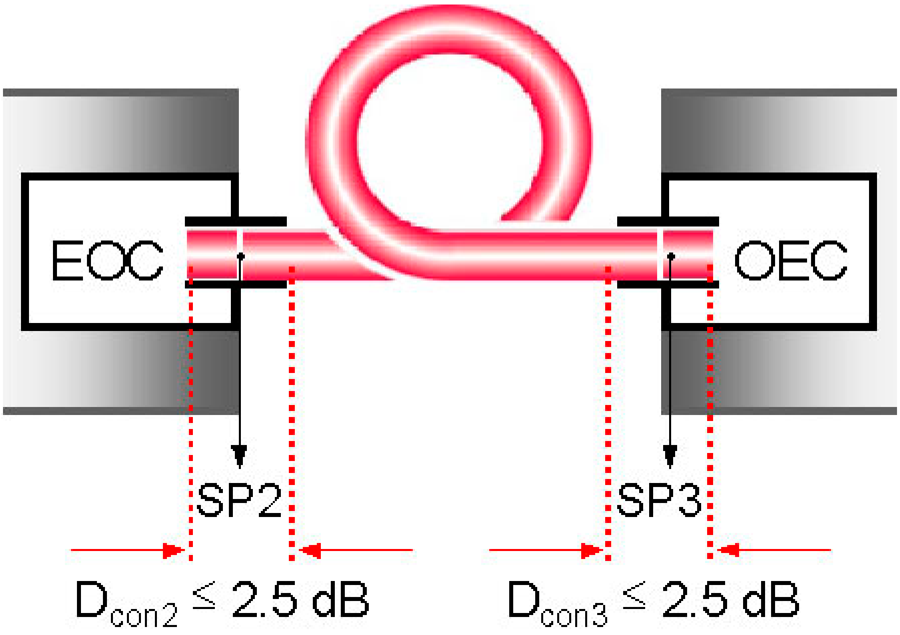

Figure 3-1: Connector insertion loss.

4 Appendix A: List of Figures

5 Appendix B: List of Tables

6 Appendix C: Abbreviations

APWD	Average pulse-width-distortion
B	Bit rate
DDJ	Data dependent jitter
EMC	Electro magnetic compatibility
EMI	Electro magnetic immunity
EOC	Electrical optical converter
FS	Frame sync per second (System sample frequency)
FWHM	Full width at half maximum
NA	Numerical aperture
NIC	MOST Network Interface Controller (MOST Protocol Chip)
OEC	Optical electrical converter
OEM	Original equipment manufacturer
PLL	Phase locked loop
PWV	Pulse width variation
Rx	Electrical input of the NIC
SPn	Specification point No. n (n= 1 … 4)
Ta	Ambient temperature
Tx	Electrical output of the NIC
UI	Unit interval
UJ	Uncorrelated jitter
W	Wander