MOST

Media **O**riented **S**ystems **T**ransport
Multimedia and Control
Networking Technology

MOST Physical Media Dependent Sublayer Specification

Rev. 3.1
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Contents

Document History

MOST Physical Media-Dependent Sublayer Specification Rev. 3.1

Change Ref.	Section	Changes
3V1_001	All	Initial document.

Bibliography

Information: Table Bibliography-1 lists all documents, which are referenced by this MOST document, along with their versions.

Document	Revision
MOST Specification	3.1
MOST Data Link Layer Specification	3.1
MOST Physical Layer Basic Specifcation	1.0
MOST150 oPHY Automotive Physical Layer Sub-Specification	1.1
MOST150 cPHY Automotive Physical Layer Sub-Specification	1.1

Table Bibliography-1: Document references

Glossary

Information: Table Glossary-1 lists commonly used terms and their definition.

Term	Definition
DC	Direct current
DCA code	DC Adaptive code
DSV	Digital sum value

Table Glossary-1: Glossary entries

1 Introduction

1.1 Purpose

This document specifies the MOST physical media dependent sublayer.

1.2 Scope

This document describes the DC Adaptive code for encoding the network bitstream, MOST network identifiers, as well as data descrambling/scrambling for MOST150 oPHY and MOST150 cPHY.

2 DCA (DC Adaptive) Code

The MOST network uses the DC Adaptive (DCA) code for encoding the network bitstream. DCA code is a DC-free code requiring only half the data rate of the bi-phase coding scheme.

The network bit-stream is encoded to DCA by making the data transition from high to low or from low to high occur either in the middle of the bit-period, at the bit-period boundary, or not at all. The transitions ensure that the Digital Sum Value (DSV), which is the cumulative direct current (DC) value of the DCA encoded bit stream, is always equal to either -1, 0, or +1. The DSV remains unchanged if there is a middle transition. If there is no middle transition, the DSV increases by 1 if the data is high at the beginning of the bit-period and decreases by 1 if the data is low at the beginning of the bit-period.

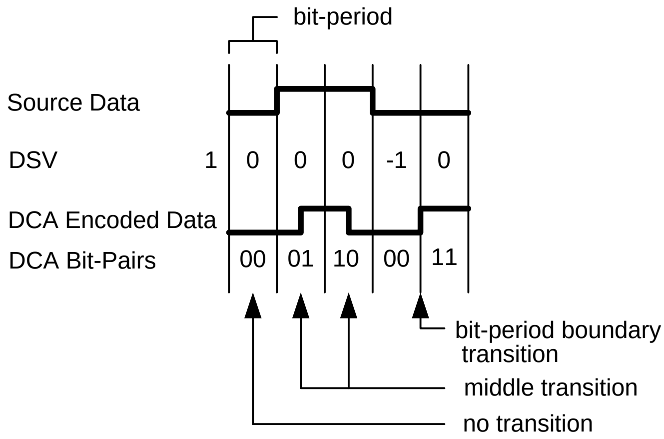

Figure 2-1: DCA code

Each bit-period of the DCA encoded data can be represented by either ‘00’, ‘01’, ‘10’, or ‘11’. These two bits comprise a DCA bit-pair and represent a single source data bit. Thus 8 DCA bit-pairs are required to represent a source data byte. The encoded data bit rate, even though it appears to be twice the source data bit rate, is in fact the same as the source data bit rate. This is due to the fact that the encoding algorithm does not permit two transitions in a single bit-period (i.e., a middle transition cannot immediately precede or follow a bit-boundary transition).

The DCA code can be described as follows:

<u>In general</u>

- To encode a ‘1’ there is a transition in the middle of the bit-period.
- To encode a ‘0’ there is no transition in the middle of the bit-period.
- There is a transition at the bit-period boundary, unless there is a middle transition in the bit-period before the bit-period boundary or a middle transition in the bit-period following the bit-period boundary.
- A DSV is incremented or decremented according to the DC value of the coded data. The DSV of a bit-period with a middle transition is the same as the DSV of the previous bit-period. The DSV of a bit-period with no middle transition is +1 of the DSV of the previous bit-period if the encoded data is high during the bit-period and -1 of the DSV of the previous bit-period if the encoded data is low during the bit-period.

<u>Exception</u>

To encode a pair of ones (‘11’) if the DSV of the bit prior to the pair is non-zero, there is no transition in the middle of either bit-period and no transition at the bit-period boundary between the two bit-periods.

2.1 Encoding

The DCA encoding algorithm shown in both Figure 3-2 and Table 3-1, describes the encoding of a source data bit stream (bit1bit2bit3...) into DCA encoded data. The algorithm determines whether there is a transition at the beginning of the bit-period, in the middle of the bit-period, or neither at the beginning nor in the middle of the bit-period. The encoding of bitn is based on the current bit value (bit_n), the next bit value (bit_{n+1}), the DSV value of the previous bit ($dsv\_sum_{[0...n-1]}$), the multiple_ones state and the middle_transition state.

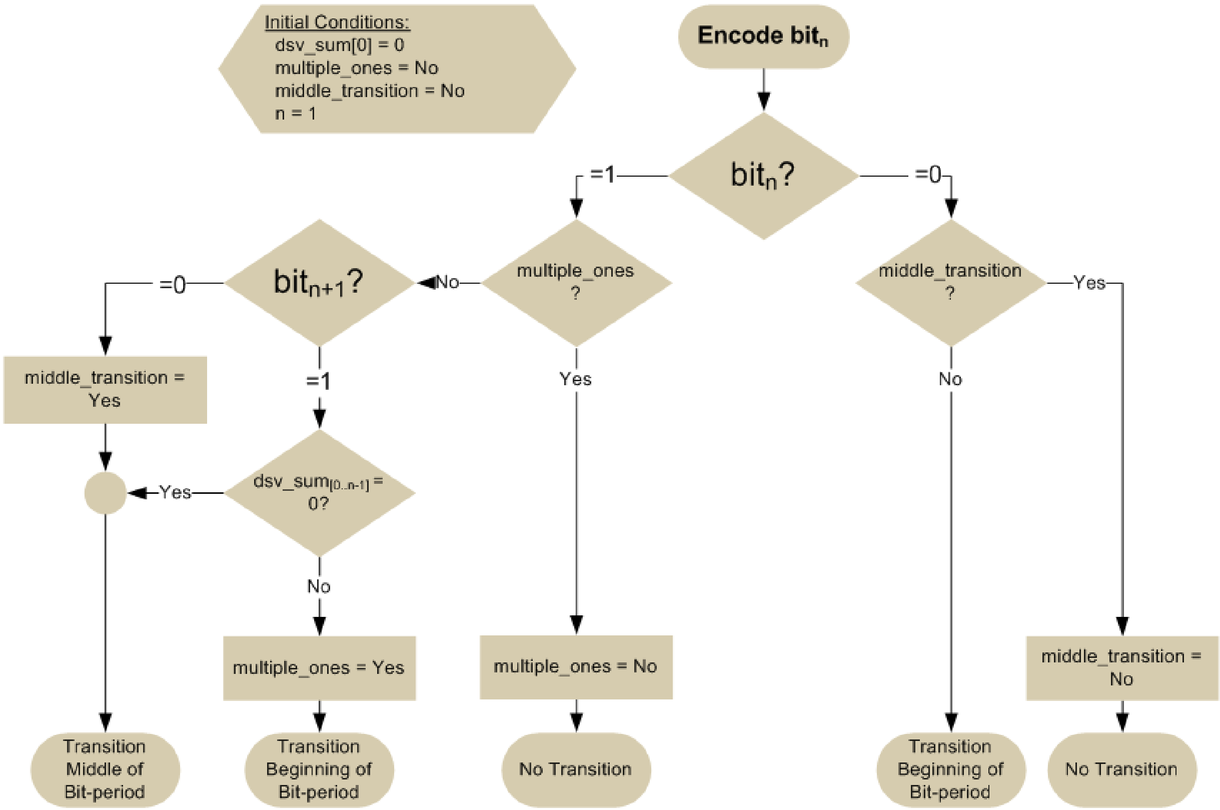

Figure 2-2: DCA encoding algorithm

	Inputs					Outputs			
Line	**bit_n**	**bit_{n+1}**	**$dsv\_sum_{[0..n-1]}$**	**middle _transition**	**multiple _ones**	**transition**	**middle _transition**	**multiple _ones**	**next line**
e1	0	X	X	No	X	beginning	unchanged	unchanged	*e1,e3,e4,e5*
e2	0	X	X	Yes	X	none	No	unchanged	*e1,e3,e4,e5*
e3	1	0	X	X	No	middle	Yes	unchanged	*e2*
e4	1	1	0	X	No	middle	Yes	unchanged	*e3,e4*
e5	1	1	-1,1	X	No	beginning	unchanged	Yes	*e6*
e6	1	X	X	X	Yes	none	unchanged	No	*e1,e3,e5*
Initial Conditions: dv_sum[0] = 0, middle_transition = No, multiple_ones = No, n = 1									

Table 2-1: DCA encoding algorithm

2.2 Decoding

The DCA bit stream can be decoded by using the algorithm described in Figure 3-3 and Table 3-2.

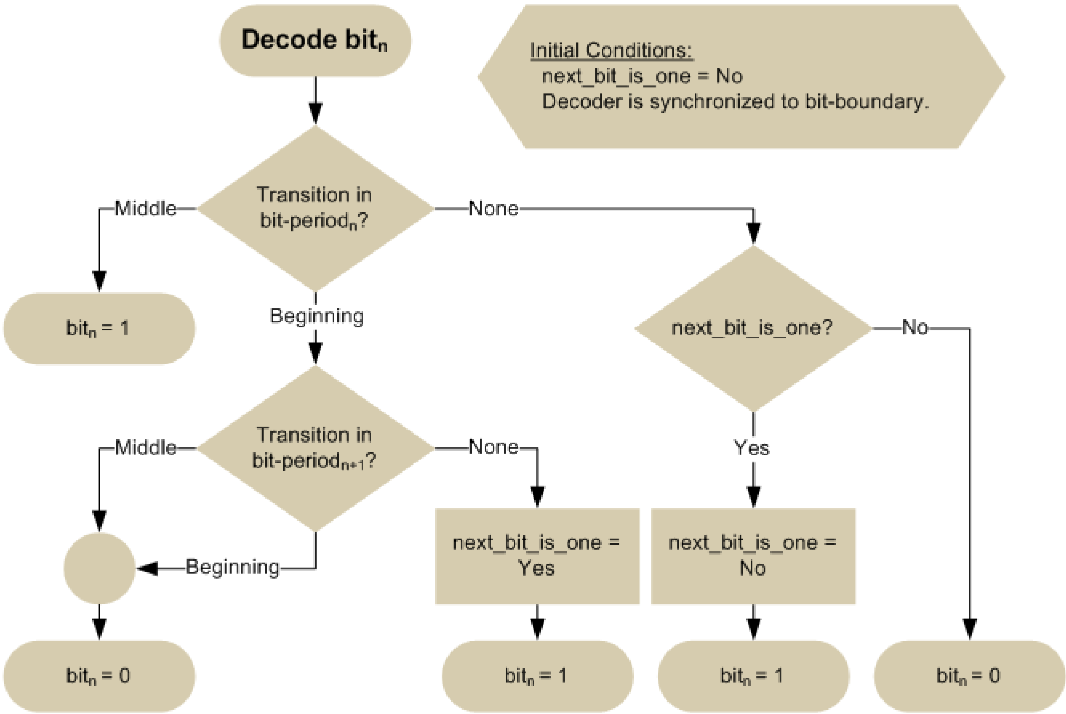

Figure 2-3: DCA decoding algorithm

Inputs			Outputs	
transition in bit-period$_n$	**transition in bit-period$_{n+1}$**	**next_bit_is_one**	**bit$_n$**	**next_bit1**
middle	X	X	1	unchanged
beginning	none	X	1	Yes
beginning	beginning or middle	X	0	unchanged
none	X	No	0	unchanged
none	X	Yes	1	No

Table 2-2: DCA decoding algorithm

3 MOST Network Identifiers

3.1 PREAMBLE Identifier

The PREAMBLE identifier is generated by the TimingMaster. TimingSlaves use the PREAMBLEs they receive to internally synchronize their hardware to the MOST network frame. TimingSlaves also create PREAMBLEs at their output, but based upon the timing of the PREAMBLEs they receive at their input. If there are no incoming PREAMBLEs, the TimingSlaves keep creating PREAMBLEs based upon their inherent timing.

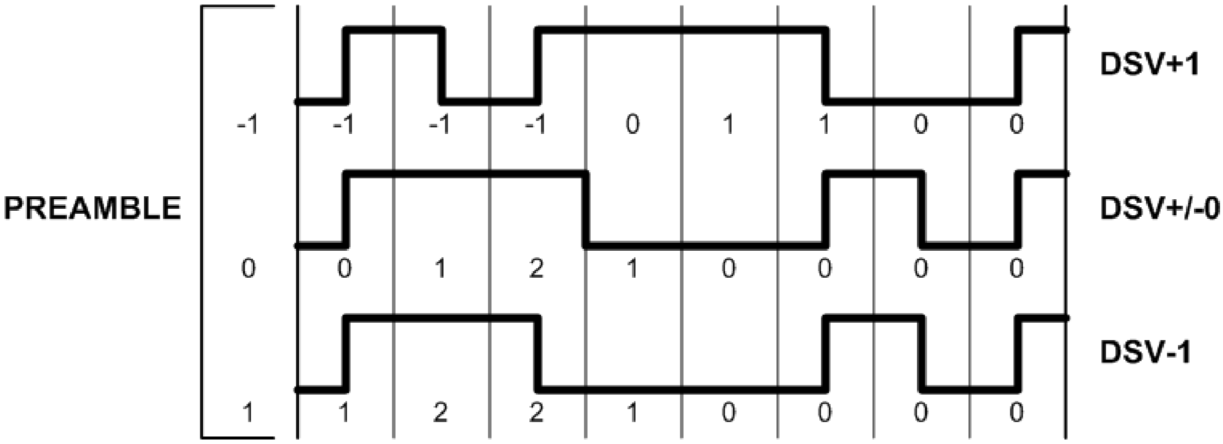

Figure 3-1: PREAMBLE identifier

Lock is achieved, whenever three consecutive PREAMBLEs are received that were aligned to the bit stream and occurred at the correct bit location in the MOST network frame. Once locked, if the receiver does not receive an aligned PREAMBLE at the correct bit location for two consecutive frames, the receiver is no longer locked. For transitions from unlock back to lock, four consecutive and correctly located PREAMBLEs are required to ensure lock. The 1st PREAMBLE provides the reference for counting the MOST network frame bytes. The 2nd - 4th PREAMBLEs then represent the three consecutive PREAMBLEs required to declare lock. If the 1st PREAMBLE that is received should already be aligned to the correct bit location, it will take only three PREAMBLEs to gain lock.

3.2 START Identifier

The START identifier is used to indicate a start condition for various kinds of data transfer mechanisms.

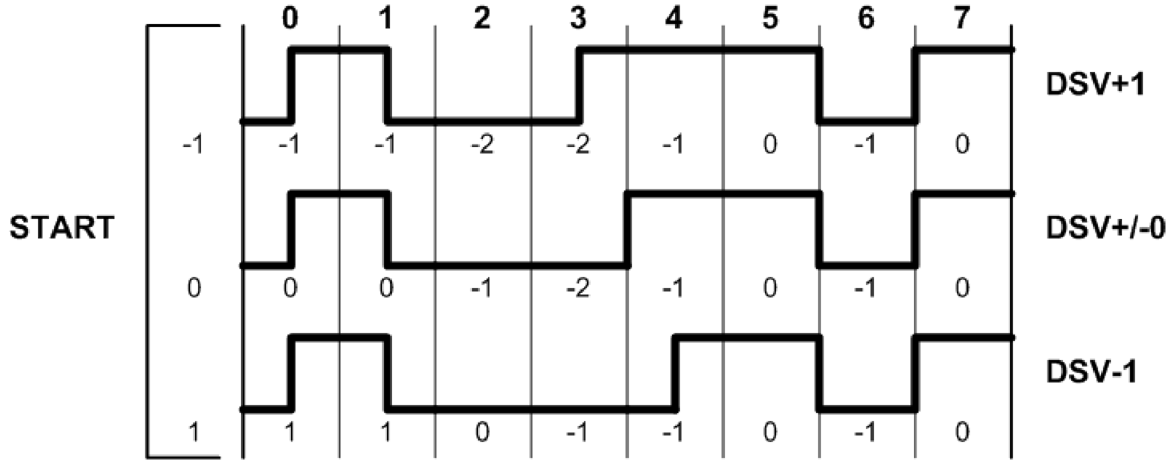

Figure 3-2: START identifier

An incoming START identifier is bypassed by default, unless the operating conditions, such as packet arbitration, require replacing it.

3.3 END Identifier

The END identifier is used to indicate an end condition for various kinds of data transfer mechanisms.

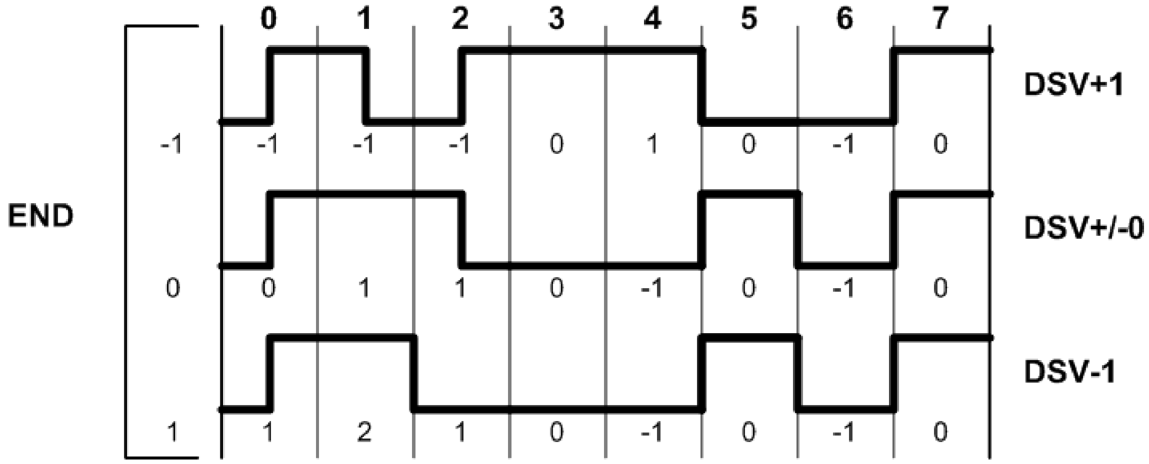

Figure 3-3: END identifier

An incoming END identifier is bypassed by default, unless the operating conditions, such as packet arbitration, require replacing it.

3.4 WAIT Identifier

The WAIT identifier is used for various kinds of data transfer mechanisms.

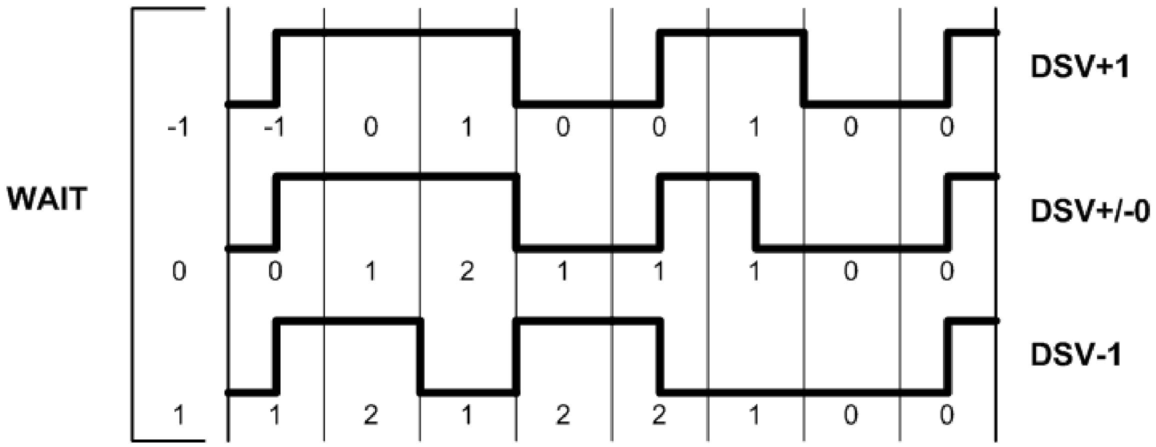

Figure 3-4: WAIT identifier

An incoming WAIT identifier is bypassed by default, unless the operating conditions, such as packet arbitration, require replacing it.

4 Data Descrambling/Scrambling

Data descrambling/scrambling is required to randomize data on the physical layer of the MOST network. Scrambling is mandatory for all nodes and includes all bytes of the MOST network frame except the network identifiers.

The descrambler and the scrambler described below are additive synchronous units based upon 15-bit shift registers. The descrambler is self-synchronizing and descrambles correctly after 15 bits.

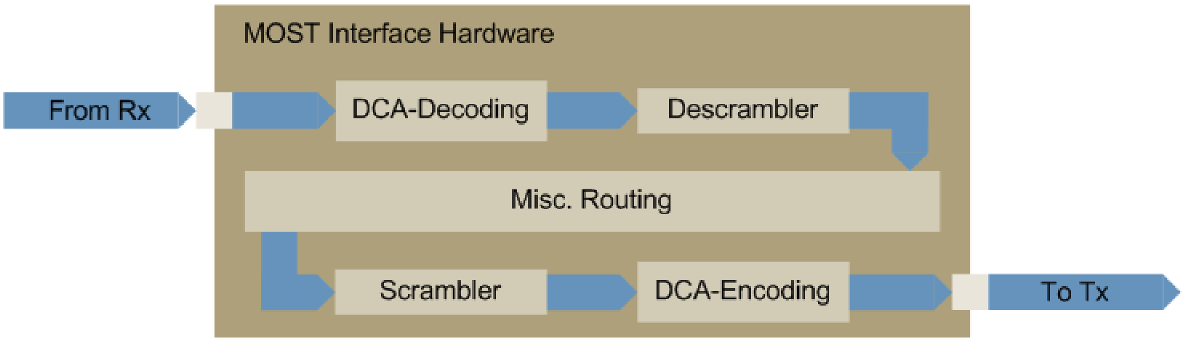

Figure 4-1: Block diagram for descrambling/scrambling

4.1 Descrambler

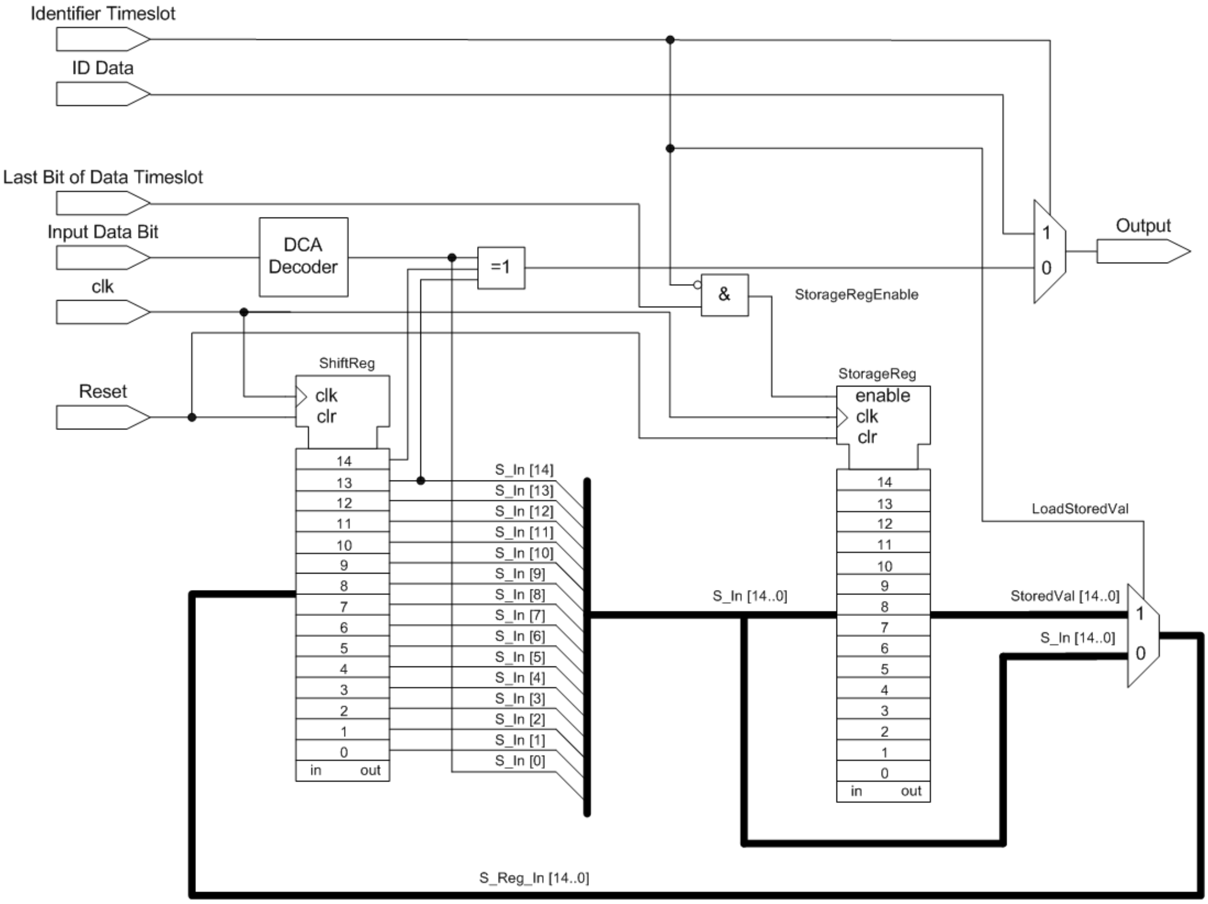

Figure 4-2: Descrambler circuitry

4.2 Scrambler

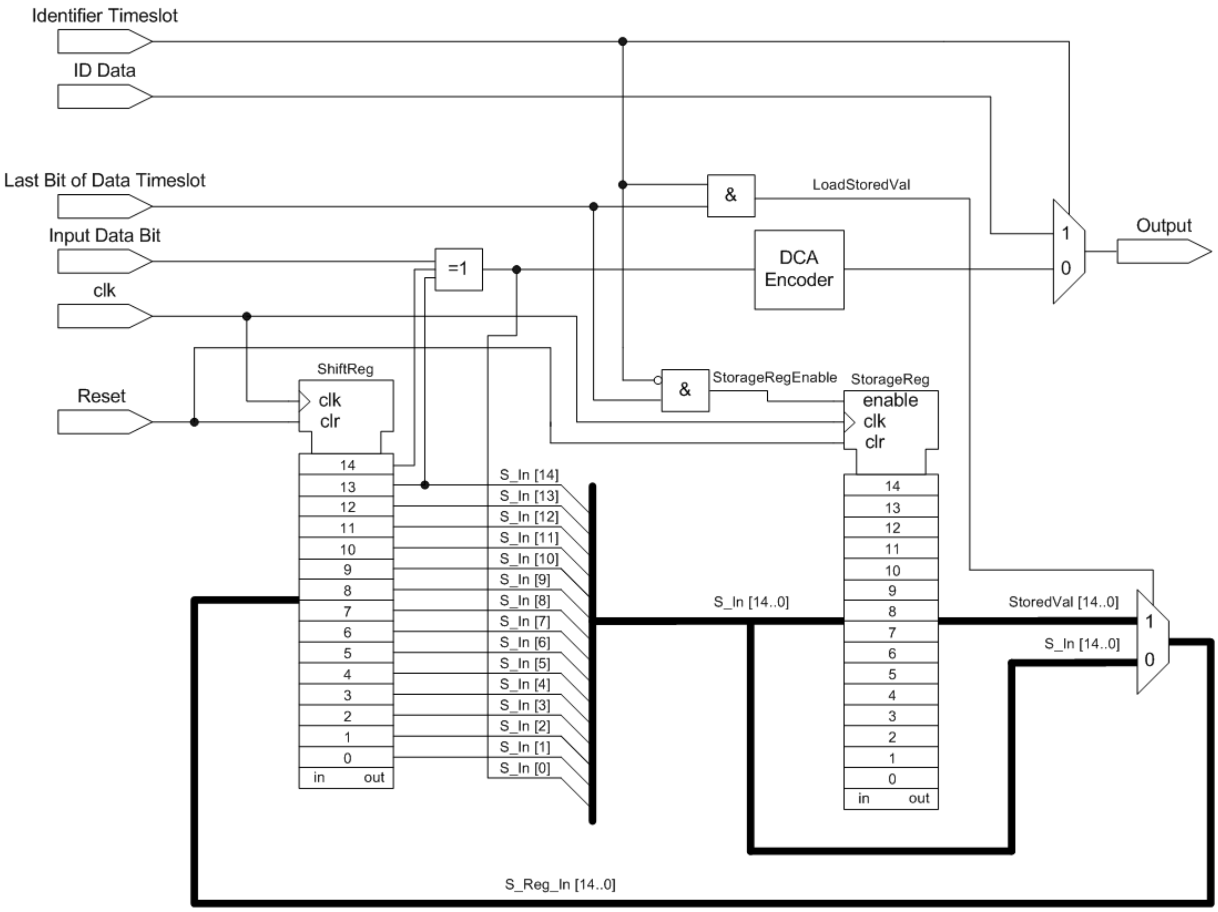

Figure 4-3: Scrambler circuitry

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